NANOSCALE DG FINFETS: SCALING ISSUES, DEVICE OPTIMIZATION AND APPLICATION TO SRAMS

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

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ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices and VLSI Technology)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work which is being presented in this dissertation report, entitled **"Nanoscale DG FinFETs: Scaling Issues, Device Optimization and Application to SRAMs "**, and is being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Semiconductor Devices and VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work, carried out from June 2008 to June 2009, under the guidance and supervision of **Dr. S. Dasgupta**, Assistant Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee.

The results embodied in this dissertation have not been submitted for the award of any other Degree or Diploma.

Date : 30/06/09
Place : Roorkee

Tapas Dutta.

Tapas Dutta

CERTIFICATE

This is to certify that the statement made by the candidate is correct to best of my knowledge and belief.

Date: 30/06/09
Place: Roorkee

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Tapas Dutta,
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ABSTRACT

Double gate FinFETs have emerged as promising devices that can replace bulk MOSFETs as we approach sub-45 nm technologies. In these devices the short channel effects are reduced because of better gate control and the use of a thin and lightly doped channel. In this dissertation report, a detailed analysis of the various scaling issues pertaining to DG FinFETs has been carried out through 2D simulations, including quantum corrections, using a state of the art device simulator. The effects of scaling down the device dimensions like gate length, fin thickness, gate oxide thickness and gate thickness were studied. The impacts on the transistor on current, off state leakage current, threshold voltage, transconductance, DIBL, subthreshold slope, and the gate leakage have been analyzed. The effect of variation of doping densities in the fin region was also studied.

An attempt was made to optimize the DG FinFET devices to approach the ITRS targets for the year 2015 for HP (High Performance) applications. Source/Drain doping engineering, gate dielectric engineering, spacer engineering and metal gate work function engineering were explored for achieving optimal characteristics.

Finally, a 6T SRAM cell was designed and simulated using the optimized FinFETs at 15 nm, using mixed mode simulations. The effects of work function modulation and V_{dd} scaling were examined using the read stability and write ability metrics based on conventional butterfly curves and N-curves. It was demonstrated that work function engineering can be an alternative method to improve the cell performance, without resorting to transistor sizing.

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List of Abbreviations

Abbreviation	Expansion
DG	Double Gate
FinFET	Fin structure Field Effect Transistor
SOI	Silicon on Insulator
BTBT	Band To Band Tunneling
SRAM	Static Random Access Memory
SRH	Shockley–Read–Hall
WKB	Wentzel-Kramers-Brillouin
DIBL	Drain Induced Barrier Lowering
FIBL	Fringe Induced Barrier Lowering
SCE	Short Channel Effect
RDF	Random Dopant Fluctuation
ITRS	International Technology Roadmap for Semiconductors
NTRS	National Technology Roadmap for Semiconductors
EOT	Effective Oxide Thickness
SoC	System on chip
ASIC	Application Specific Integrated Circuit
SPICE	Simulation Program with Integrated Circuit Emphasis
SNM	Static Noise Margin
RNM	Read Noise Margin
WNM	Write Noise Margin

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Chapter 1

Introduction

1.1 Device Scaling Trends

The semiconductor industry has witnessed a phenomenal increase in transistor density in integrated circuits in the last four decades, keeping the famous Moore's law alive in this age i.e. doubling the number of transistors per unit area on the chip every 18-24 months [1]. Table 1 illustrates this exponential increase in the transistor count in the Intel microprocessors from the year 1971 to 2004. All this has been possible due to aggressive scaling of the device dimensions, nowadays approaching sub 50 nm gate lengths.

Table 1: Increase in transistor counts since 1971 [2]

Microprocessor	Year of Introduction	Transistors
4004	1971	2,300
8008	1972	2,500
8080	1974	4,500
8086	1978	29,000
Intel286	1982	134,000
Intel386™ processor	1985	275,000
Intel486™ processor	1989	1,200,000
Intel® Pentium® processor	1993	3,100,000
Intel® Pentium® II processor	1997	7,500,000
Intel® Pentium® III processor	1999	9,500,000
Intel® Pentium® 4 processor	2000	42,000,000
Intel® Itanium® processor	2001	25,000,000
Intel® Itanium® 2 processor	2003	220,000,000
Intel® Itanium® 2 processor (9MB cache)	2004	592,000,000

Maintaining this continuous scaling trend is not possible with the bulk devices as the device performance degrades due to small dimension effects and hence novel device structures are being researched actively. A common approach in these new devices is the use of an ultra thin layer of silicon as the channel which minimizes the short channel effects by eliminating the leakage paths from the gate. Also, in recent years, a lot of research has been done on multi gate MOS devices. The SOI (Silicon on Insulator) multi-gate FETs offer many

advantages over the classical MOS devices through better channel control which makes these devices very attractive in this age of ultra-scaling [3].

One of the promising non-classical devices is the double-gate FinFET. This is a self-aligned nanoscale structure having a vertical channel and has the ability to facilitate more aggressive geometrical scaling as we approach the sub 45 nm technology nodes.

As the dimensions of the transistor go on shrinking, the short channels effects worsen significantly. In FinFETs the Short-channel effects are reduced as compared to a bulk MOSFET. These devices have sharper subthreshold slopes which allows for better switching-off in the device. Also, the threshold voltage is controlled without the use of heavy channel doping, thereby eliminating the problematic random doping fluctuations and at the same time reducing the mobility degradation due to scattering and the drain to body BTBT leakage currents.

1.2 Thesis Contribution

In this work, the various scaling issues in FinFETs with channel lengths of 30 nm and below have been investigated in detail through device simulations using a state of the art numerical device simulator. The effects of scaling the gate length, the fin thickness, the gate insulator thickness, the fin extension lengths and gate thickness have been investigated. Quantum mechanical effects which become prominent in the nanometer regime have been included in the simulations for getting a realistic picture.

DG FinFETs at the 15 nm technologies were optimized so as to approach the ITRS targets for the year 2015 for HP (High Performance) applications. Source/Drain doping engineering, gate dielectric engineering, spacer engineering and metal gate work function engineering were applied to approach the targets.

A 6T SRAM cell was designed using 15 nm FinFETs and its performance was evaluated with respect to the noise margins based on the conventional butterfly curves as well as n-curves.

1.3 Thesis Organization

Rest of this report is organized as follows:

Chapter 2 begins with a brief description of the FinFET device structure and fabrication techniques followed by the details of the simulation methodology used in this work. The Sentaurus device simulation suite from Synopsys was used. This chapter explains the tool flow in Sentaurus, the different physical models that were included in the simulations and details of the parameter extraction methods adopted.

In Chapter 3, the scaling issues have been analyzed through 2D simulations. The variation in the on current (I_{on}), off current (I_{off}), threshold voltage (V_t), transconductance (g_m), drain induced barrier lowering (DIBL), subthreshold slope (S), and the gate leakage ($I_{g,leak}$) have been investigated.

Chapter 4 discusses the details of the FinFET device optimization for gate length of 15 nm.

In chapter 5, the operation of a conventional 6T SRAM cell has been explained along with a description of the read stability and write ability criteria. The simulation results based on the SNM metrics and n-curve analysis have been presented for SRAM cells designed using DG FinFETs considering variation in V_{dd} and the work function of the access transistors.

In chapter 6, conclusions are drawn on the basis of this work.

Chapter 2

FinFET Basics and Simulation Methodology

Among the various types of multi - gate structures, FinFETs have been shown to be the most attractive alternative to the bulk MOSFETs as it's fabrication is compatible with the current CMOS fabrication technology.

2.1 FinFET Structure

In a FinFET device, the channel is in the form of a thin vertical silicon structure referred to as the fin (as it resembles the tail fin of a fish). It is called a quasi-planar device because of this vertical fin, even though the current conduction is parallel to the plane of the silicon wafer.

FinFETs come in two flavors : double gate and triple gate. In triple gate FinFETs the gate wraps around the fin from the top as well as from the side walls and the gate insulator thickness on the three sides are similar, while in the double gate FinFETs, either the top insulator layer is made much thicker than the vertical insulator layers or a top gate is avoided altogether. In this work, only double gate FinFETs have been considered.

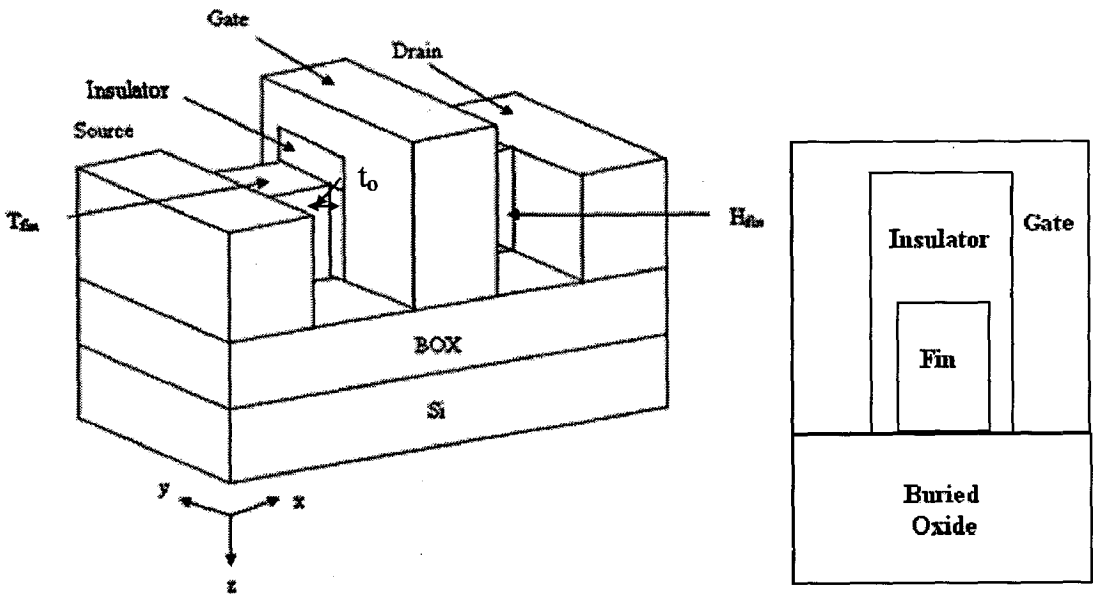

Figure 2.1: (a) 3D structure of a FinFET (b) Cross-sectional view of the gate region

The three dimensional structure and the 2-D cut-plane (y–z plane) view of the gate region of a typical double gate FinFET have been shown in figure 1. The fin height and fin thickness have been denoted by H_{fin} and T_{fin} respectively. The oxide thickness between the side gates and the fin is t_{ox}. Fin engineering (balancing fin height, fin thickness, oxide thickness, and channel length) is crucial in minimizing the leakage currents, I_{off}, and maximizing the on current, I_{on}.

For a double gate FinFET the effective channel width is dependent on the fin height, given as $W_{fin} = 2H_{fin}$. This is because the gate controls the channel from two sides each having width H_{fin} (Note: For a triple gate FinFET, the expression becomes $W_{fin} = 2H_{fin}+T_{fin}$ since now we have additional gate control from the top).

2.2 Doping Densities

The fin is generally lightly doped (or even undoped). Source/Drain regions are heavily doped, while the Source/Drain Extension regions have been subjected to different doping levels by different researchers – from undoped to constantly doped to Gaussian doped.

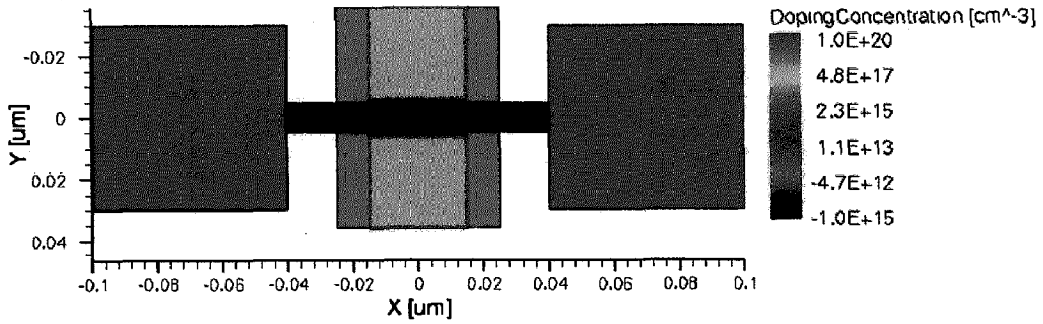

Figure 2.2: 2D FinFET structure with constant doping in the fin

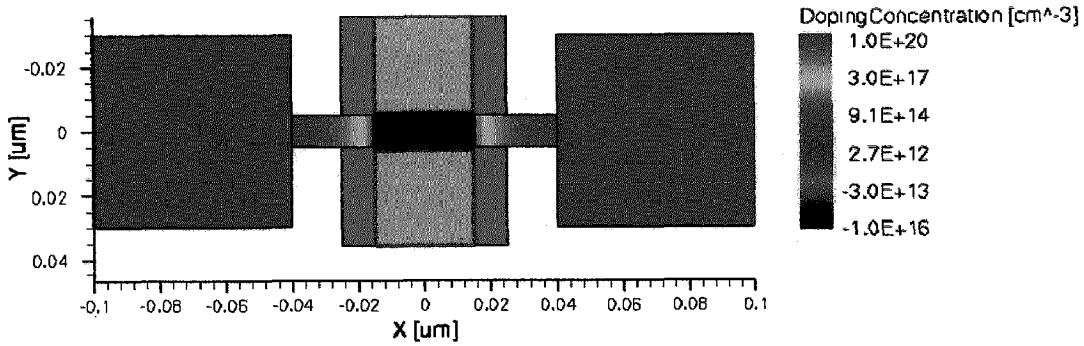

Figure 2.3: FinFET structure with Gaussian doping in the underlap region

2.3 FinFET Fabrication

FinFETs have been fabricated by mainly two different techniques:

Gate-First Approach: In this process, the source and drain regions are created after the formation (patterning) of the gate stack [4].

Gate-Last Approach: Here the source and drain regions are formed before the formation of the gate stack [5, 6].

The fabrication of the FinFET begins with the patterning and etching of a thin fin on an SOI substrate using a hard mask which is retained throughout the fabrication process. The fin thickness is smaller than the gate length, and hence either electron-beam lithography or optical lithography with extensive linewidth trimming is used to pattern the thin fin.

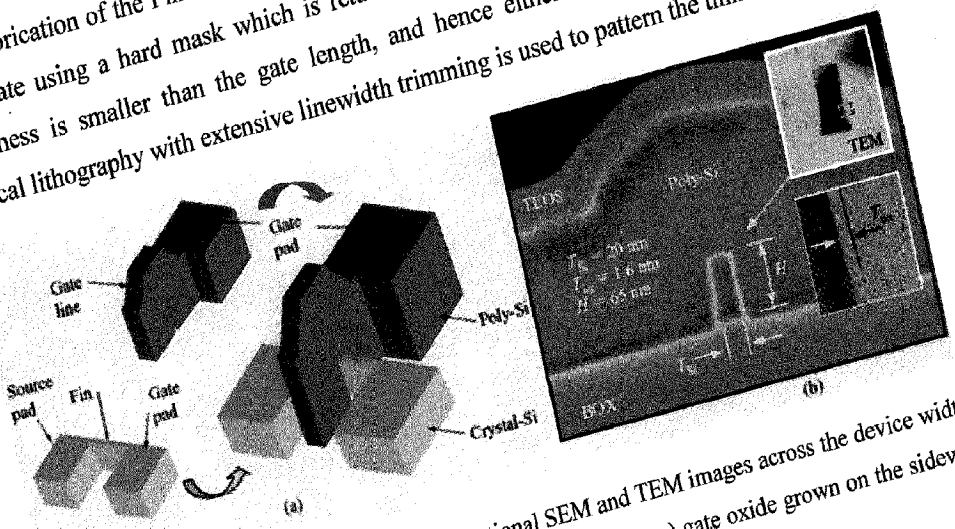

Figure 2.4: (a) Gate-First Process (b) Cross-sectional SEM and TEM images across the device width, illustrating the fin cross-sectional dimensions and the thin (1.6-nm) gate oxide grown on the sidewall of the fin. [7]

For the gate-first process, the fabrication steps after the fin formation are similar to the fabrication steps of the conventional bulk MOSFET. After the gate oxide is grown, the gate polysilicon is deposited, patterned, and etched. A sidewall spacer is formed next to the gate. Source/drain and extension implants can be performed before and/or after the gate spacer, using angled implants.

For the gate-last process, the source and drain regions are formed immediately after patterning the patterning. Doped polysilicon or polycrystalline SiGe is deposited on the fin, followed by lithographic patterning of the source/drain pads with a thin slot between the

source and drain. This distance between the source and drain determines the gate length. The slot length is further reduced by a dielectric sidewall spacer. Then the gate oxide is grown, and the gate material is deposited and patterned.

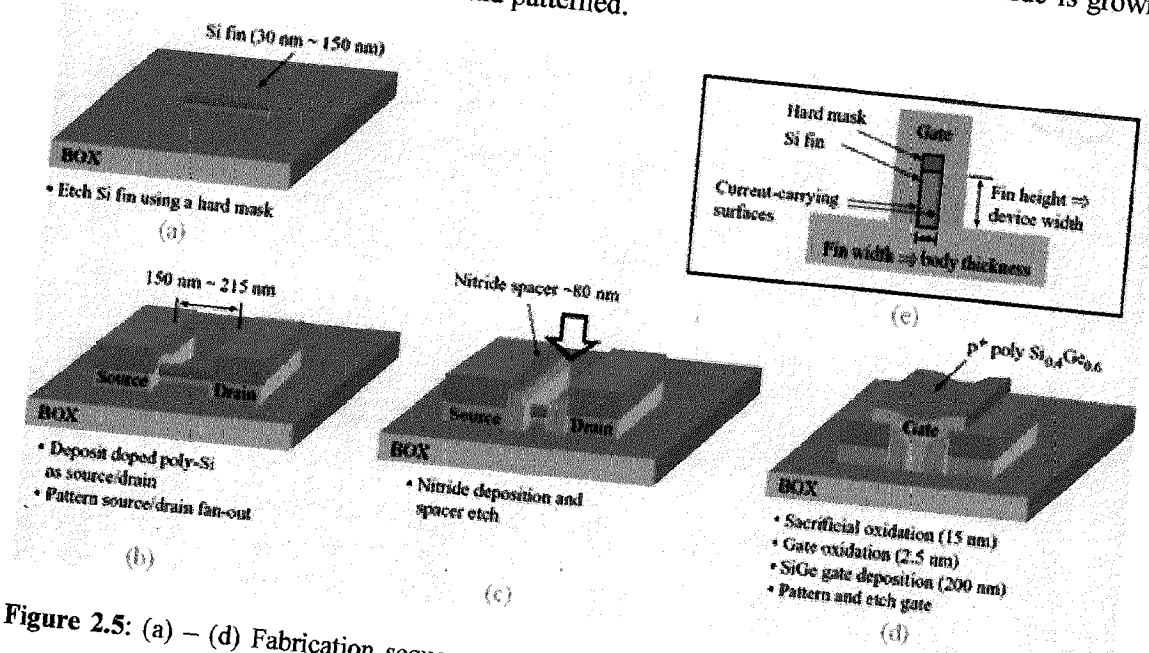

Figure 2.5: (a) – (d) Fabrication sequence of a Gate-Last double gate FinFET process. (e) Cross section of the silicon fin showing the current-carrying plane. Direction of current flow is into the plane of the diagram [7]

The gate-last process enables more flexibility in cases where metal-gate and high $-\kappa$ dielectrics are used.

2. 4 Simulation Methodology

2.4.1 TCAD Device Simulations

Technology CAD (TCAD) refers to using computer simulations to develop and optimize semiconductor devices and processing technologies. TCAD simulation tools solve fundamental physical partial differential equations, such as transport equations for discretized geometries, representing the silicon wafer or the layer system in a semiconductor device. This deep physical approach gives TCAD simulation predictive accuracy. It is, therefore, possible to substitute TCAD computer simulations for costly and time-consuming test wafer runs when developing and characterizing a new semiconductor device or technology.

Device simulations can be thought of as virtual measurements of the electrical behavior of a semiconductor device. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration. For each node, the carrier concentration, current densities, electric field, generation and recombination rates, and so on can be computed.

Electrodes are represented as areas on which boundary conditions, such as applied voltages, are imposed. The device simulator solves the Poisson equation and the carrier continuity equation (and other suitable equations). After solving these equations, the resulting electrical currents at the contacts can be extracted.

2.4.2 Sentaurus TCAD Package from Synopsys

The following tools from the Sentaurus package from Synopsys were used in this work:

Sentaurus Structure Editor

The device structures were created using this editor. The doping levels can be set and the meshing of the structure can also be done. It has a GUI as well as a command line interface. The input files for this editor are written in the scheme programming language.

Sentaurus Device

Sentaurus Device can simulate the electrical, thermal, and optical characteristics of semiconductor devices. It contains a comprehensive set of physical models that can be applied to all relevant semiconductor devices and operation conditions. A real semiconductor device, such as a transistor, is represented in the simulator as a 'virtual' device whose physical properties are discretized onto a non-uniform 'grid' (or 'mesh') of nodes. Continuous properties such as doping profiles are represented on a sparse mesh and, therefore, are only defined at a finite number of discrete points in space. The doping at any point between nodes (or any physical quantity calculated by Sentaurus Device) can be obtained by interpolation.

Each virtual device structure is described in the Synopsys TCAD tool suite by a *tdr* file containing the following information:

- The grid (or geometry) of the device contains a description of the various regions, that is, boundaries, material types, and the locations of any electrical contacts. It also contains the locations of all the discrete nodes and their connectivity.
- The data fields contain the properties of the device, such as the doping profiles, in the form of data associated with the discrete nodes. By default, a device simulated in 2D is assumed to have a 'thickness' in the third dimension of 1 μm.

For maximum efficiency of a simulation, a mesh must be created with a minimum number of vertices to achieve the required level of accuracy. For any given device structure, the optimal mesh varies depending on the type of simulation

Tool Flow

In a typical device simulation tool flow, the Sentaurus Structure Editor generates a *tdr* file, which is then used in the Sentaurus Device along with other input files viz. command file (*.cmd*) and a parameter file to simulate the electrical characteristics of the device. The parameter file(*.par*) is used for changing the default values. The *tdr* file can be generated using the Sentaurus Structure Editor alone or it can also be created in an alternate manner: the generation of a device structure by process simulation (using Sentaurus Process), followed by re-meshing using Sentaurus Structure Editor. In this scheme, control of mesh refinement is handled automatically through the command file.

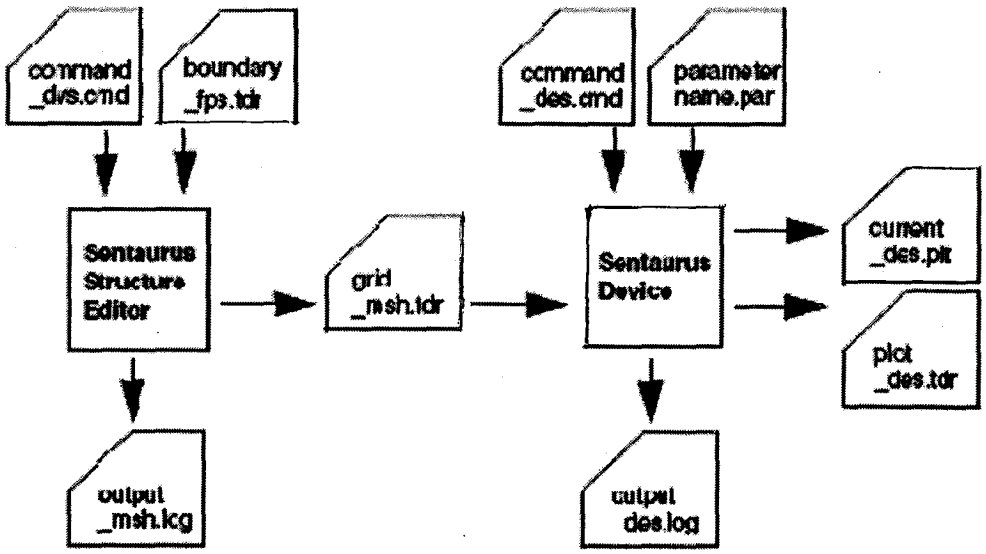

Figure 2.6: Typical tool flow for device simulation using Sentaurus Device [8]

The log files contain step-by-step information of the commands executed.

Tecplot: This tool is used for visualization purposes. It can plot solutions and derived variables like potential, carrier density, mobility, electrical field, etc.

Inspect: Inspect is a plotting and analysis tool. It is be used to extract various device parameters from the data generated by simulations by executing script files. It has a library of functions which can be used to perform mathematical operations on the data.

2.4.3 A typical FinFET device used in the simulations

Two dimensional simulations were performed on the FinFET device, a typical one being shown in figure 2.7. This diagram depicts a view from the top of the device. The various regions and geometrical parameters have been marked on the figure. T_{fin} is the fin thickness, L_g is the gate length, Lspacer and Lextn are the width of the spacer along the channel and total underlap length (including the spacer) respectively, while T_{gate} is the gate thickness.

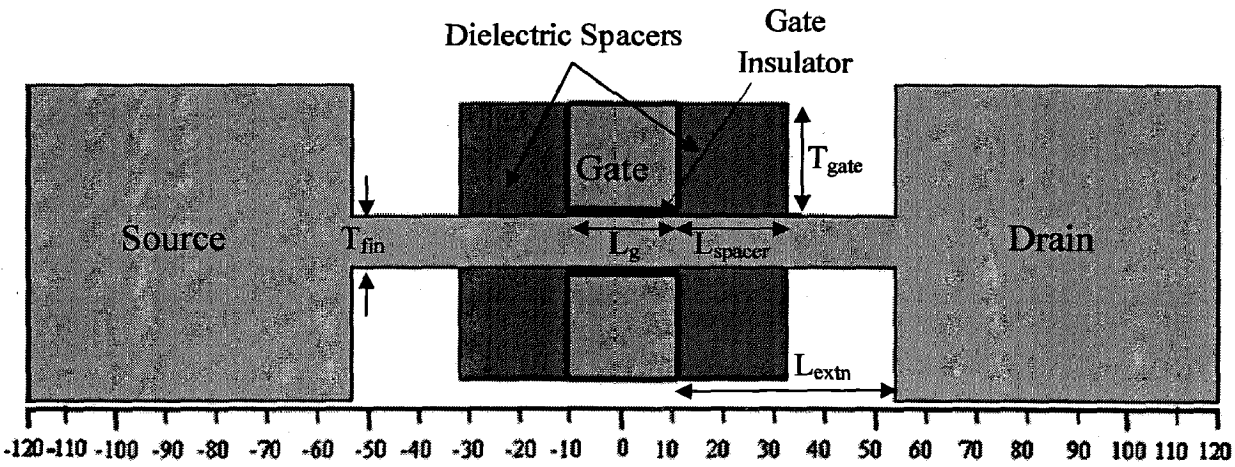

Figure 2.7: A typical 2D FinFET structure used in the Sentaurus simulations
(The dimensions shown are in nm)

2.5 Details of physical models used

This section describes the various physical models used in the simulations.

2.5.1 Band Gap Narrowing Model

The energy bandgap and the intrinsic carrier concentration are very important characteristics of a semiconductor material. At high impurity concentrations the density of energy states no longer has a parabolic energy distribution and becomes dependent on the impurity

concentration and it has been found experimentally that the bandgap is effectively reduced with increasing doping densities [9].

$$E_{g,eff}(T) = Eg(T) - E_{bgn},$$

where E_{bgn} is the amount of band gap narrowing.

The Old Slotboom model was used [8], which gives the amount of band –gap narrowing as:

$$E_{bgn} = E_{ref}\left[\ln\left(\frac{N}{N_{ref}}\right) + \sqrt{\left(\ln\left(\frac{N}{N_{ref}}\right)\right)^2 + 0.5}\right]$$

with $E_{ref} = 9\text{x}10^{-3}$ and $N_{ref} = 1\text{x}10^{17}$.

As a result of band-gap narrowing, the effective intrinsic carrier concentration also changes

$$n_i^{\,2}(N,T) = n_{i0}^{\,2}(T)\exp(E_{g,eff}(N,T)/kT)$$

2.5.2 Mobility Models

The following mobility models were included in the simulation:

(a) The constant mobility model: It is the default model in Sentaurus Device. It accounts only for phonon scattering and, therefore, it is dependent only on the lattice temperature:

$$\mu_{const} = \mu_L\left(\frac{T}{300K}\right)^{-\zeta}$$

the following table lists the values of the coefficients μ_L and ζ.

Table 2.1: Constant Mobility Model: Default coefficients for Si

Parameter	Electrons	Holes
μ_L	1417 cm^2/Vs	470.5 cm^2/Vs
ζ	2.5	2.2

(b) Doping Dependent Mobility Model: In doped semiconductors, the charged impurity ions cause scattering of the carriers, leading to degradation of the carrier mobility. In this work, the Masetti model [10] was used

$$\mu_{dop} = \mu_{\min 1} \exp\left(-\frac{Pc}{N}\right) + \frac{\mu_{const} - \mu_{\min 2}}{1+\left(N_{tot}/C_r\right)^{\alpha}} - \frac{\mu_1}{1+\left(C_S/N_{tot}\right)^{\beta}}$$

The reference motilities $\mu_{\min 1}$, $\mu_{\min 2}$, μ_1 and μ_{const}, the reference doping concentrations C_r and C_S and , and the exponents α and β are available in [8]

(c) High Field Saturation Mobility model

Since the FinFET dimensions are sub –100nm, the electric fields in the channel can be pretty high. In high electric fields, the carrier drift velocity gets saturated. The Extended Canali model based on [11] was used for accounting for this effect in the device simulations.

$$\mu(F) = \frac{(\alpha+1)\mu_{low}}{\alpha + \left[\left(\frac{(\alpha+1)\mu_{low}F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}}$$

where μ_{low} denotes the low-field mobility, v_{sat} the saturation velocity and β is a temperature dependent exponent, given by $\beta = \beta_0\left(\frac{T}{300K}\right)^{\beta_{exp}}$ and $F_{hfs} = |\nabla\Phi|$, is the electric field strength.

(d) Mobility degradation at interfaces

High perpendicular electric fields in the channel region causes strong interaction of carriers at the silicon–insulator interface. Carriers are subjected to scattering by acoustic surface phonons and surface roughness. The Lombardi model [12] was used to include the degradation of carrier mobility at the interfaces.

The surface contribution due to acoustic phonon scattering has the form:

$$\mu_{ac} = \frac{B}{F_{\perp}} + \frac{C\left(N_{tot}/N_0\right)^{\lambda}}{F_{\perp}^{1/3}\left(T/300K\right)^{k}}$$

and the contribution attributed to surface roughness scattering is given by:

$$\mu_{sr} = \left(\frac{\left(F_{\perp} / F_{ref}\right)^{A^*}}{\delta} + \frac{F_{\perp}^{3}}{\eta} \right)^{-1}$$

The values for the various coefficients are available in [8]

The net mobility is given by the combination of the mobility models described above, according to the well known Mathiessen's rule: $\mu^{-1} = \mu_1^{-1} + \mu_2^{-1} + \mu_3^{-1} + ...$

2.5.3 Recombination Model

Electron-hole recombination is an important mechanism by which carrier concentrations tend to approach their equilibrium values. Phonon emission can occur during this recombination process in the presence of a trap (or defect) within the forbidden gap of the semiconductor. The doping dependent model of Shockley–Read–Hall (SRH) recombination was used to consider recombinations through deep defect levels in the band gap. In Sentaurus Device, the following form is implemented:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^{2}}{\tau_p (n + n_1) + \tau_n (p + p_1)}$$

where, n and p are the electron and hole concentrations at the site, and

$$n_1 = n_{i,eff} \exp\left(E_{trap} / kT\right),$$

$$p_1 = p_{i,eff} \exp\left(-E_{trap} / kT\right)$$

where is E_{trap} the difference between the defect level and intrinsic level. The variable is accessible in the parameter file (.par file). It's default value for silicon is 0. $n_{i,eff}$ is the effective intrinsic electron concentration. τ_p and τ_n are the minority carrier lifetimes and are dependent on the doping, electric field and temperature. The doping dependence of the SRH lifetime τ_{dop} is modeled in Sentaurus Device with the Scharfetter relation, written below. Table 2.2 lists the default parameters.

$$\tau_{dop}\left(N_{A,0}+N_{D,0}\right)=\tau_{\min}+\frac{\tau_{\max}-\tau_{\min}}{\left(1+\frac{N_{A,0}+N_{D,0}}{N_{ref}}\right)^{\gamma}}$$

Table 2.2: Default parameters for the doping dependent SRH lifetimes

Parameter	Electrons	Holes	Unit
$\tau_{\min}$	0	0	s
$\tau_{\max}$	$1x10^{-5}$	$3x10^{-6}$	s
N_{ref}	$1x10^{16}$	$1x10^{16}$	cm^{-3}
γ	1	1	1
E_{trap}	0	0	eV

Since the simulations performed included quantum transport models to account for the quantum mechanical effects, the expression for R_{net}^{SRH} needs to be modified as follows

$$R_{net}^{SRH}=\frac{np-\gamma_n\gamma_p n_{i,eff}^{2}}{\tau_p(n+\gamma_n n_1)+\tau_n(p+\gamma_p p_1)}$$

where

$$\gamma_n=\frac{n}{N_C}\exp(-\eta_n),\ \gamma_p=\frac{p}{N_C}\exp(-\eta_p)$$

$$\eta_n=\frac{E_{F,n}-E_C}{kT},\ \eta_p=\frac{E_V-E_{F,p}}{kT}$$

2.5.4 Tunneling Models

In the nanoscale FinFETs, different tunneling mechanisms occur and contribute to the leakage currents. Direct tunneling at the gate dielectric/silicon interface and BTBT has been included in the simulations.

(a) Band to Band Tunneling (BTBT): The Schenk model [13] was used. Phonon-assisted band-to-band tunneling cannot be neglected in high normal electric fields of MOS structures.

It must be taken into consideration if the field, in some regions of the device, exceeds $8x10^5$ V/cm (approximately).

BTBT is modeled according to the expression [8]

$$R_{net}^{bb} = AF^{7/2}\frac{\tilde{n}\tilde{p} - n_{i,eff}^{\ 2}}{(\tilde{n}+n_{i,eff})(\tilde{p}+n_{i,eff})}\left[\frac{(F_C^{\mp})\exp\left(-\frac{F_C^{\mp}}{F}\right)}{\exp\left(\frac{\hbar\omega}{kT}\right)-1}+\frac{(F_C^{\pm})\exp\left(-\frac{F_C^{\pm}}{F}\right)}{1-\exp\left(-\frac{\hbar\omega}{kT}\right)}\right]$$

There is an option for including local density correction. If no density correction is made, then where $\tilde{n}$ and $\tilde{p}$ are equal to n and p respectively, while the following equation has to be used for using modified electron densities.

$$\tilde{n} = n\left(\frac{n_{i,eff}}{N_C}\right)^{\frac{\gamma_n|\nabla E_{F,n}|}{F}}$$

A similar expression exists for holes.

(b) Direct Tunneling:

Scaling of the SiO_2 layer thickness below 3 nm results in heavy direct quantum mechanical tunneling of electrons from the channel to the gate across the gate dielectric through a trapezoidal energy barrier. It turns into Fowler–Nordheim tunneling at oxide fields higher than approximately 6 MV/cm. The model used in Sentaurus also includes the option to consider the reduction in tunneling barrier height due to the Image Force Effect.

Direct tunneling can take place in a MOS structure in the following three ways [14]:

ECB - Electron Conduction Band tunneling,
EVB - Electron Valence Band tunneling, and
HVB - Hole Valence Band tunneling.

Figure 2.8 shows these tunneling mechanisms in a double gate structure.

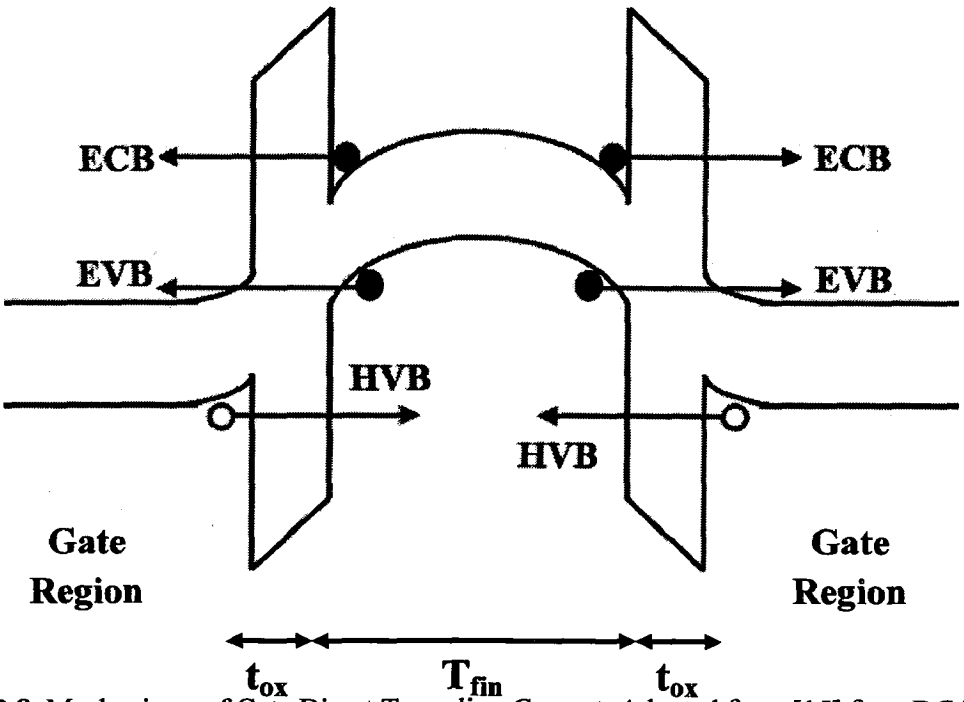

Figure 2.8: Mechanisms of Gate Direct Tunneling Current. Adapted from [15] for a DG FinFET device

The direct tunneling current density for electrons is given by [14]:

$$j_n = \frac{qm_c{}^* k_B T}{2\pi^2 h^3}\int_0^\infty dE\Gamma(E)x\ln\left\{\frac{\exp\left[\frac{E_{F,S}(d)-E_C(d)-E}{k_B T}\right]+1}{\exp\left[\frac{E_{F,M}(d)-E_C(d)-E}{k_B T}\right]+1}\right\}$$

where q is the elementary charge, m_c^* is the conductivity mass, k_B *is* the Boltzmann constant, $E_{F,S}(d)$ is the substrate Fermi energy at the Si/SiO_2 interface, $E_{F,M}(0)$ is the gate Fermi energy, $E_c(d)$ is the conduction band energy at the Si/SiO_2 interface, E is energy, T *is* temperature and $\Gamma(E)$ is the transmission coefficient.

The insulator barrier is approximated by a trapezoidal barrier (assuming absence of fixed charges), with a parabolic E-k relation in the barrier region

Image Force Effect: The image force effect is included in the Direct Tunneling model by taking $E_B(E)$ as an energy-dependent pseudobarrier:

$$E_B(E)=E_B(E_0)+\frac{E_B(E_2)-E_B(E_0)}{(E_2-E_0)(E_1-E_2)}(E-E_0)(E_1-E)-\frac{E_B(E_1)-E_B(E_0)}{(E_1-E_0)(E_1-E_2)}(E-E_0)(E_2-E)$$

where E_0, E_1 *and* E_2 are chosen in the lower energy range of the barrier potential (between 0 and 1.5 eV in most practical cases).

2.5.5. Transport Model

The Density Gradient transport model was used for the device simulations. This model advanced by Ancona [16] and his coworkers is an approximate approach to the quantum mechanical correction of the macroscopic electron transport equation. In this approach, an extra term is introduced in the carrier flux by making the equation of state for the electron gas density gradient dependent.

DD equation for electrons: $\frac{\partial n}{\partial t} = \frac{\nabla \bullet J_n}{q} = \nabla \bullet \left(-n\mu_n \nabla \psi_n + D_n \nabla n\right)$

Correction: $\psi_n \rightarrow \psi_n + \psi_{qn}, \psi_{qn} = 2b_n \left(\frac{\nabla^2 \sqrt{n}}{\sqrt{n}}\right); b_n = \frac{\hbar^2}{4 r_n m_n q}$

Here r_n is a fitting parameter generally taken to be equal to 3.

Quantum-corrected current density: $J_n = -qn\mu_n \nabla \psi_n + qD_n \nabla n - qn\mu_n \nabla \left(2b_n \frac{\nabla^2 \sqrt{n}}{\sqrt{n}}\right)$

2.6 Parameter Extraction

The various device parameters were extracted from the simulated FinFET characteristics using the "Inspect" tool. Scripts were written using the functions available in the inspect library to perform operations on the I-V data. Here is a description of the extraction methodologies and parameter definitions used.

2.6.1 I_{on} Extraction: The on-current is defined as $I_{DS}(V_{DS}=V_{GS}=V_{DD})$.

2.6.2 I_{off} Extraction : The off current i.e. the subthreshold leakage current ($I_{DS,sat}$) is defined as $I_{DS}(V_{DS}= V_{DD}, V_{GS}=0)$

2.6.3 Threshold Voltage Extraction: The threshold voltage (V_t) is a fundamental parameter in MOSFET design and modeling. Many different definitions and extraction methodologies exist in literature and are in use [17]. In essence, it is interpreted as the gate voltage value at which the transition between weak and strong inversion takes place in the channel of the device. The theoretical definition of V_t for conventional MOS devices is based on the "strong-inversion" condition at which the surface potential is twice of the bulk Fermi

potential ($\phi_S = 2\phi_F$). However, most practical FinFETs have undoped or lightly doped channels. In such cases, $\phi_F \approx 0$ and hence this definition of threshold voltage doesn't have any relevance.

In this work, the threshold voltages have been calculated from the simulated drain current versus gate voltage transfer characteristics in the following two ways:

(a) Extrapolation in the Linear Region (ELR) Method:

In this method (also known as max-g_m method) the the threshold voltage ($V_{t\text{-}gm}$) is taken to be equal to the gate-voltage axis intercept (I_d =0 A) of the linear extrapolation of the I_d–V_{gs} curve at its maximum first derivative point i.e. the point of maximum transconductance, g_m.

(b) Constant-current (CC) method

In the CC method the threshold voltage is evaluated as the value of the gate voltage, V_g, corresponding to a given arbitrary constant drain current, I_d with V_{ds} < 100 mV. The threshold voltage can be determined easily with only one voltage measurement. In this work, the CC threshold voltage of the FinFET has been taken as the value of V_G for which the drain current is given by $I_{D0} = 300\ nA \times W/L_g$, where W is the effective width of the FinFET, which is given by $W = 2T_{fin}$, at low drain bias of 0.05V for extracting the linear threshold voltage [18]. Since the drain current in the 2D simulations is available in units of A/μm, the constant current value is modified as $I_{D0} = (300\ nA \times W/L_g) \times W = 300\ nA/L_g$, the L_g value being in units of μm. For p-finFETs, the current was taken to be $0.4I_{D0}$.

2.6.4 Gate Leakage Extraction

Leakage current in Off State, $I_{g,leak} = I_g(V_G=V_S=0,\ V_{DS}=V_{DD})$ A/μm

Leakage Current Density $J_{g,leak} = (I_{g,leak} * 10^9 / L_g)$ A/cm^2

2.6.5 Subthreshold Slope Extraction

First the drain current I_{crit}, corresponding to the gate voltage equal to $V_{t\text{-}gm}$ is found. If the current level at V_G=0 is less than $I_{crit}/10$, we proceed to find the subthreshold slope, else it implies that there is no well defined subthreshold region.

$$S = \frac{dV_{GS}}{d\log I_D}$$

2.6.6 DIBL Extraction

The threshold voltages were measured at $V_{DS}=V_{DD}$ and VDS=0.05V and then the following expression was used :

$$DIBL = \frac{|V_t(V_{DS}=V_{DD}) - V_t(V_{DS}=0.05V)|}{V_{DD} - 0.05} \text{ mV/V}$$

Chapter 3

Scaling Issues in DG FinFETs

As the device dimensions go on shrinking, the device behavior changes significantly and the devices become increasingly sensitive to process variations. To investigate the the scaling issues in double gate FinFETs, the device dimensions were varied and the results were analyzed. In this section, the primary FinFET used in the simulations had the following characteristics:

Table 3.1: The Primary FinFET Device parameters

Device Parameter	**Value**
Gate Length(L_g)	30 nm
Fin Width (T_{fin})	10 nm
Gate Oxide Thickness(t_{ox})	1 nm
Gate Oxide	SiO_2
Fin Doping	10^{15} cm^{-3}
S/D Doping	10^{22} cm^{-3}
Spacer Material	Si_3N_4
Spacer Thickness	15 nm
Total Underlap Length(L_{extn})	25 nm
Supply Voltage (V_{dd})	1 V

3.1 Gate Length (L_g) Scaling

Gate lengths were varied from 40 nm to 15 nm and the different parameters were extracted to see the effect of scaling. As can be seen from figure 3.1(a), both I_{on} and I_{off} are found to increase with decreasing gate lengths, as they do in case of bulk MOSFETs, because of the increased longitudinal electric field. Subthreshold slope is found to worsen, indicating poorer switch-off behavior. Other effects observed were threshold voltage roll off, degradation of DIBL and improvement in the transconductance.

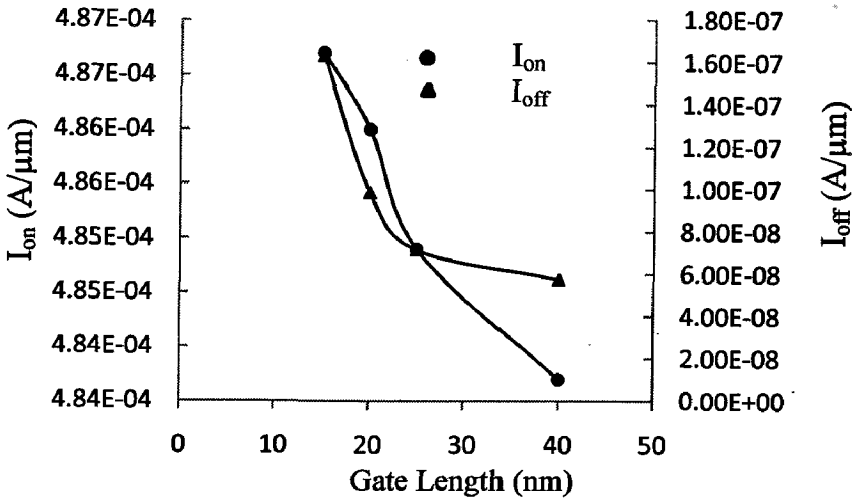

Figure 3.1 (a): Variation of I_{on} and I_{off} with L_g

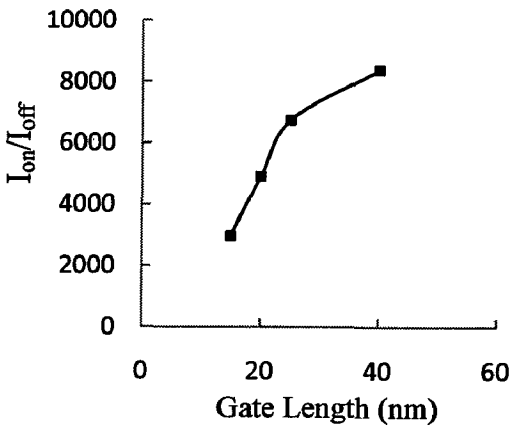

Figure 3.1 (b): Variation of I_{on}/I_{off} with L_g

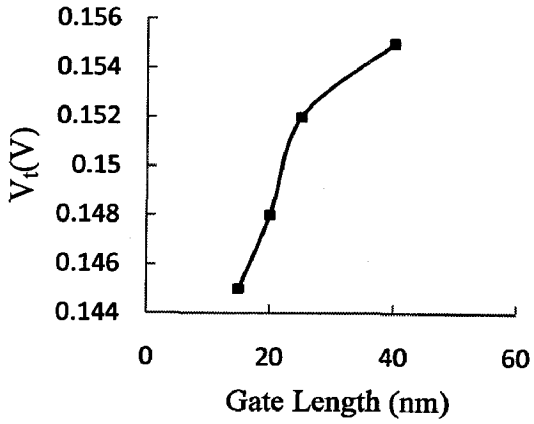

Figure 3.1 (c): Variation of V_t with L_g

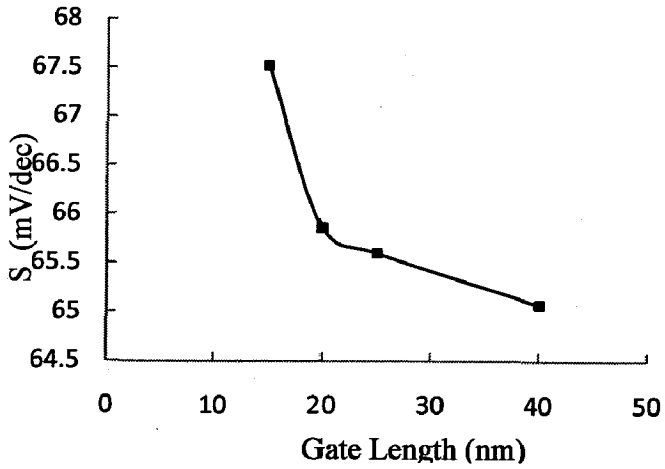

Figure 3.1(d): Variation of S with L_g

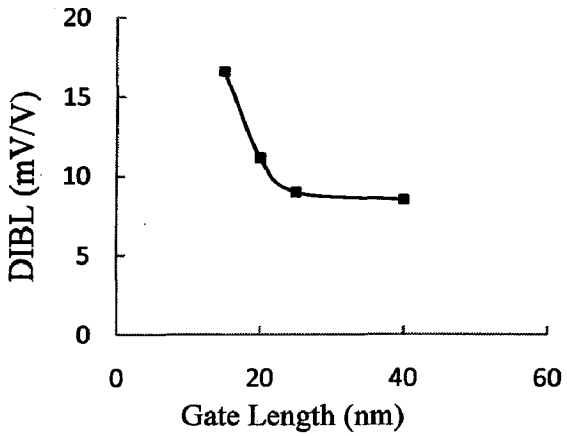

Figure 3.1(e): Variation of DIBL with L_g

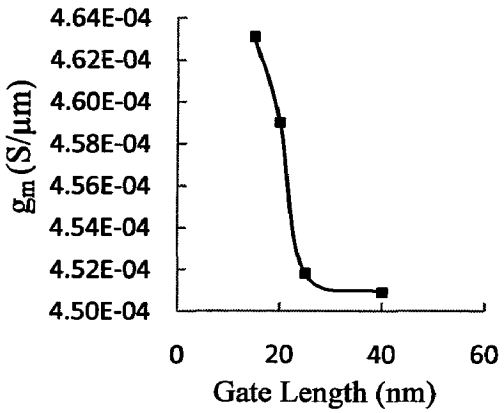

Figure 3.1(f): Variation of g_m with L_g

The threshold voltage (V_t) rolls off as we decrease the gate length because of decrease in the required gate voltage for achieving same level of channel charge.

The DIBL degrades by about 100% on reducing the gate length from 40 nm to 15 nm, because of the increased proximity of the source and drain regions in FinFETs with reduced gate lengths.

3.2 Fin Thickness (T_{fin}) Scaling

An overall performance improvement is observed as far as the short channel effects are concerned. I_{off}, S and DIBL are found to decrease on reducing the fin thickness as can be seen from figures 3.2(a), 3.2(e) and 3.2(f) . The on current reduces (figure (3.2(a))) due to reduction in number of carriers in a thinner fin.

The amount of carrier confinement in the silicon fin depends on the fin thickness. This structural quantum confinement in the potential well causes the minimum energy of electrons in the potential well to rise to non-zero values as the silicon fin becomes thinner. This effectively increases the threshold voltage of the device as carriers must now populate a higher energy subband [19]. The V_t variation is shown in figure 3.2(d).

Thinner T_{fin} leads to reduced gate leakage as can be seen from figure. This can be explained as follows. The net depletion charge in the channel is proportional to T_{fin} and is given by:

$$Q_{Depletion} = q(N_D^+ - N_A^-)T_{fin})$$

Hence as the fin is made thinner, the depletion charge goes on reducing, thereby decreasing the normal electric field from gate to channel. Consequently the gate leakage is reduced, as shown in figure 3.2(g).

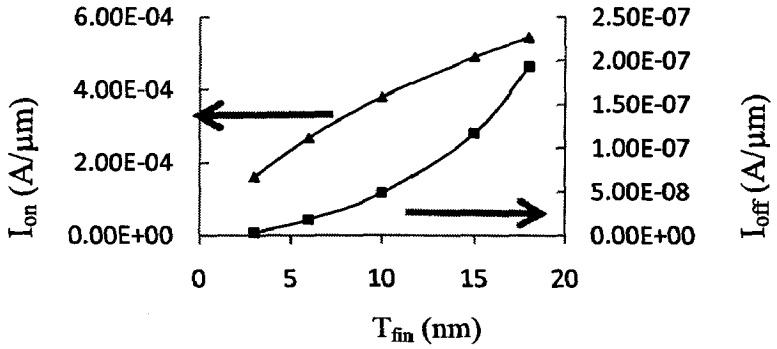

Figure 3.2(a): Variation of I_{on} and I_{off} with T_{fin}

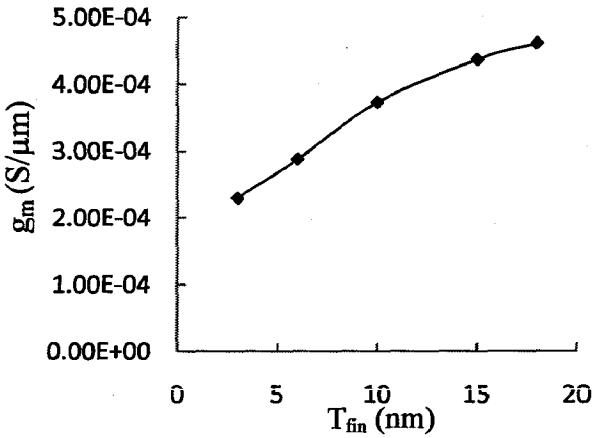

Figure 3.2(b): Variation of g_m with T_{fin}

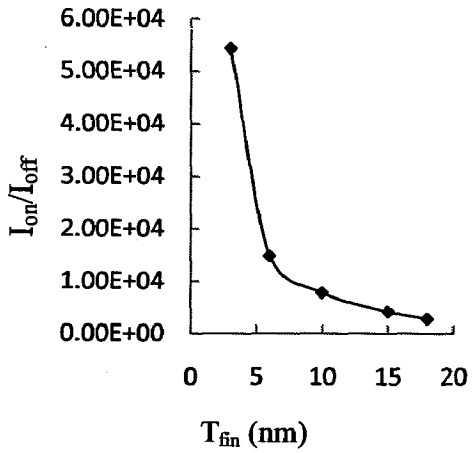

Figure 3.2(c): Variation of I_{on}/I_{off} with T_{fin}

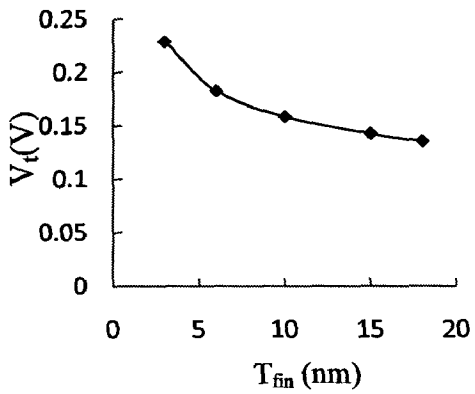

Figure 3.2(d: Variation of V_t with T_{fin}

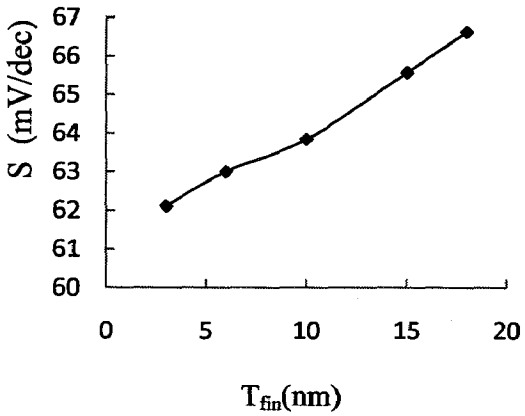

Figure 3.2(e): Variation of S with T_{fin}

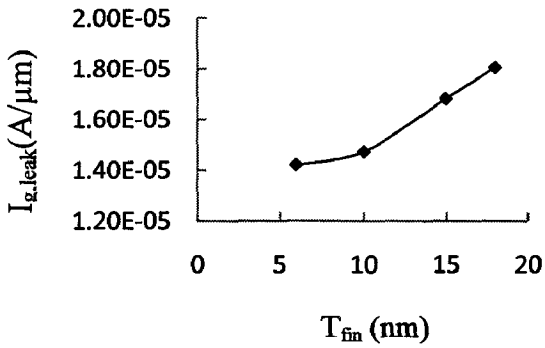

Figure 3.2(f): Variation of $I_{g,leak}$ with T_{fin}

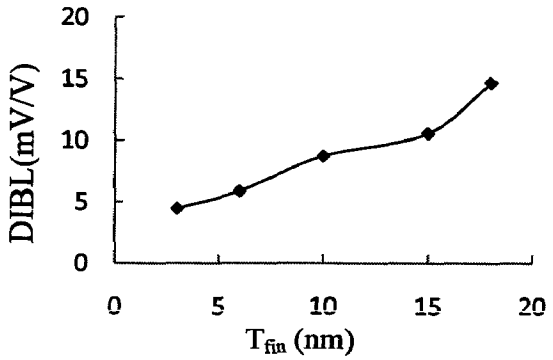

Figure 3.2(g): Variation of $I_{g,leak}$ with T_{fin}

3.3 Gate Oxide Scaling

As we decrease the gate length, the gate oxide thickness also needs to be reduced. In this section the oxide thickness was varied from 1 nm to 2.5 nm and its impact on the FinFET characteristics was studied. The on current, I_{on}/I_{off} ratio and gate transconductance were found to increase with decreasing t_{ox} as depicted in figures 3.3(a)-3.3(c). The subthreshold slope (figure 3.3(d)) and DIBL (figure (3.3(e)) were also found to improve as the oxide layer was made thinner, due to better gate control. But the main concern is the overwhelming increase in the gate leakage. The gate leakage current was found to increase exponentially with decreasing gate oxide thickness (showing a linear variation on the log scale in figure 3.3(f)). This is because of the exponential dependence of the tunneling probability on the oxide thickness, as can be calculated by applying the WKB approximation. The electric field across the SiO_2 layer increases on reducing its thickness, and as a result the tunneling probability increases.

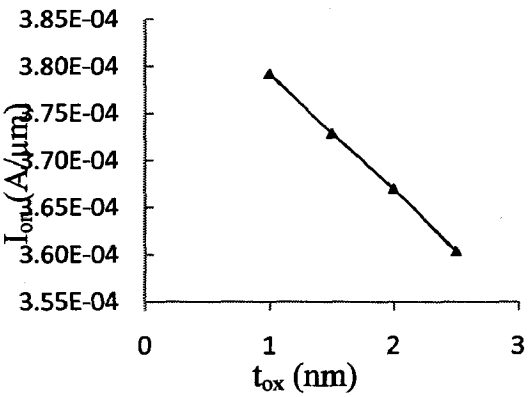

Figure 3.3(a): Variation of I_{on} with t_{ox}

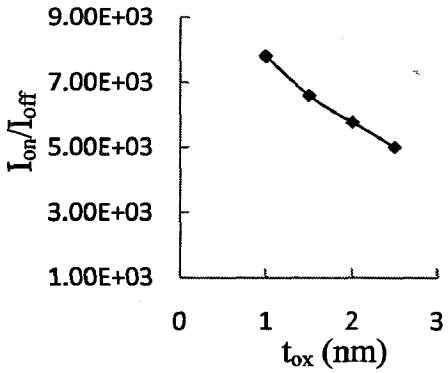

Figure 3.3(b): Variation of I_{on}/I_{off} with t_{ox}

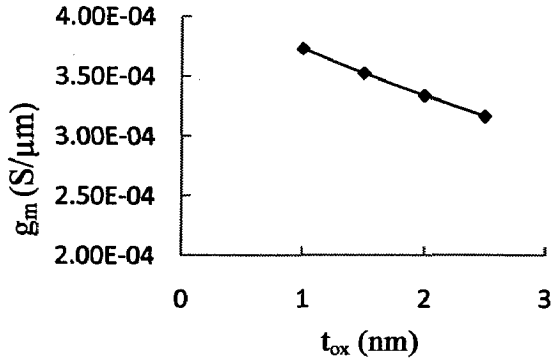

Figure 3.3(c): Variation of g_m with t_{ox}

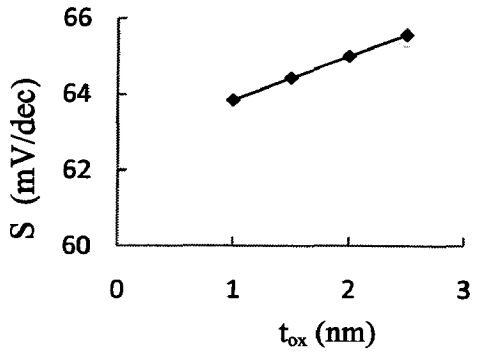

Figure 3.3(d): Variation of S with t_{ox}

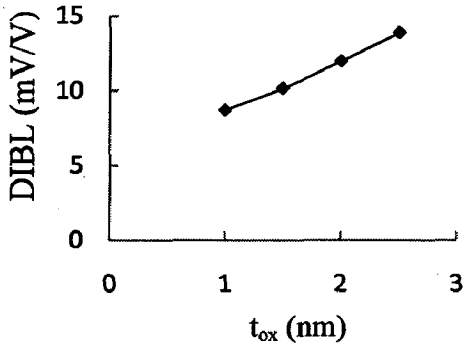

Figure 3.3(e): Variation of DIBL with t_{ox}

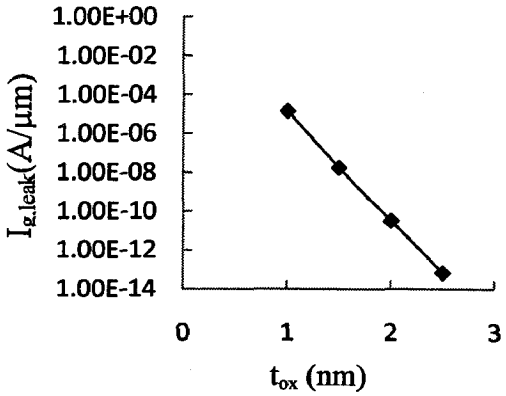

Figure 3.3(f): Variation of $I_{g,leak}$ with tox

Although the results and analysis presented here were for n-FinFETs, the gate leakage trends in p-FinFETs are expected to be similar due to similar reduction in the perpendicular electric field. Of course, the quantitative values will be different due to different carrier effective masses and tunneling barrier heights in the p-FinFETs.

3.4 Impact of Image Force on Gate Leakage

Simulations were carried out with and without the inclusion of the image force effect. The gate leakage is increased when the image force effect is also accounted for. When an electron approaches a dielectric layer, it induces a positive charge on the interface which acts like an image charge within the layer [20]. This effect leads to a reduction of the barrier height for both electrons and holes. The conduction band bends downward and the valence band bends upward, respectively. The reduced barrier results in appreciable increase in current flow across the dielectric and hence, the image force effect can't be neglected while considering gate leakages in FinFETs with ultra thin oxides.

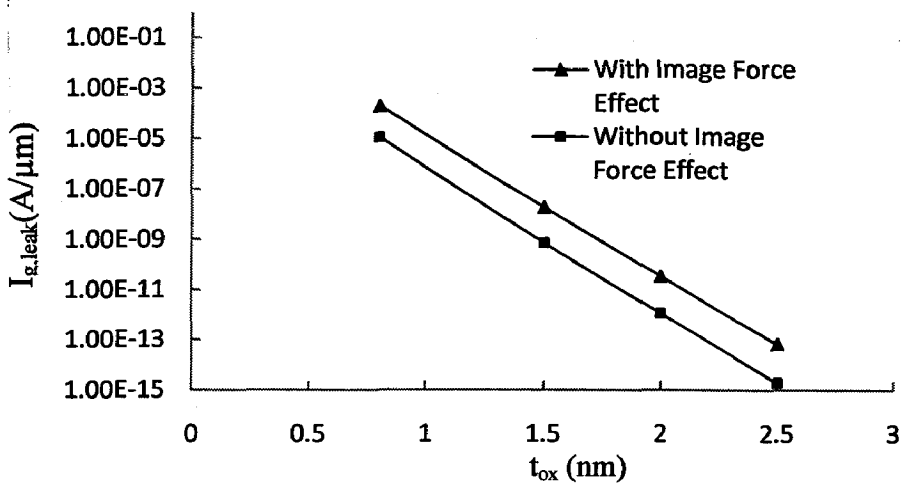

Figure 3.5: Impact of Image Force on Gate Leakage

3.5 Gate Thickness Scaling

The impact of gate thickness is a relatively less explored area. Generally the minimum gate thickness allowed in current technologies is kept at a value equal to the gate length (L_g), but there are some published results [21] that mention fabrication of MOS devices with gates thinner than the gate length used.

The effect of scaling the gate thickness on the characteristics of DG FinFETs was studied using simulations.

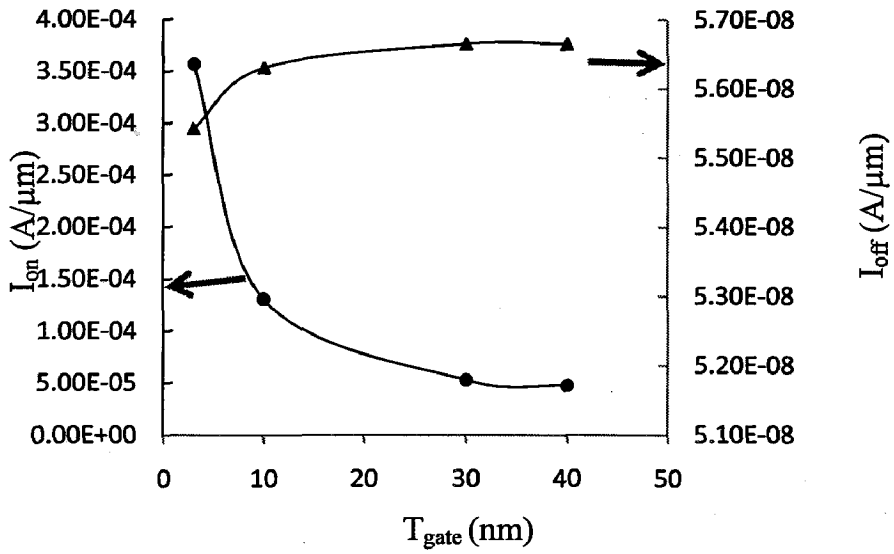

Figure 3.5(a): Variation of I_{on} and I_{off} with T_{gate}

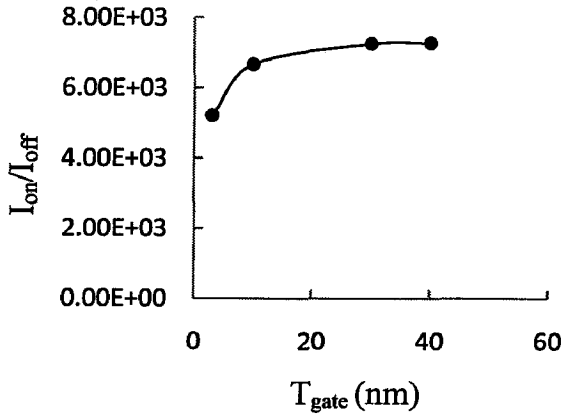

Figure 3.5(b): Variation of I_{on}/I_{off} with T_{gate}

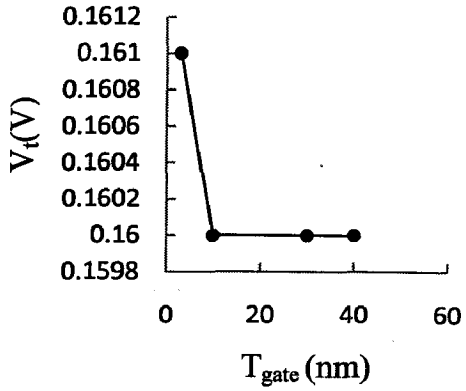

Figure 3.4(c): Variation of V_t with T_{gate}

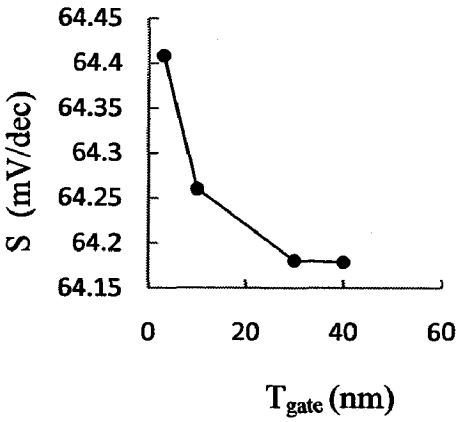

Figure 3.5(d): Variation of S with T_{gate}

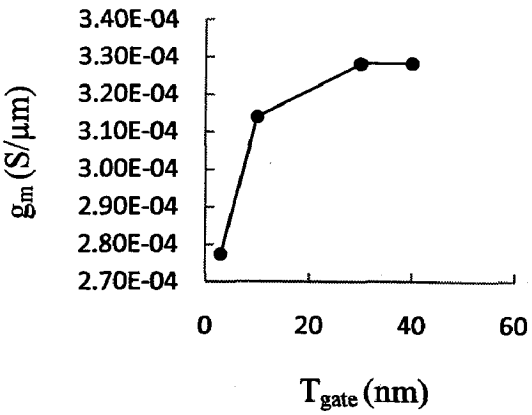

Figure 3.5(e): Variation of g_m with T_{gate}

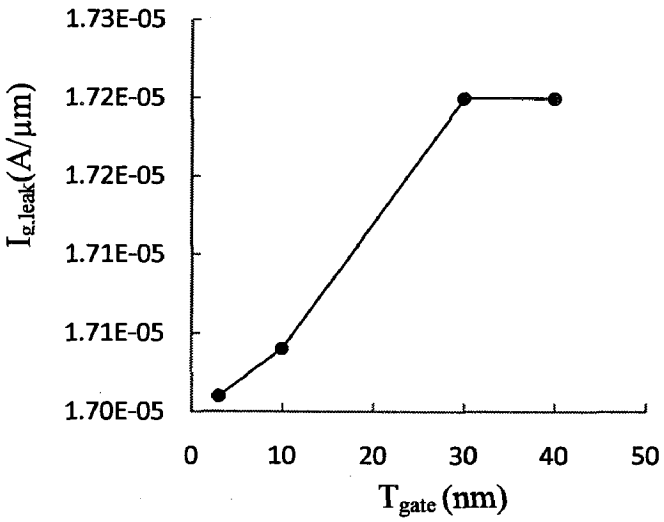

Figure 3.5(f): Variation of $I_{g,leak}$ with T_{gate}

3.5 Effect of Fin Doping Variation

The doping in the fin region (N_{fin}) was varied from $1x10^{15}$ cm^{-3} to $1x10^{18}$ cm^{-3}. The results are shown in figures 3.5(a)-(g). I_{on} , I_{off} and the transconductance were found to decrease, rolling off at a faster pace at higher doping densities. This can be attributed to the

decrease in mobility due to scattering. But still, the I_{on}/I_{off} ratio is improved. Threshold voltage expectedly increases, just as in bulk devices. The subthreshold slope and the DIBL – the two parameters which characterize the SCEs are found to degrade excessively, as can be seen from figures 3.5(e) and 3.5(f).

As the p-type doping is increased, the depletion charge is no longer negligible and hence the vertical electric field increases and consequently the gate tunneling current are seen to rise with increased doping in figure 3.5(g). Also, this leakage degradation will be more severe for devices with thinner fins because then a higher doping concentration will be required for achieving a particular threshold voltage.

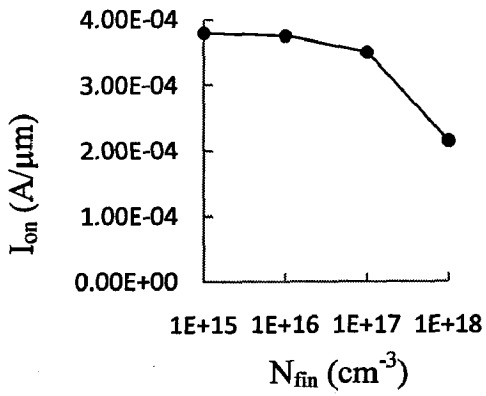

Figure 3.6(a): Variation of I_{on} with N_{fin}

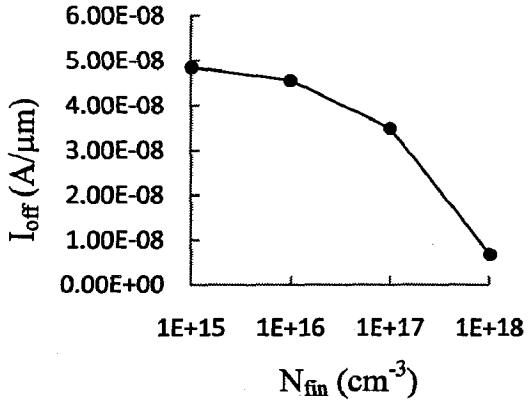

Figure 3.6(b): Variation of I_{off} with N_{fin}

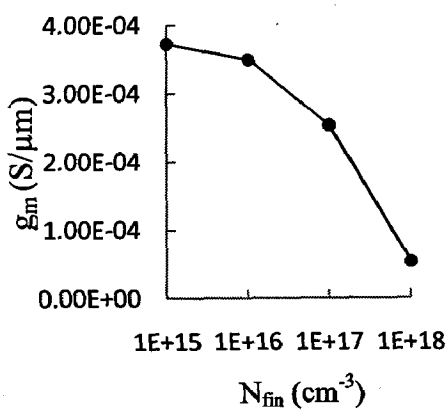

Figure 3.6(c): Variation of g_m with N_{fin}

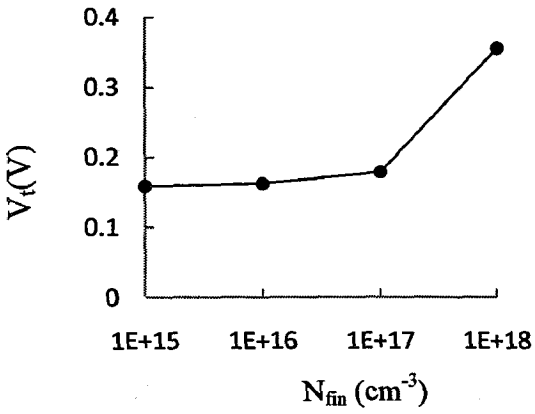

Figure 3.6(d): Variation of V_t with N_{fin}

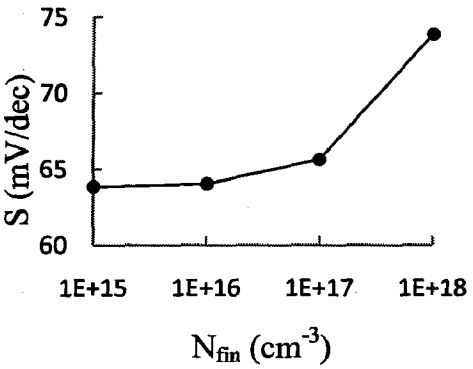

Figure 3.6(e): Variation of S with N_{fin}

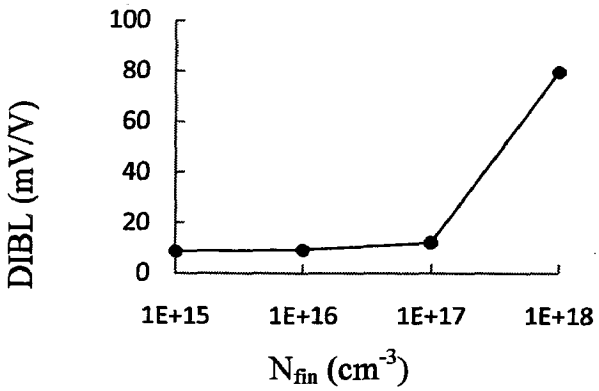

Figure 3.6(f): Variation of DIBL with N_{fin}

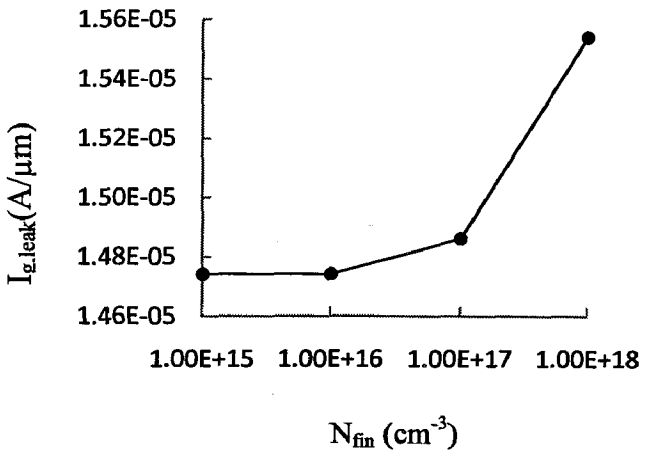

Figure 3.6(g): Variation of $I_{g,leak}$ with N_{fin}

This analysis justifies the use of undoped or lightly doped channels in the ultra thin body devices like FinFETs from the gate leakage point of view, in addition to the RDF (random doping fluctuations) and source to drain tunneling issues.

Chapter 4

Device Optimization for 15 nm Technologies

4.1 Meaning of "15 nm" Technology

Since 2005, ITRS has stopped using the term "technology node" for describing the status of technology with respect to the scaled dimensions. Instead, each distinct scaling feature is specifically referenced as such. Until recently the gate length corresponding to a technology "node" of say "xx nm" was quite smaller than "xx nm" (in fact approximately equal to xx/2). This "xx nm" actually referred to the metal half pitch in DRAM. The reduction from generation to generation of the DRAM half-pitch of metal by 30% (0.7× the previous technology generation) identified a "technology node". But around the 22 nm node and beyond, when we talk of "xx nm" technology, the gate length is close to "xx nm" [22]. So 15 nm technology corresponds to a physical gate length of 15 nm. Figure 4.1 puts these ideas in proper perspective. Here NTRS stands for "National Technology Roadmap for Semiconductors" – the precursor to the ITRS.

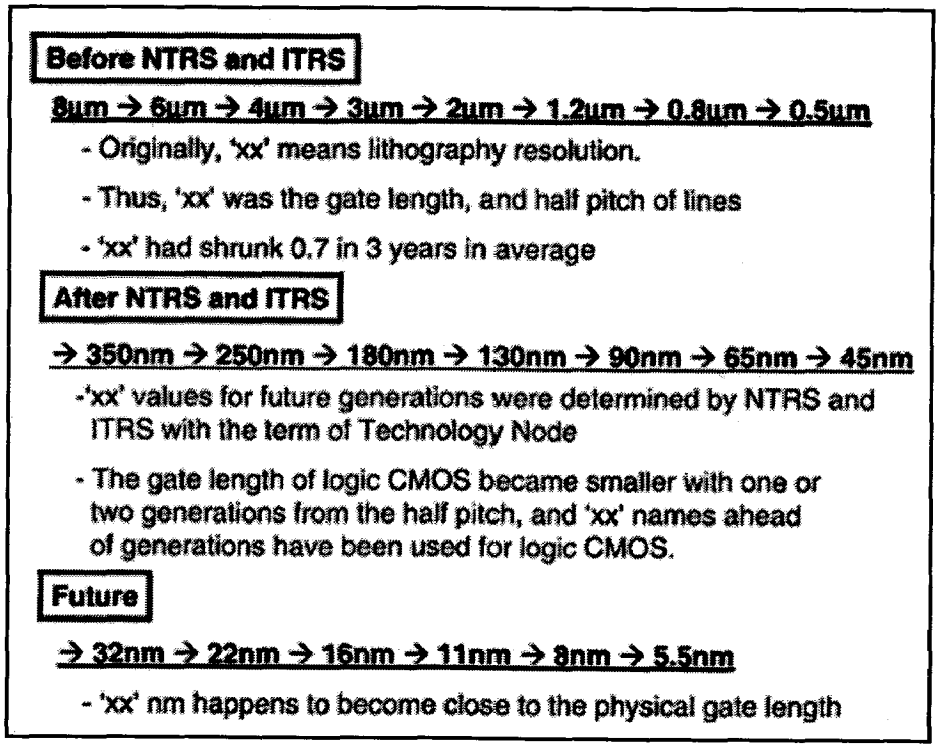

Figure 4.1: Meaning of "xx nm" Technology [22]

4.2 ITRS 2008 update Specifications

Table 4.1 lists the target parameters for the High Performance (HP) double gate devices for the year 2015 according to the ITRS 2008 update. In this work, an attempt has been made to approach these targets by applying suitable device optimization ideas. Optimized doping profile for the source/drain extension region, gate dielectric with a suitable value of κ, work function engineering for the metal gates and spacer engineering were applied on 15 nm gate length DG FinFETs to obtain a device that satisfies the ITRS specifications.

Table 4.1: ITRS Projections for High Performance DG Devices in the year 2015 [23]

Device Parameter	ITRS Projection
L_g: Physical Gate Length	15 nm
EOT: Equivalent Oxide Thickness	0.77 nm
$J_{g,limit}$: Maximum gate leakage current density	1300 A/cm2
V_{dd}: Power Supply Voltage	0.925 V
$V_{t,sat}$: Saturation Threshold Voltage	0.11 V
$I_{d,sat}$: NMOS Drive Current	1.93x 10^{-3} A/μm
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current	0.27 μA/μm

4.3 Source/Drain Extension Doping Engineering

The doping of the source/drain extension region in FinFETs can have profound impact on the device characteristics. Instead of abrupt doping profiles, it has been reported that a gradual doping profile defined by a Gaussian function can improve the device performance [24, 25]. This Gaussian profile needs to be optimized taking into account the length of the underlap region (L_{extn}) between gate edge and the heavily doped source/drain.

Simulations with Gaussian Doping: The device parameters used in this simulation were as follows: L_g =15 nm, T_{fin}=7 nm, EOT = 1 nm, κ_{gate}=7.4, L_{spacer}=L_{extn}=10 nm. Gaussian doping profile with different values of average doping roll

offs, signified by the doping level at the gate edge (N_{edge}) were simulated and the results are shown in figure 4.2(a) –4.2(h).

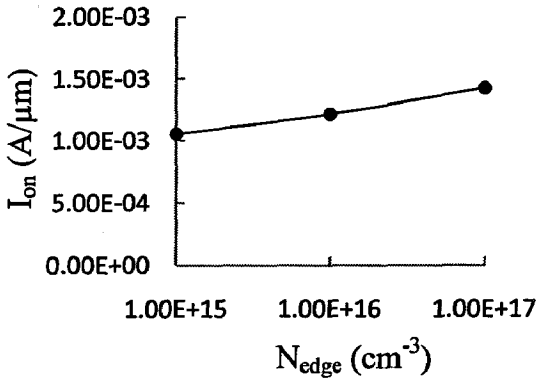

Figure 4.2(a): Variation of I_{on} with N_{edge}

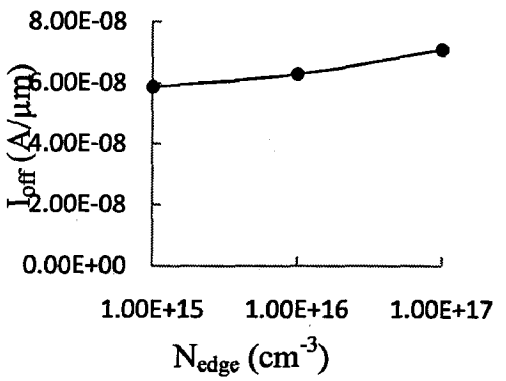

Figure 4.2 (b): Variation of I_{off} with N_{edge}

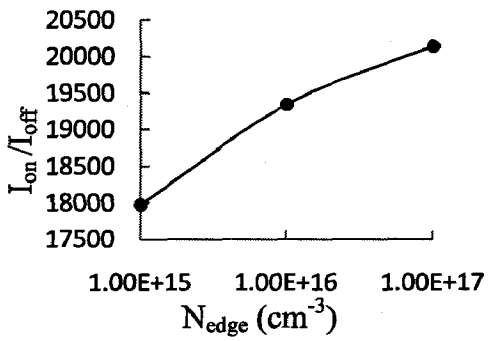

Figure 4.2 (c): Variation of I_{on}/I_{off} with N_{edge}

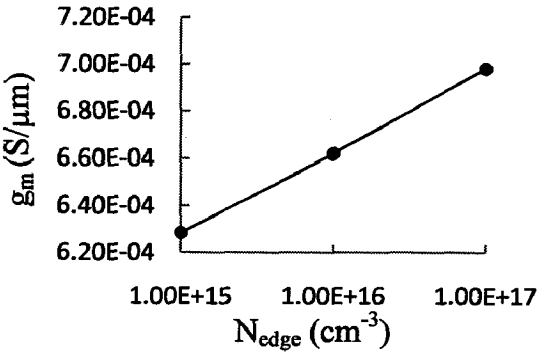

Figure 4.2 (d): Variation of g_m with N_{edge}

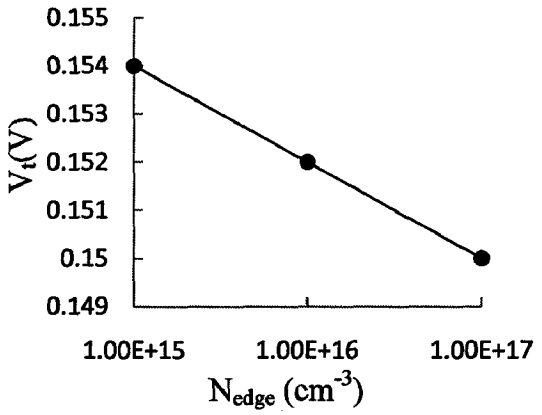

Figure 4.2(e): Variation of V_t with N_{edge}

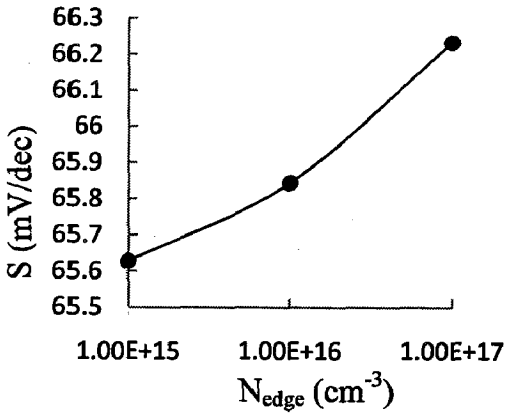

Figure 4.2(f): Variation of S with N_{edge}

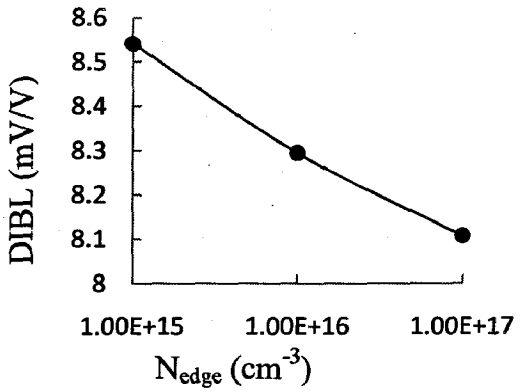

Figure 4.2 (g): Variation of DIBL with N_{edge}

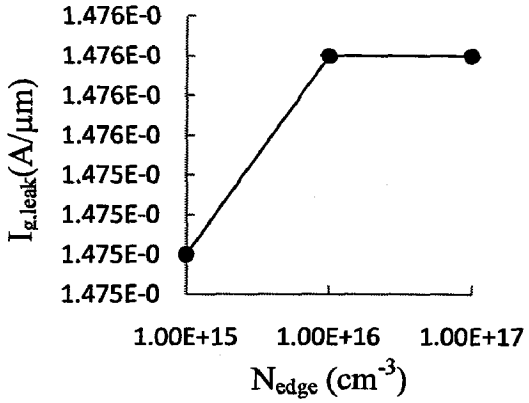

Figure 4.2 (h): Variation of $I_{g,leak}$ with N_{edge}

Simulation Results

With increased average doping gradient, the source/drain resistance ($R_{S/D}$) is decreased and the drive current increases as depicted in figure 4.2(a). But the downside is that the SCEs and I_{off} are also seen to rise. So we have a tradeoff between reduction of $R_{S/D}$ and increased SCEs

Based on these graphs, a suitable doping profile seems to be such that the doping value falls to 10^{16} cm^{-3} at the gate edge from a value of 10^{20} cm^{-3} at the source/drain i.e. an average doping gradient of 2.2 nm/decade with total extension length of 10 nm. At this value the drive current, I_{on}/I_{off} ratio and the transconductance are high enough, while threshold voltage shift, subthreshold slope increase and DIBL degradation have acceptable values. The leakage current is not much affected by the doping gradient.

4.4 High – κ Gate Dielectric Engineering

In recent years there has been a trend towards high-κ materials for use as a gate dielectric for extending the scalability of the silicon based devices. The important criteria for selecting the compounds for possible use as a gate insulator are as follows:

- It should be stable, should not react with the Si and be compatible with the processing technology.
- It should be able to block boron penetration from p-type poly-silicon gates. This criterion is withdrawn in case of metal gates.
- It should provide a high-quality electrical interface

- Also, there should be sufficient band offsets (figure) so as to act as potential barriers for both electrons and holes. This is very important as it directly affects the tunneling current.

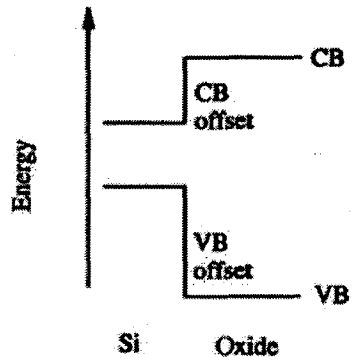

Figure 4.3: CB and VB Offsets between Si and the gate oxide

A variety of new high $-\kappa$ gate dielectrics, mostly oxides have come up in the last few years. The effect of high $-\kappa$ dielectrics in conjunction with metal gates was studied for DG FinFETs, keeping the EOT (Effective Oxide Thickness) fixed at 1 nm. Data from table 4.2 was used.

Table 4.2: Properties of various dielectrics. Taken from [26]

Gate Dielectric	Relative Dielectric Constant (κ)	Refractive index (η)	Optical Dielectric Constant (η^2)	CB Offset with Si (eV)	VB Offset with Si (eV)
SiO_2	3.9	1.46	2.13	3.1	4.7
Si_3N4	7.4	2.1	4.41	2.2	1.8
Al_2O_3	9	1.79	3.204	2.4	2.9
Y_2O_3	18	1.7	2.89	2.2	2.6
ZrO_2	14	2	4	2	2.4
HfO_2	26	2.45	6	2	2.5
La_2O_3	30	2	4	2.3	2.6

Simulation Results

The simulation results have been shown in figures 4.3(a)-4.3(f). Although the gate leakage (I_{gate} at V_G=V_S=0 V) decreases drastically, the SCEs are found to worsen with increase in κ. The drive current reduces because of mobility degradation at the high-κ/Si interface. The I_{on}/I_{off} ratio and the transconductance are also reduced, while the subthreshold slope is found to increase. The SCE degradation occurs because of loss of gate control on the channel due to the thicker higher κ gate insulator used. Further, a V_t roll – off is observed with increasing relative permittivity. This can be attributed to the enhanced fringing electric fields from the gate electrode due to higher κ, thereby enhancing the FIBL (Fringe Induced Barrier Lowering) effect [27] and reducing V_t.

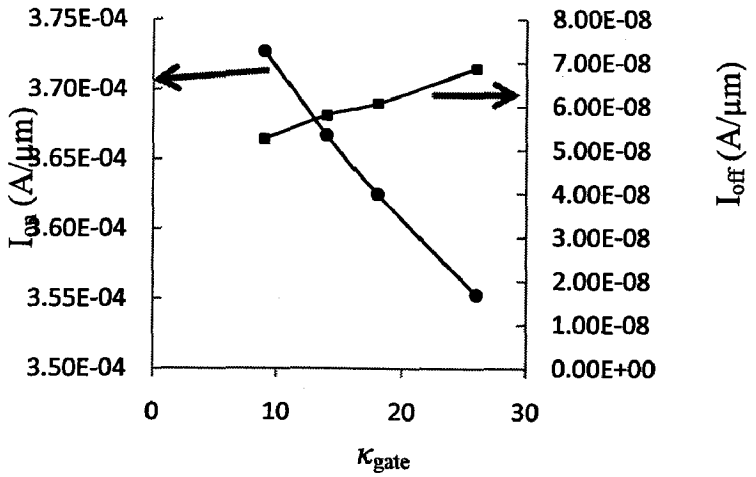

Figure 4.4(a): Variation of I_{on} and I_{off} with κ_{gate}

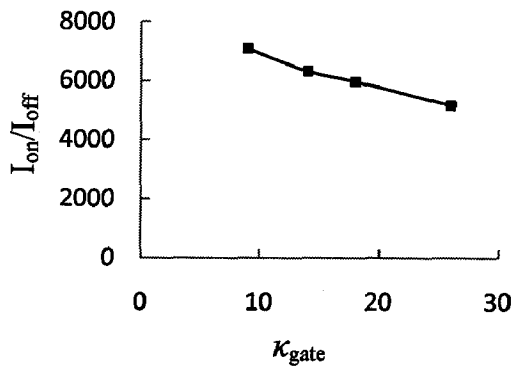

Figure 4.4(b): Variation of I_{on}/I_{off} with κ_{gate}

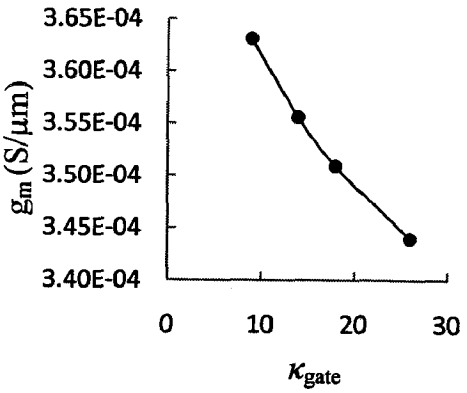

Figure 4.4(c): Variation of g_m with κ_{gate}

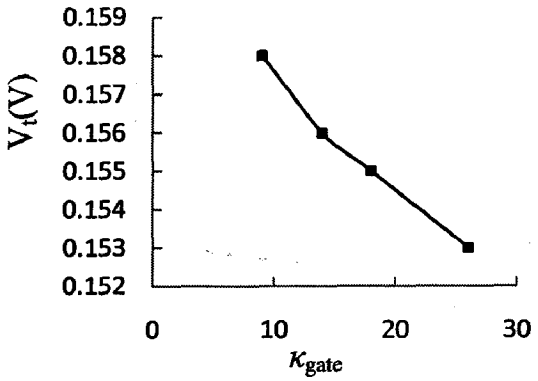

Figure 4.4(d): Variation of V_t with κ_{gate}

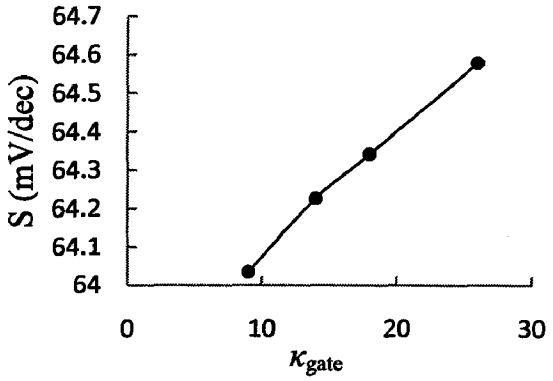

Figure 4.4(e): Variation of S with κ_{gate}

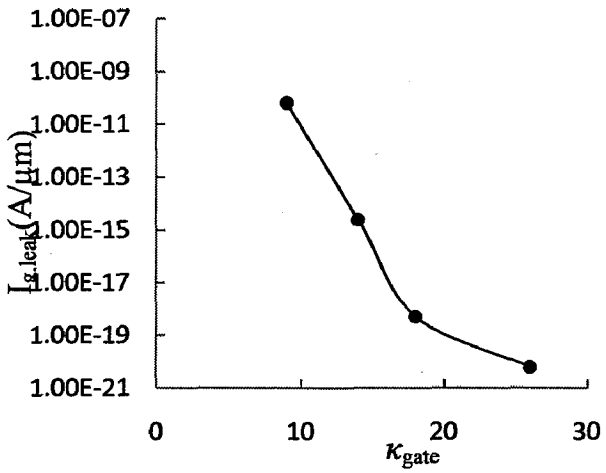

Figure 4.4(f): Variation of $I_{g,leak}$ with κ_{gate}

Hence, the use of a high κ gate material for reducing gate leakage will have to be accompanied by an increase in L_{extn} for minimizing the SCEs.

4.5 Spacer Engineering

The spacers surround the underlap regions FinFET structures as explained in chapter1. These spacers are helpful in reducing the gate leakage currents. In this study, the impact of variation of the dielectric constant of these spacers has been extensively investigated, with a view to optimize the double gate FinFET devices where achieving the ITRS targets for I_{on}/I_{off} and SCE control are of paramount significance.

4.5.1 Changing the Spacer Width (L_{spacer}) at constant L_{extn}

The effect of spacer width on the gate current was investigated using simulations of a 30 nm FinFET device with 10 nm wide fins. The spacer material used was Si_3N_4. The simulation results have been analyzed below.

It was found that as the spacer width increases, the on current increases steadily. I_{off} initially decreases and then almost saturates for spacer widths larger than 10 nm. The gate leakage current increases due increased range of the fringe field coupling between gate and channel.

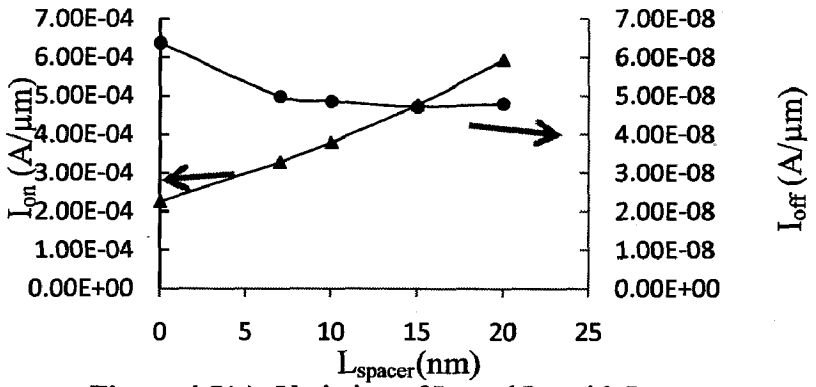

Figure 4.5(a): Variation of I_{on} and I_{off} with L_{spacer}

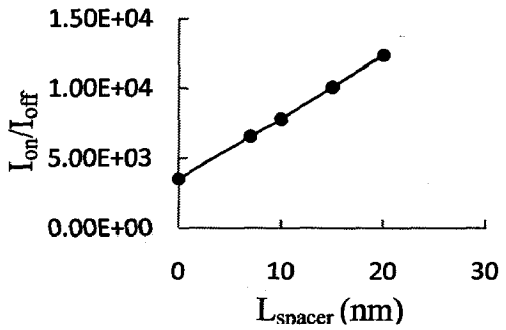

Figure 4.5(b): Variation of I_{on}/I_{off} with L_{spacer}

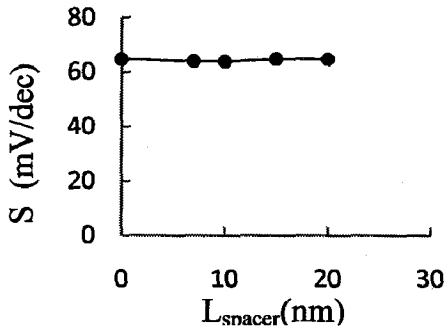

Figure 4.5(c): Variation of S with L_{spacer}

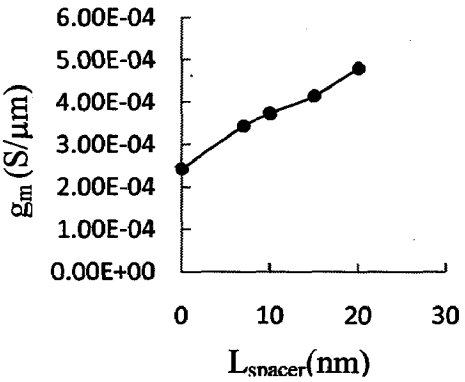

Figure 4.5(d): Variation of g_m with L_{spacer}

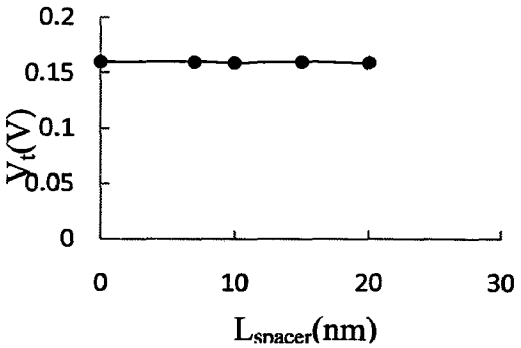

Figure 4.5(e): Variation of V_t with L_{spacer}

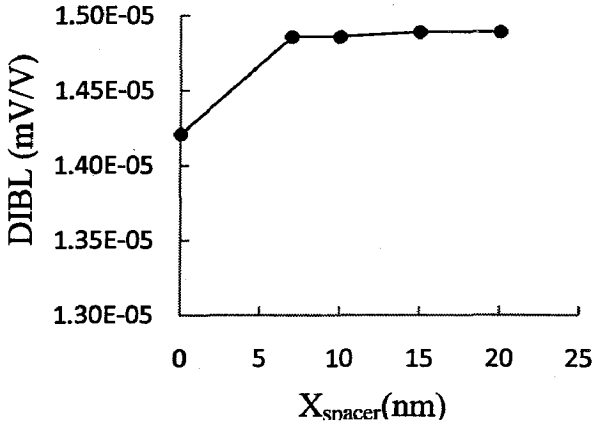

Figure 4.5(f): Variation of S with L_{spacer}

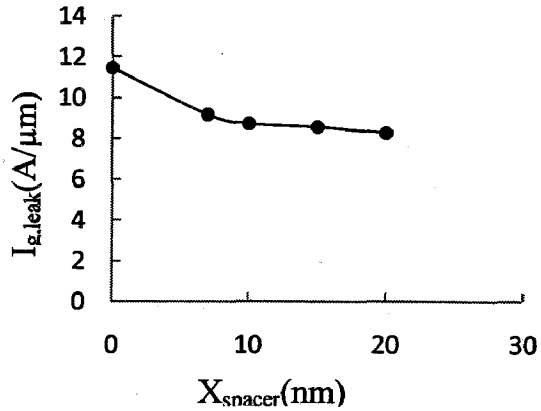

Figure 4.5(g): Variation of S with L_{spacer}

4.5.2 Effect of high –κ Dielectric Spacers

The spacer width and total extension region lengths were fixed at nm and nm respectively. The dielectric constant of the spacer material was varied upto 26. The on current was found to increase with increase in κ. It is because some amount of inversion takes place in the underlap region also because of the encroachment of the fringe fields from the gate through the high – κ dielectric. The coupling of the gate fringe field with the underlap region becomes stronger with increasing dielectric constant. A similar observation was reported in case of bulk MOSFETs with underlap in [28].

Also, the off current is found to decrease at higher values of spacer κ. Hence, the use of high - κ spacers seems to a promising technique to boost the drive current and I_{on}/I_{off} ratio of nanoscale FinFETs without sacrificing the off state leakage.

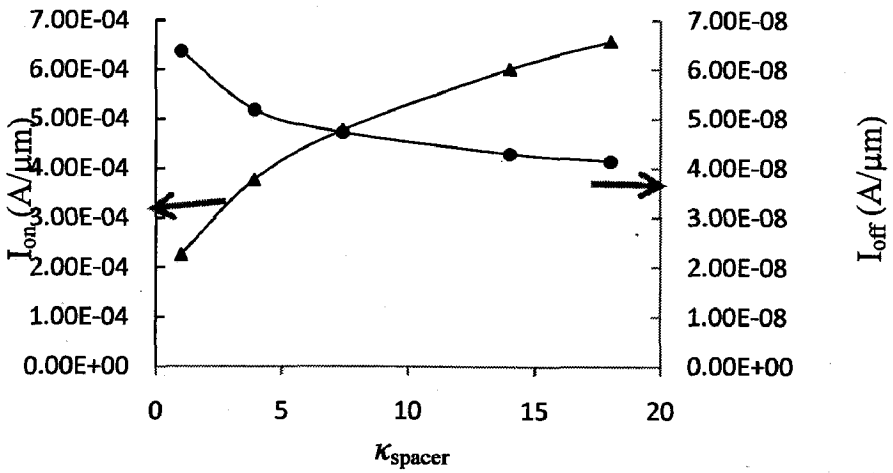

Figure 4.6(a): Variation of I_{on} and I_{off} with κ_{spacer}

The transconductance also increases because of the higher drain current at the same value of gate voltage. The threshold voltage falls by a marginal value at higher κ, implying the

additional FIBL (fringe induced barrier lowering) is not substantial. The only issue with these high κ spacers seems to be the degradation of DIBL and gate leakage.

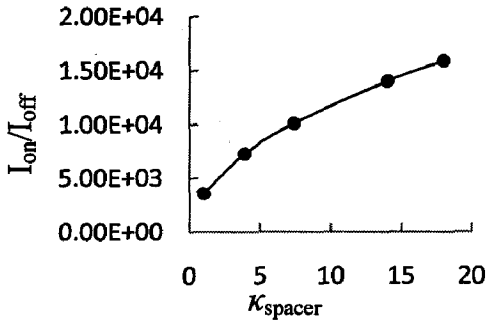

Figure 4.6(b): Variation of I_{on}/I_{off} with κ_{spacer}

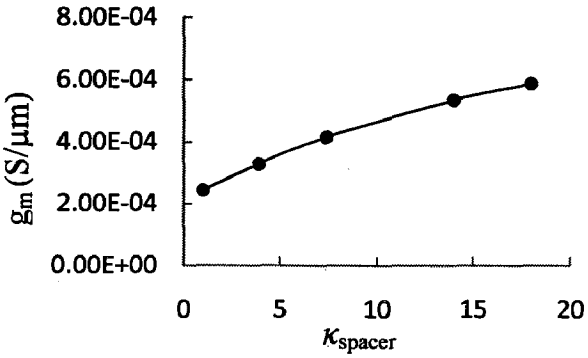

Figure 4.6(c): Variation of g_m with κ_{spacer}

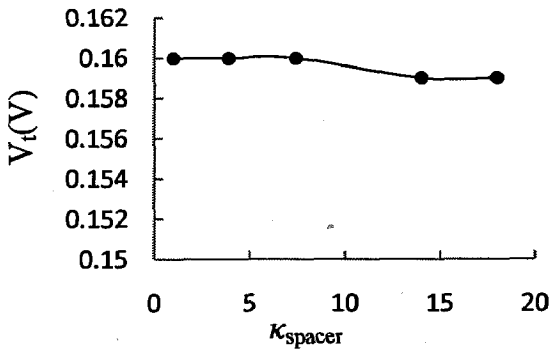

Figure 4.6(d): Variation of V_t with κ_{spacer}

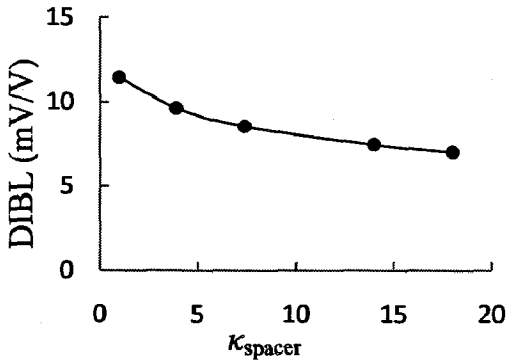

Figure 4.6(e): Variation of DIBL with κ_{spacer}

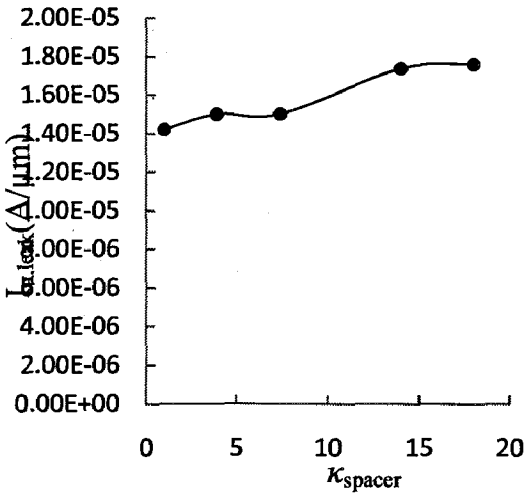

Figure 4.6(f): Variation of $I_{g,leak}$ with κ_{spacer}

4.6 Metal Gate Work function Engineering

This section describes the advantages of using metal gates instead of polysilicon gates, followed by simulation results.

4.6.1 Moving from polysilicon to metal gates

Metal gates are expected to replace the polysilicon gates as we approach the ITRS projections as several issues have arisen with the polysilicon gates in the nanoscale regime:

- **Boron penetration**: It has been reported that boron atoms used for creating p+ doped polysilicon gates (for PMOS) can penetrate into the gate dielectric [29]. The presence of boron in the oxide enhances both the electron trapping rate as well as the rate of generation of new electron traps, the effects being more pronounced at increased negative gate biases [30]. Boron penetration can cause flatband voltage shift, threshold voltage instability, reduction of channel mobility and drive current, and subthreshold slope degradation, thus creating serious reliability problems [31].

- **Polysilicon Depletion Effects**: When a MOS device is in the strong inversion regime, a depletion layer can form in polysilicon material near the interface with the gate insulator. This effect is more observable in non-degenerately doped polysilicon (a process constraint in ultra-scaled devices with very thin insulator layers, e.g. to avoid boron penetration) [32]. This causes a lowering of the inversion capacitance and slight shift in the flat band voltage resulting in increased threshold voltage.

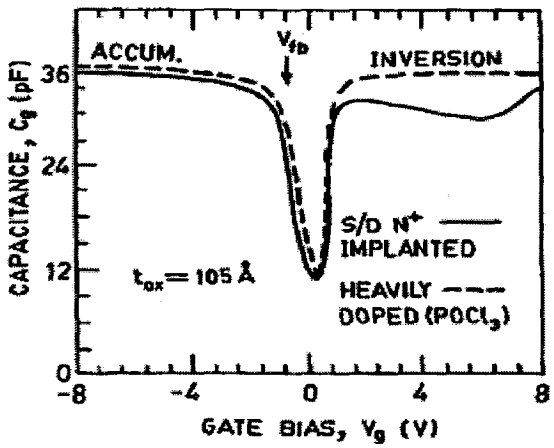

Figure 4.7: Gate capacitance variation in MOSFETs with heavily doped poly-Si (dotted line) and non-degenerately doped poly-Si (solid line) [33]

- **Incompatibility with high-κ gate dielectrics**: Fermi level pinning takes place in high- κ/poly-Si transistors, leading to high threshold voltages [34]. Also mobility degradation due to the coupling of low-energy surface optical (SO) phonon modes

arising from the polarization of the high-κ dielectric to the inversion channel carriers has been reported in literature [35].

Advantages of Metal Gates:

- Avoidance of gate - depletion
- Lower gate resistance
- Use of metal gates is effective in reducing surface phonon scattering, resulting in improved channel mobility.
- Work function tuning of various metal compounds is an attractive technique for setting the device threshold voltage without modifying the channel doping.

Quite a few metals and metal compounds have been investigated for possible use as gate material. The approach has been to find materials with the suitable the work functions for replacing n^+ and p^+ poly-Si in nMOS and pMOS. The use of materials with work functions close to the middle of the silicon band gap have been proposed for achieving symmetric threshold voltages for NMOS and PMOS devices with undoped or lightly doped fins. The threshold voltage in these devices can be tuned by varying the composition of the metal compounds.

4.6.2 Threshold Voltage Tuning by Work Function Engineering

Since the V_{dd} values have been scaled down to around 1 V, it is important that the devices have reasonably low threshold voltages. Also, for CMOS logic applications the NMOS and PMOS threshold voltages should be symmetrical (V_{Tn}= $|V_{Tp}|$). For achieving symmetric yet low enough threshold voltages, different gate work functions for the NMOS and PMOS are required. For symmetric gate devices, it is possible by using either two different materials for the two types of devices (e.g. Ti for PMOS and Mo for NMOS) or by the use of a gate material whose work function can be tuned by varying the mole fractions of constituent elements(e.g. TiN [36] and Mo [37]).

4.6.3 Simulation Results

A series of simulations were carried out for both n-FinFETs and p-FinFETs with the following structural parameters (based on simulations performed in the previous chapter and this one)

Table 4.3: Device Parameters

Device Parameter	Values used
L_g	15 nm
EOT	1 nm
$L_{extn} = L_{spacer}$	10 nm
$\kappa_{gate} = \kappa_{spacer}$	14
SDE doping gradient	2.2 nm/dec

Table 4.4: Φ Variation Results for n-FinFETs

Φ(eV)	I_{on}(A/μm)	I_{off}(A/μm)	V_t (V)	S(mV/dec)	DIBL(mV/V)
4.75	1.765e-03	1.657e-07	0.192	74.198	31.813
4.7	1.884e-03	8.277e-07	0.142	74.141	32.172
4.67	1.954e-03	2.106e-06	0.113	73.895	32.996

The results of work function variation of the metal gates are shown in table 4.4. It was observed that drive current close to the ITRS specification can be obtained in all the three cases. Both drive current and threshold voltage requirements are satisfied with Φ=4.67 eV, but the subthreshold leakage is higher than the target value by an order of magnitude.

A work function value of 4.75 eV satisfies both the I_{on} and I_{off} targets but has a higher threshold voltage than the target value. Hence for optimal on-off characteristics with acceptable values of subthreshold slope and DIBL, we will have to settle for threshold voltages higher than the ITRS projection.

The ITRS projection for the saturation threshold voltage is 0.11 V. Though it is achievable for the n-FinFETs, it was found through a series of simulations that it is

difficult to obtain a symmetric threshold voltage value of -0.11 V for the p-FinFETs. Hence it implies that for CMOS applications a higher threshold voltage for the n-FinFETs will have to be set so as to be commensurate with the high threshold voltage of the p-FinFETs. In this work, the p-FinFETs used in the SRAM design in the subsequent section have been assigned a threshold of - 0.22 V and higher (more negative) using metal gates having work functions in the range of of 4.9 eV to 5.2 eV.

Chapter 5

FinFET Based SRAM Design

5.1 Introduction

In current system on chips (SoCs) and ASICs a large portion of the total area is occupied by SRAMs. The trend of embedding SRAMs into the chips has fueled the ongoing research in nanoscale SRAMs based on the novel devices.

In this section, the 6-T SRAM cell has been designed using optimized FinFET devices for high performance and low leakage. The n-curve analysis has also been carried out for the SRAM cells under V_{dd} variation and different work functions.

5.2 A Note on Mixed Mode Simulations

In conventional circuit simulation softwares like SPICE, the electrical behavior of the devices is characterized using a compact model which is obtained by analytically finding closed form expressions describing the device operation. Although suitable for simulating complex circuits in acceptable computing times, it has it's own limitation of being a fixed node model i.e. device optimizations are either difficult or impossible to include in the model files, especially as we move away from the particular "technology node", since for doing this the whole process of developing a compact model has to be redone. Also, for novel device designs, suitable compact models are not easy to derive without taking into consideration various assumptions. These issues limit the usefulness and accuracy of compact model based circuit simulators, especially while evaluating circuits based on the new emerging devices. In contrast, in mixed-mode device simulation the solutions of the basic transport equations for the semiconductor devices are directly embedded into the solution procedure for solving the circuit equations [38]. Compact modeling is thus avoided and much higher accuracy is obtained along with great freedom to experiment with device design and it's optimization for circuit applications.

5.3 6T SRAM Cell Structure and Basic Operation

There are two back to back connected inverters which ensure complementary status of the internal nodes. There are two NMOS pass transistors for data transfer to (i.e. read access)

and from (i.e. write access) the bit lines. A schematic of the 6T SRAM constructed using double gate FinFETs is shown in figure 5.1.

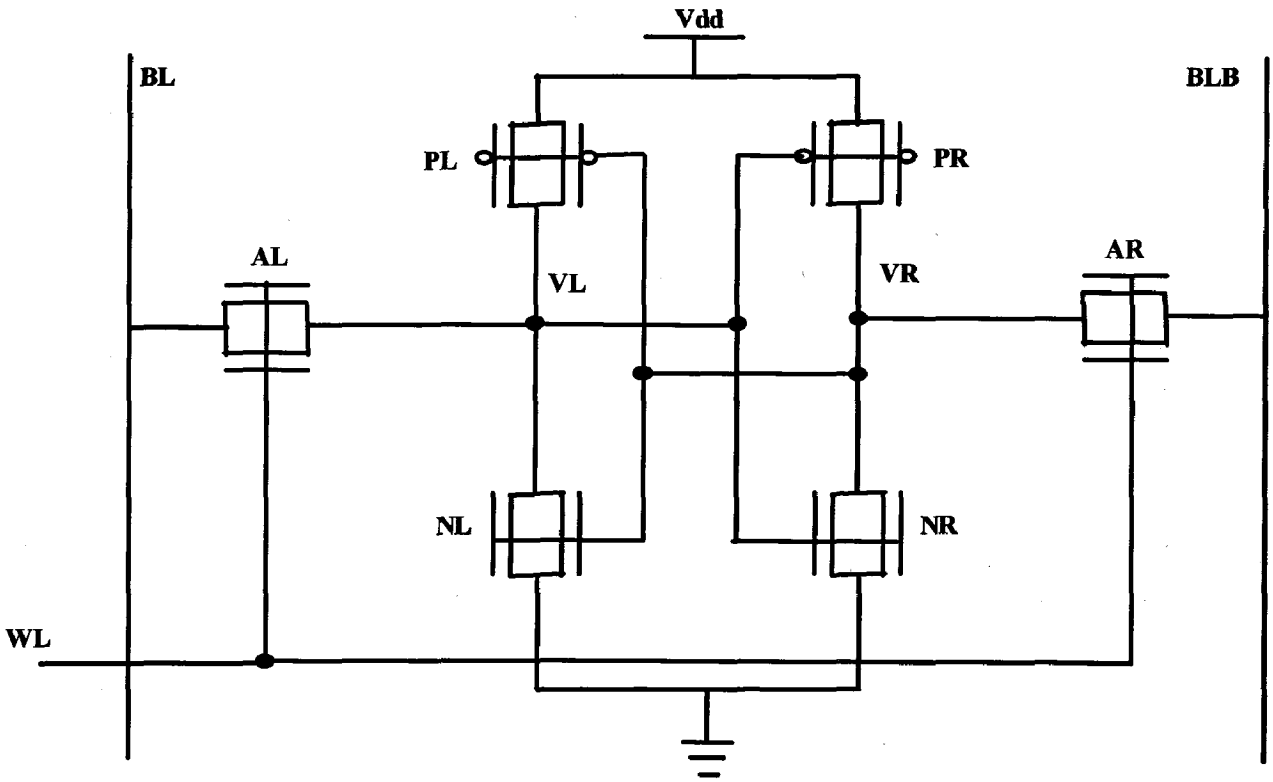

Figure 5.1: DG FinFETs based 6T SRAM Cell

Read Operation: For reading data from the memory cell, both the bit lines are precharged high and then the word line is turned on to select the cell. The bit line on the side of the cell storing a "0" will be discharged via the access transistor. The voltage difference between the bit lines is amplified by a sense amplifier and thus the content of the SRAM cell is known.

Write Operation: For writing a "0" into a node, the corresponding bit line is pulled down and to write a "1" into a node the complementary node is pulled down through the access transistors, while maintaining a "high" on the word line.

5.4 Stability Criteria for the 6T SRAM

Read Stability Condition: During a read operation, the voltage at the node storing a "0" is raised to a value determined by the relative strengths of the pull down transistor (NR) and the access transistor (AR). To ensure a non – destructive read i.e. avoid the flipping of the cell content, it is important that this rise should not exceed the switching threshold

of the other inverter. The ratio of (W/L) of the pull down transistor to that of the access transistor determines how high the "0" node voltage will rise and is usually known as the cell ratio, $CR = (W/L)_{NR}/(W/L)_{AR}$. Generally a CR greater than 1 ensures read stability.

Write Ability Condition: For a successful write operation to occur, the node which is initially at "1" has to be pulled below the switching threshold of the inverter to which this node is connected as input. The ratio of (W/L) of the pull –up transistors and access transistors, known as the pull up ratio (PR) is the determining factor for this issue. $PR = (W/L)_{PR}/(W/L)_{AR}$

Noise Margins:

Hold SNM: In the hold mode *i.e.* when the access transistors are switched off, the PMOS load transistor (PT) must be strong enough to compensate for the sub-threshold and gate leakage currents of all the NMOS transistors connected to the storage node containing a "0". The increased leakages, low cell supply voltages and increased variability in nanometer technologies make it a critical issue. Hold stability is determined by cell static noise margin (SNM) in standby mode (WL=0, BL=BLB=1). SNM is defined as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the cell state. In the conventional circuit arrangement for measuring the SNM, two DC noise voltage sources are placed in series with the cross-coupled inverters and with worst-case polarity at the internal nodes of the cell [39]. Graphically, the SNM is given by the length of the smaller of the two largest squares contained within the wings of the butterfly curve, as shown in figure 5.2.

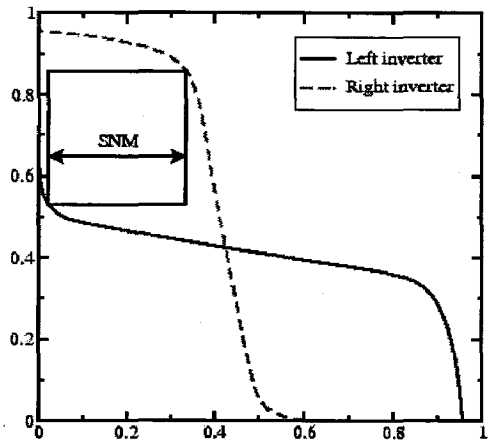

Figure 5.2: SNM Butterfly Curves

Read Noise Margin (RNM) : The read stability be represented in terms of Read SNM values, also obtained from the butterfly curves corresponding to a read access condition (WL=1, BL=BLB=1) . The cell is most vulnerable to noise during the read access. The RNM can be improved by increasing the pull up ratio, but has the problem of increased area.

Write Noise Margin (WNM): The conditions for evaluating the write noise margins from the SRAM cell's butterfly curves is WL=1, BL=1 BLB=0. Write SNM can be increased by reducing the pull up ratio.

5.5 N-Curve Based Read Stability and Write Ability Analysis

An important issue with the SNM as measured by the butterfly curves concepts for cell stability is that it's not possible to measure it with automatic inline testers. The SRAM N-curve analysis methodology doesn't suffer from this limitation as it involves the measurement of current and voltage at a single internal node which is possible by using inline parametric testers [40]. Also, knowledge of current information is also required along with the conventional noise voltage margins to properly assess the stability and write ability of an SRAM cell.

Figure 5.3 shows the setup for extracting the N-curve during read operation [41]. The bit-lines are clamped at V_{dd} and the word-line is activated. A voltage sweep V_{in} from 0 V to V_{dd} is then applied at "0" internal storage node V_R to obtain the corresponding current I_{in}. The N-curve is obtained by plotting the internal node voltage V_R against the current I_{in}. Figure 5.4 shows the butterfly curves and the N-curves obtained from the measurements as depicted in figure 5.3. The injected current I_{in} is zero at the three points A, B and C. Points A and C correspond to the two stable points of the butterfly curve while B corresponds to the meta-stable point in the butterfly curves.

The N- curve based performance metrics [41]

- **Static Voltage Noise Margin (SVNM):** It is the maximum dc voltage that can be applied into the SRAM cell storage node in the read mode, before its content changes. This is given by the voltage difference between point A and B in the N-curve.

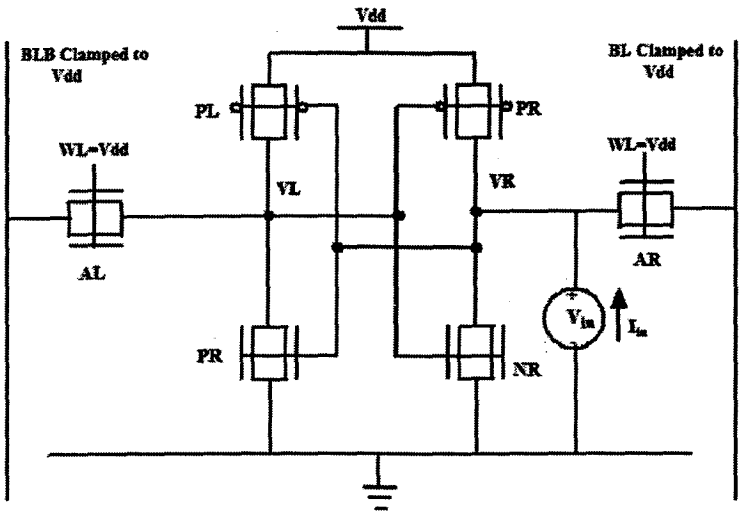

Figure 5.3: Circuit Arrangement for extracting the read N-Curve. Adapted from [41]

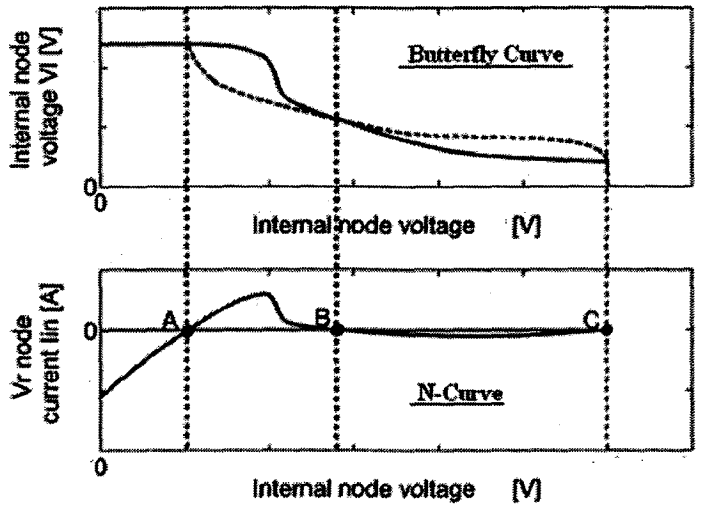

Figure 5.4: The butterfly curve and N-curve of the cell

- **Static Current Noise Margin (SINM):** It is defined as the maximum value of DC current that can be injected in the SRAM cell before its content changes. This additional current information given by the peak current located between points A and B is an important parameter that can be used to characterize the cell read stability. The SVNM and SINM definitions together provide better criteria of the cell stability. For example, a small SVNM combined with a large SINM will still result in a stable cell since the amount of required noise charge to disturb the cell is large. Hence, two SRAM cells with the same SNM and SVNM values may not be equally stable and it is the SINM that will be a deciding factor. Thus a correct analysis of the read cell stability requires the knowledge of both the N-curve metrics SVNM and SINM.

- **Write Trip Current (WTI):** It is the amount of current needed to perform a write operation in the cell when both bit-lines are maintained at V_{dd}. At the WTI value the cell-content changes, and can be seen as the current margin of the cell. Since for write operation, the node storing a "1" is discharged by pulling the bit line to ground, the N-curve has to be analyzed from the right-most zero crossing point C towards the left. The WTI is equal to the height of the negative current peak between points C and B. Now higher the WTI, more is the current needed or higher is the amount by which the bit line voltage has to be pulled down, implying a lower value of Write Trip Point. The value of WTI should be large enough to so as to avoid unwanted writes, while a smaller value makes it easier to do a write operation.

- **Write Trip Voltage (WTV):** It is the voltage drop needed to flip the internal node containing "1" with both the bit-lines clamped at Vdd. Graphically, it is given by the voltage difference between point C and B. To estimate the write ability of the cell, we need to have the knowledge of both WTV as well as WTI. Increasing the transistor widths of cell degrades the WTI while it improves the SINM, thus again confirming the conflicting constraints between the read and write operation of the cell.

5.6 Simulation Results

In these simulations the geometry of both the n-FinFETs and p-FinFETs were set at the values depicted in table 4. 3.

5.6.1 Effect of variation of the work function of the access transistors

The work functions of the access transistors (AR, AL) were varied from 4.65 eV to 4.8 eV while keeping the work functions of the load p-FinFETs and driver n-FinFETs at 5.1 eV and 4.75 eV respectively. Figure 5.5 shows the read condition butterfly curves.

The read noise margins were found to increase with the increase in the work function of the metal gates of the access transistors. Figure 5.6 shows the read N-curves.

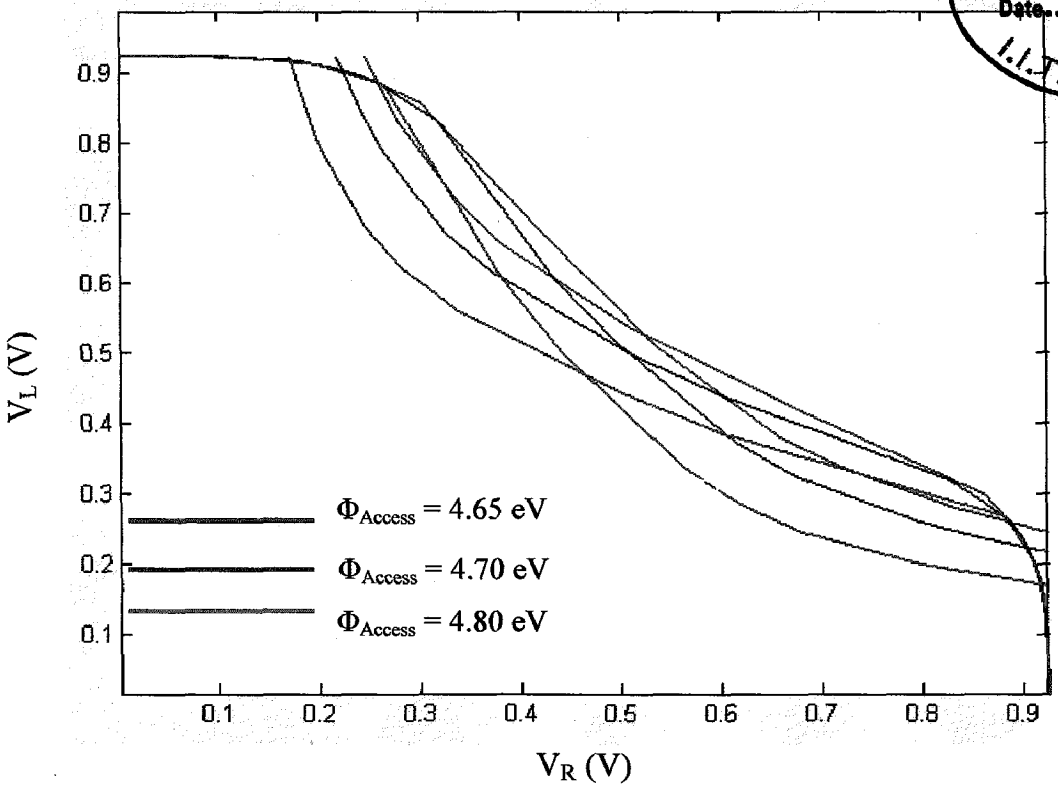

Figure 5.5: Butterfly curves showing the impact of Φ_{AR} modulation on read noise margin

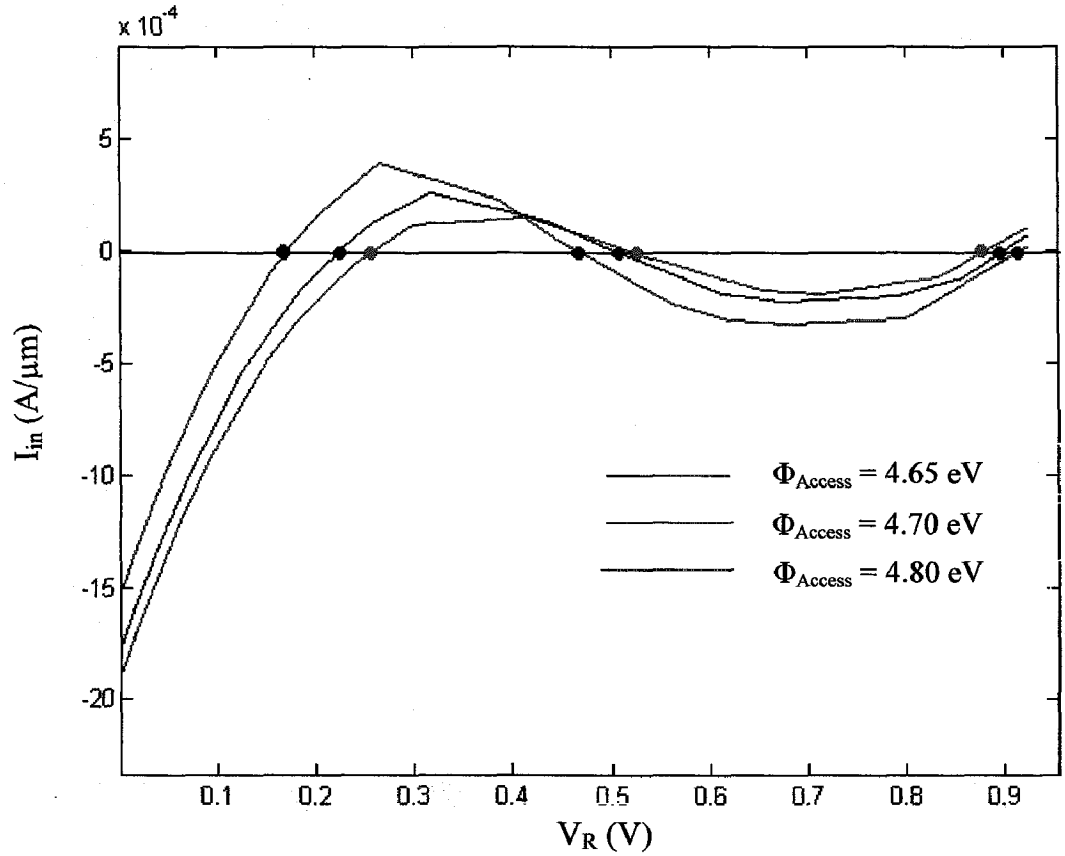

Figure 5.6: The N-curves showing the impact of Φ_{AR} modulation

There is a slight increase in the SVNM. Also the SVNM values are larger than the SNM values. SINM was relatively more affected than the SVNM by the change in work function and was found to increase with increase in the work function of the access transistors. Hence it means that the read stability improves on increasing the work function and making the access transistor weaker. WTI and WTV both increase as Φ_{Access} is changed from 4.65 eV to 4.8 eV. The WTI increase translates into a better current margin with regard to the cell's read stability, but it also means that writing into the cell will require larger currents. Equivalently, it implies that the larger values of the WTV will result in slower write operations.

5.6.2 Effect of Variation in supply voltage

V_{dd} was varied from 0.7 V to 0.8 V for the SRAM designed with p-FinFET work functions of eV, driver n-FinFET at 4.75 eV and access n-FinFET at 4.7 eV. The butterfly curves corresponding to the read mode have been shown in figure 5.7. It was found that the read noise margin is degraded with reduced V_{dd}.

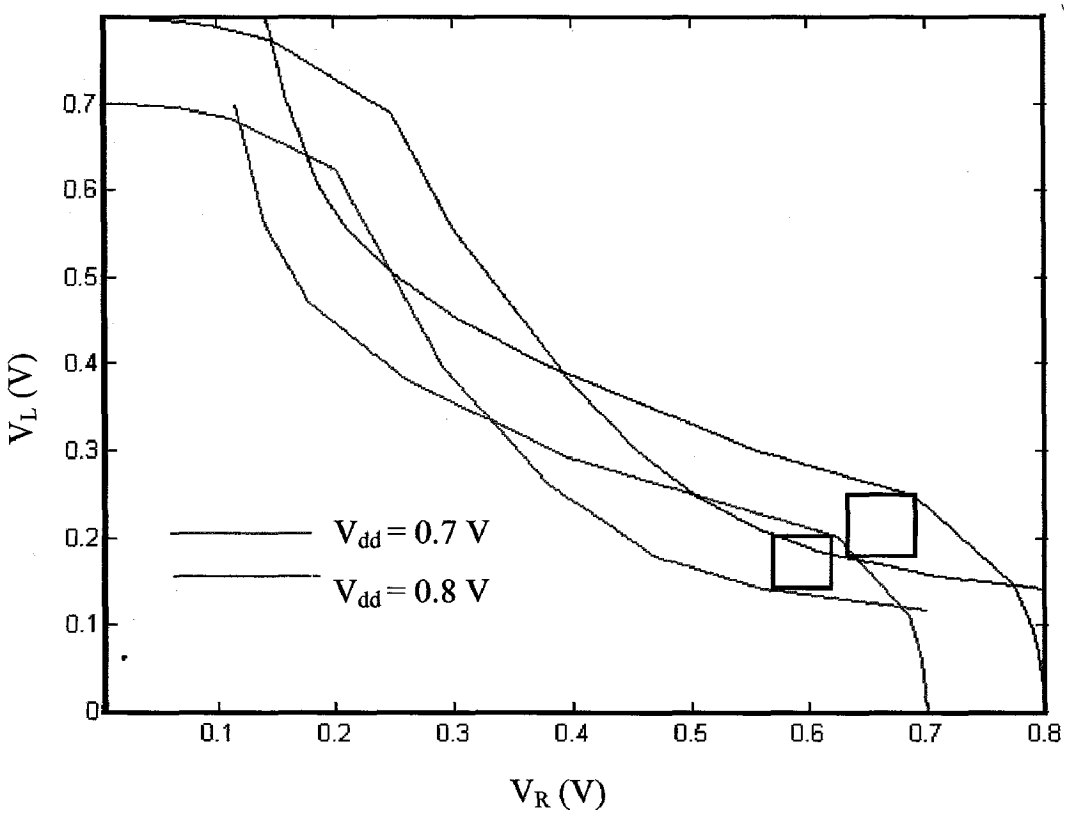

Figure 5.7: Effect of V_{dd} variation on read SNM

The read N-curves corresponding to different V_{dd} values are shown in figure 5.8. The read stability metrics SVNM and SINM both are found to degrade. Thus the cell stability is limited by V_{dd} scaling. But, as shown in section 5.6.1, the SINM can be improved by increasing the access transistor work function and hence a more stable cell can be designed for low supply voltage operations despite lower voltage noise margins.

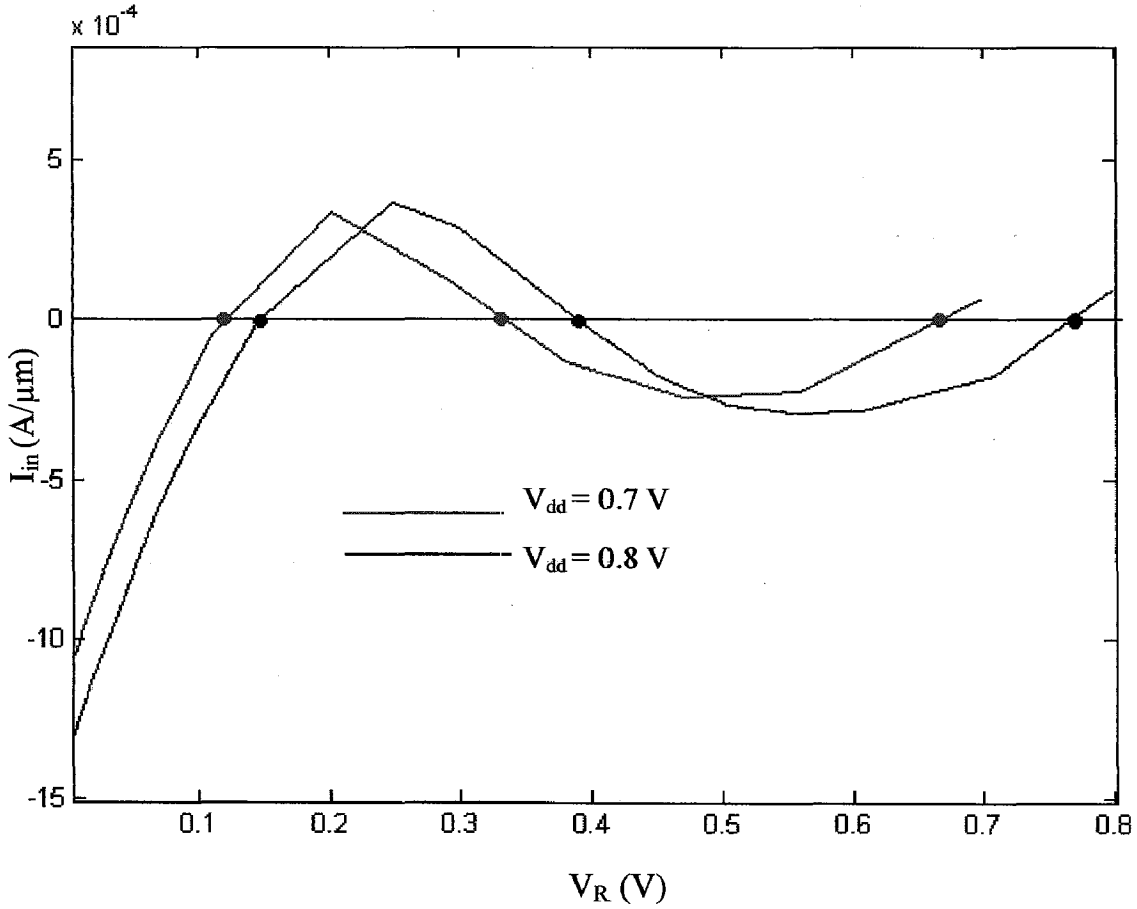

Figure 5.: Effect of V_{dd} variation on the SRAM N-curves

Thus it has been demonstrated that work function engineering can be an alternate way of controlling the noise margins of SRAM cells, instead of changing the transistor widths. This is particularly important for FinFETs where pull up ratio and cell ratio can't be set to any arbitrary values by transistor sizing since the fin widths are quantized due to the process constraint of keeping constant fin heights [42]. Also this analysis showed the importance of the N-curve metrics in gauging the performance of nanoscale SRAMs.

Chapter 6

Conclusions

A thorough analysis of the scaling issues in double gate FinFET devices with gate lengths of 30 nm and below was carried out in this dissertation work using the Sentaurus simulation package. It was found that gate length scaling severely degrades the device performance, reducing the I_{on}/I_{off} ratio, causing V_t roll- off and increasing the DIBL and subthreshold slope. It was seen that fin thickness reduction is necessary to improve the SCEs and gate leakages at small gate lengths. Though oxide thickness scaling results in better transistor characteristics, the gate leakage increases excessively. It was found that the image force effect plays an important role and its impact can't be neglected while evaluating gate leakages as it can increase leakage currents by an order of magnitude. Scaling down of the gate thickness results in higher drive currents and lower off currents, but gate transconductance and subthreshold slope were found to degrade. The effect of fin doping was also studied. It was seen that the transistor performance deteriorates on all fronts on increasing the doping. Hence it is better to keep the channel undoped or lightly doped.

For optimizing the 15 nm devices so as to approach the ITRS targets different techniques were applied in this work. Through simulations, a suitable doping gradient was selected for Gaussian doping in the SDE region as there is a trade - off between I_{on}/I_{off} ratio and SCEs. High – k gate dielectrics are necessary to suppress gate leakages. It was observed that although the gate leakage decreased drastically, the I_{on}/I_{off} ratio and transconductance were reduced and DIBL and subthreshold slope deteriorated along with a V_t roll-off with increase in κ. Hence a moderate value of κ_{gate} needs to be used. Also, an increase in the L_{extn} can be considered for improving the SCEs while using high - κ materials.

Investigation of high- k dielectric spacers threw up some interesting results. Through the use of high - κ spacers, it is possible to boost the drive current and I_{on}/I_{off} ratio of nanoscale FinFETs and reduce the off-state leakage simultaneously. Work function tuning was used for setting the threshold voltages of the optimized devices. It was found that for optimal on-off characteristics with acceptable values of subthreshold slope and DIBL, we will have to settle for threshold voltages higher than the ITRS projection.

Finally, a 6T SRAM cell was simulated using optimized n-FinFETs and p-FinFETs using mixed mode simulations to evaluate the read stability and write ability using conventional SNM as well as N-curve based metrics. It was found that increasing the work function of the access transistors results in higher read stability but slower write operation. Reducing the supply voltage had a detrimental effect on the cell noise margins, but the current noise margins can be improved by increasing the work function of the access transistors. Thus work function engineering can be used to circumvent the sizing constraints in FinFET based SRAMs due to fin – width quantization.

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