HARMONICS AND VOLTAGE STABILITY ANALYSIS IN POWER SYSTEMS USING FACTS BY THYRISTOR-CONTROLLED REACTOR

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ALTERNATE HYDRO ENERGY SYSTEMS

By

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CANDIDATE'S DECLARATION

I hereby declare that the work is being presented in the dissertation entitled **"Harmonics and Voltage Stability Analysis in Power Systems using FACTS by Thyristor Controlled Reactor"** in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in "**Alternate Hydro Energy Systems**" submitted at Alternate Hydro Energy Centre, Indian Institute of Technology, Roorkee is an authentic record of my own work carried out during a period from July 2006 to June 2007 under the supervision of **Shri S. N. Singh, Senior Scientific Officer, Alternate Hydro Energy Centre, Indian Institute of Technology, Roorkee.**

I have not submitted the matter embodied in this report for the award of any other degree or diploma.

Rudra Rameshwar

Date: June 27, 2007 **(RUDRA RAMESHWAR)**

Place: Roorkee

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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Date: June 27, 2007 **(RUDRA RAMESHWAR)**

ABSTRACT

In this study, non-sinusoidal quantities and voltage stability, both known as power quality criteria, are examined together in detail. The widespread use of power electronics elements causes the existence of significant non-sinusoidal quantities in the system. These non-sinusoidal quantities can create serious harmonic distortions in transmission and distribution systems. In this dissertation, harmonic generation of a static VAR compensator with Thyristor-Controlled Reactor and effects of the harmonics on steady-state voltage stability are examined for various operational conditions.

KEYWORDS

Harmonics, Stability, Thyristor-Controlled Reactor (TCR), etc.

CONTENTS

PUBLICATIONS

1. **Abstract is Selected and Full Paper is submitted on *"Harmonics and Voltage Stability Analysis in Power Systems Using FACTS by Thyristor Controlled Reactor"* in International Conference in Energy Research, Organised by Indian Institute of Technology, Bombay, Dec. 12-14, 2007.**

2. **Paper Accepted on *"FACTS, HVDC Controls and Their Applications"* in the All India Conference conducted by Institution of Engineers India, Guwahati Centre, Dec. 14-16, 2006.**

LIST OF FIGURES

INTRODUCTION AND LITERATURE REVIEW

1.0 INTRODUCTION TO FACTS

The main objective of any AC transmission or distribution line compensation is to increase the steady state and short term power transfer capability of the existing transmission systems. This chapter describes the general concept of AC transmission system compensation using tools such as shunt and series capacitive or reactive compensation and then the new concept of solid-state, converter-based Flexible AC Transmission Systems (FACTS) is introduced. The chapter reviews the previous works on FACTS schemes and presents the full thesis outline and structure also incorporated in Literature Review.

1.1 ELECTRICAL TRANSMISSION SYSTEMS

Almost all electrical energy in the world is generated in the form of three phase AC power and transmitted via high voltage AC transmission systems. Rapid growth in electrical energy utilization, combined with the increased demand for efficient low cost electrical energy has gradually led to the development of generation sites remotely located from the major load centers. To enhance the AC system stability, security and reliability multiple AC transmission grids, connecting load centers to remote generation and neighboring utilities, are constructed. These interconnections have led to the evolution of complex transmission grids that pool power plants and load centers all for the sole purpose of minimizing the total power generation capacity and cost, while ensuring supply reliability and security. They enable taking advantage of time diversity of electric loads, availability of other local generation resources and fuel price to supply the power to the loads at minimum cost with specified reliability index. On the other hand, the increased demand on the transmission grid, absence of long term planning and

deregulated open market with multiple companies and large customer pools have created new system security and reliability problems [1],[2].

1.1.1 Transmission Line Loading Capability

Basically, there are three factors that limit the lading capability of a transmission line [1],[3]. These factors can be classified to thermal, dielectric and stability limits. Thermal capability of an overhead line is a function of the ambient temperature, wind conditions, and conductor-to-ground clearance. The nominal thermal rating of a transmission line is generally determined on a conservative basis [3].

The dielectric limit is determined by voltage limit of insulators. Since insulators are usually designed very conservatively (2.5-3pu), for a given nominal voltage it is often possible to increase the line voltage by 10% without exceeding the specified Basic Insulation Level [4]. From the stability viewpoint, there are several issues that limit the transmission capability. They are Transient Stability, Dynamic Stability, Steady-State Stability, Voltage Stability and Harmonic Stability [5], [6], [7].

1.2 POWER FLOW IN AN AC TRANSMISSION SYSTEM

Figure 1.1 shows a two-bus interconnected power transmission system.

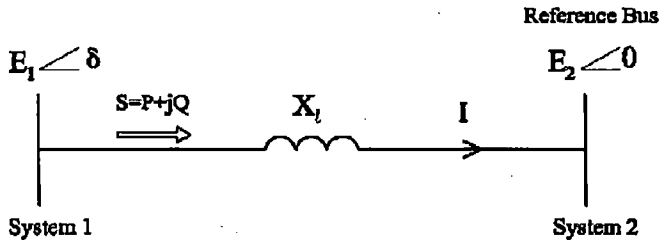


Figure 1.1: A Two-Bus Power Transmission System

Assuming E_1 and E_2 are the magnitudes of the internal voltages of the two equivalent machines representing buses 1 and 2, the real and reactive power at bus 2 can be obtained as:

$$I = \frac{E_1 \angle\delta - E_2}{jX_l} = \frac{E_1 \sin\delta}{X_l} + j\left(\frac{E_2 - E_1\cos\delta}{X_l}\right) \tag{1.1}$$

$$S = E_2 I^* = \frac{E_1 E_2 \sin\delta}{X_l} + j\left(\frac{E_1 E_2 \cos\delta - E_2^2}{X_l}\right) = P + jQ \tag{1.2}$$

$$P = \frac{E_1 E_2}{X_l}\sin\delta \tag{1.3}$$

$$Q = \frac{E_1 E_2 \cos\delta - E_2^2}{X_l} \tag{1.4}$$

Figure 1.2 shows the phasor diagram of this transmission system where ($E_L = E_1 - E_2$) is the voltage drop across the transmission line. Since $I = E_L/jX_l$, line current is perpendicular to E_L.

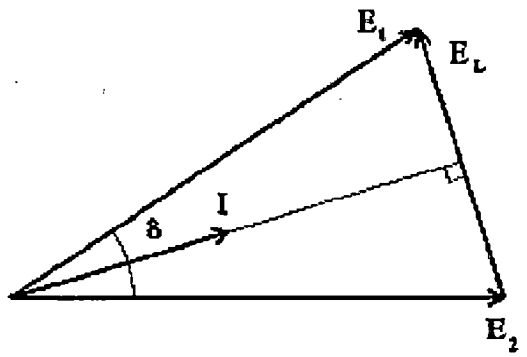


Figure 1.2: Phasor Diagram of the Two-Bus Transmission System

1.2.1 The Concept of AC Transmission System Compensation

The effects of changing the magnitudes of sending bus voltage, E_1, and system reactance, X_l, on the power flow as well as transient and steady state stability are presented in this section. Figure 1.3 shows the effect of changing $|E_1|$ by a small value. Changing $|E_1|$ by the small value, ΔE_1, does not change the magnitude of the transmission system voltage drop, E_L, by an appreciable value, however it does change its phase angle by much and also the phase angle of line current, Φ. Therefore regulating the magnitude of E_1 has profound influence on reactive power flow but not real power.

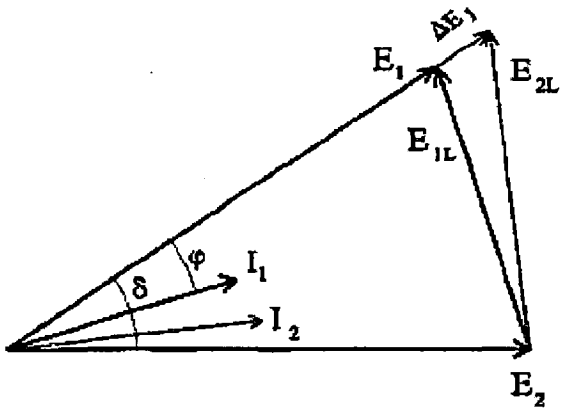


Figure 1.3: Effect of | E_1| on the Transmission System

As equations (1.3) and (1.4) indicate, when the real power demand of the line increases, the reactive power demand is also increased. In other words, to provide and increase in real power demand, reactive power has to be increased [3],[6]. Hence shunt capacitive compensation, may be required to maintain the system bus voltage E_1within specified limits and provide the required reactive power.

Controlling the magnitude of transmission line reactance, X_l, can control the real power flow within the specified maximum line capacity [3],[8]. Figure 1.4 shows the power angle curves for variations in system equivalent reactance, X_l, as described by equation (1.3). For a given power angle, δ, and bus voltage magnitude, reducing X_l will increase the real power flow by increasing the steady state stability or maximum power.

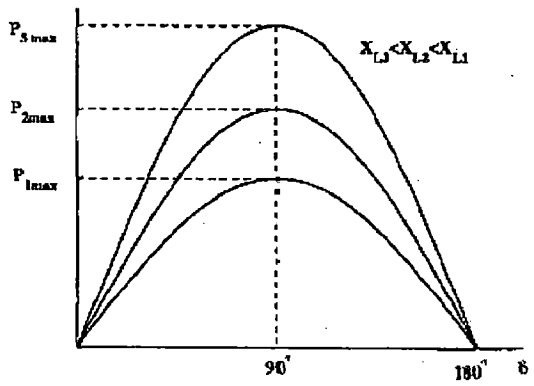


Figure 1.4: Effect of X_l on Power-Angle Curves

This can be easily achieved by capacitive series compensation that cancels as portion of line reactance as shown in Figure 1.5. Therefore series compensation is a powerful approach to increase the transmission line capability or power capacity [3],[5].

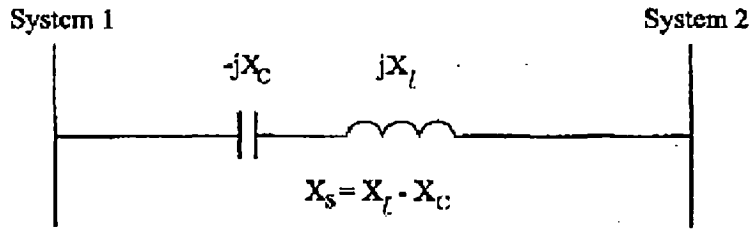


Figure 1.5: Effect of Series Capacitor on the Total Line Reactance

Besides, for a given real power, P, reducing X_l, corresponds to a reduction in operating power angle, δ. Therefore series capacitive compensation improves both transient and steady-state stability limits of the transmission system [5],[6]. This is an important aspect of a power system and power flow. Series capacitive sizing and location as well as control strategies depend on system topology and operating conditions [9].

1.2.2 Conventional Control of Transmission Line Power Flow

The conventional techniques to control the power flow over HV transmission lines are generally implemented in the generating stations to provide the power requirements of the load [2]. They include speed-governors, excitation systems, tap-changing transformers and phase-shifting transformers.

The speed-governors system provides full control of synchronous generator output power by regulating the input power or prime mover torque while the excitation system of synchronous generator provides as fast-regulating field current control, hence controlling the generated voltage. However, when the synchronous generator is connected to very large power system, voltage is almost stabilized and the excitation control can result in changing the reactive power [10],[11].

Tap-changing transformers provide a limited range of voltage control and therefore can be used to slowly control the reactive power flow within limits (±10% - ±15%). Finally, phase-shifting transformers are special series-connected transformers that introduced phase shift in the transmission system voltages and hence control the power flow [1],[2].

1.3 FLEXIBLE AC TRANSMISSION SYSTEMS (FACTS)

Flexible AC Transmission Systems (FACTS) is a new concept based on power electronic switching devices and controllers to enhance the transmission grid utilization and power capacity as well as stability, security, reliability, power quality and efficient interconnections. This concept can be more clarified by the IEEE definitions of *Flexibility*; FACTS and FACTS Controllers [1].

Flexibility of Electric Power Tranmission: *The ability to accommodate changes ion the electric transmission or operating conditions while maintaining sufficient steady-state and transient margins.*

Flexible AC Transmission Systems: *Alternating current transmission systems incorporated power electronic-based and other static controllers to enhance controllability and increase power transfer capability.*

FACTS Controllers: *Power electronics-based systems and other static equipment that provide control of one or more AC transmission parameters.*

The possibility that the current and power of a transmission line can be fully controlled at a reasonable cost enables a large potential of increasing the capacity of the existing transmission systems. These new opportunities are provided through the ability of FACTS controllers to control the interrelated parameters that govern the operation of a transmission system.

FACTS technology is based on high power line or self-commutated solid-state devices such as thyristors and Gate Turn-off thyristors (GTO) that provide the ability to continuously control the transmission system in order to meet the power flow requirements. Recent advances

in solid-state technology have introduced thyristors and GTOs in higher voltage and current ratings such as (5.5 KV, 4KA) for thyristors and (4.5 KV, 4KA) for GTOs [1]. Therefore FACTS controllers with a reasonable capacity of a few hundred of Megawatts can be realized in large interconnected power pools.

1.3.1 Conventional Thyristor-Based FACTS Schemes

By definition, capacitors generate and reactors absorb reactive power in AC systems. They have been used with mechanical switches for shunt and series compensation since the early days of AC power transmission [3],[5].

Since the early 1970s line commutated thyristors in conjunction with capacitors and reactors have been employed in various circuit configurations for variable shunt and series compensation. The shunt compensation device is called Static Var Compensator (SVC) and is defined as [1]:

Static Var Compensator: *A shunt-connected static Var generator or absorber whose output is adjusted to exchange capacitive or inductive current so as to maintain or control specific parameters of the electrical power system. (typically bus voltage)*

SVC is based online-commutated thyristor-switched capacitors and modulated reactors. Fixed Capacitor, Thyristor-Controlled Reactor(FC-TCR) is an example of SVC scheme as shown in Figure 1.6. By controlling the firing angles of T1 and T2 reactive power compensation can be adjusted to the desired value. At the maximum capacitive Var output, the thyristor- controlled reactor is off ($\alpha = 90^0$). By decreasing the delay angle, α, the inductive current increases and therefore the net capacitive Var output decreases. At zero delay angle maximum inductive Var output is obtained and the total SVC Var output is the difference between the capacitor and thyristor-controlled reactor Vars [12].

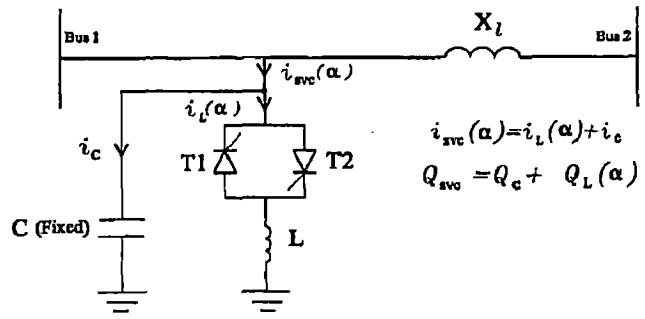


Figure 1.6: Fixed Capacitor, Thyristor-Controlled Reactor (FC-TCR)

Thyristor-Controlled Series Capacitor (TCSC) is another example of thyristor-controlled series compensation. Figure 1.7 shows the basic configuration of TCSC. It was proposed in 1986 by Vithayathil with others [1] as a method of rapid adjustment of equivalent system reactance, X_l. The TCSC presents a smoothly variable parallel LC series blocking circuit. The total series reactance of TCSC is function of the delay angle of thyristors, α.

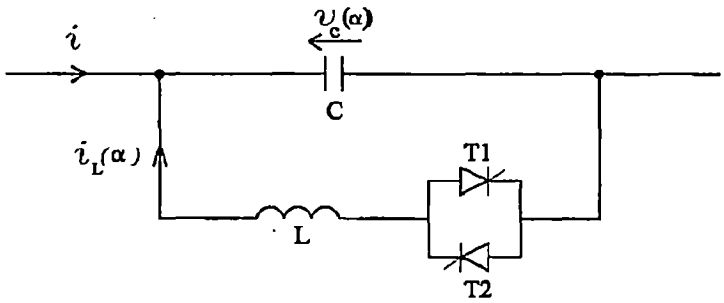


Figure 1.7: Thyristor-Controlled Series Capacitor (TCSC)

The total TCSC reactance is:

$$X_{TCSC}(\alpha) = \frac{X_C X_L(\alpha)}{X_L(\alpha) - X_C} \tag{1.5}$$

At $\alpha = 90^0$, the inductor is off ($X_L = \infty$) and the maximum capacitive series reactance is obtained. By reducing α, the capacitive reactance of TCSC decreases until parallel resonance at $X_C = X_L(\alpha)$ is established and the total reactance is theoretically infinite. Therefore the operation of TCSC should be avoided in this region. Further reducing of α creates an inductive series reactance and the maximum inductive reactance is obtained at $\alpha = 0$ [1].

1.3.2 Switching Converter Type FACTS Schemes

The most significant difference between the new approach of FACTS implementation and the conventional one is that it does not employ discrete capacitor or reactor banks for shunt or series compensation, but rather it employs dc-ac link converters to exchange shunt or series reactive power with the transmission system. It should be noted that "*converter*" is used as general description of any solid-state device (converter or inverter) that converts either AC or DC voltage to the other form. Since in FACTS applications the flow of real power can be from either DC or AC side to the other side, "*converter*" is used as a general term. For reasons of economics and design simplicity, voltage-source converters are often preferred over current-source converters for FACTS applications [1].

The FACTS shunt compensation scheme is called *Static Synchronous Compensator* (STATCOM) as shown in Figure 1.8.

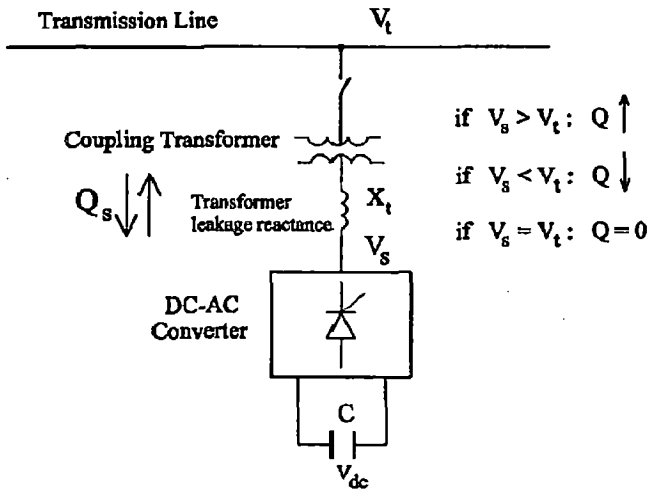


Figure 1.8: General Diagram of the Static Synchronous Compensator (STATCOM)

The basic concept of the STATCOM is that a set of three phase voltage in phase with line voltage can transfer reactive power between the power system and STATCOM. The direction of reactive power flow, Q_s, depends on the relative magnitudes of line and STATCOM voltages, V_t and V_s, respectively. Since V_t and V_s are in phase there is no real power exchange between the STATCOM and the transmission system. In Figure 1.8 the direction of reactive

power flow is from the STATCOM to the transmission system if ($V_s > V_t$) and vice versa. Therefore by controlling the magnitude of V_s reactive power exchange can be continuously adjusted to meet any compensation level [13].

Similarly the series compensation device is called *Static Synchronous Series Compensator (SSSC)* as shown in Figure 1.9. It is well-known that a series capacitor can reduce the equivalent line reactance and hence increase the transmission capability.

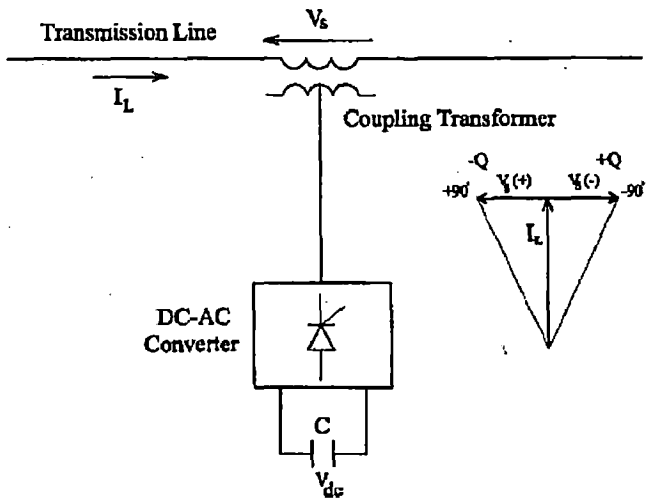


Figure 1.9: General Diagram of the Static Synchronous Series Compensator (SSSC)

This can be performed by injecting a series boosting voltage across the line which lags the line current by 90^0. In Figure 1.9, V_s is essentially in quadrature with I_L and by controlling the magnitude of V_s series line reactance compensation can be adjusted. Since V_s is in quadrature with I_L there is no real power exchange between the SSSC and the transmission line. It should be noted that if V_s leads line current by 90^0, inductive series compensation will be obtained [14].

1.4 CONTRIBUTIONS AND THESIS OUTLINE

Before presenting the thesis outline an brief literature review of voltage-source converter-based FACTS (VSC-FACTS) is presented.

The possibility of generating controllable reactive power without the use of Ac capacitor or reactor banks by various switching power converters was disclosed by Gyugyi in 1979 [15]. Edwards *et al.* reported the operation of a ± 1 MVA prototype advanced static Var generator (ASVG) in 1988 [16]. They used a 12-pulse converter scheme to test the operation of a STATCOM. The control fundamental of VSC-FACTS was developed by Schauder and Mehta in 1991 [17]. They developed a decoupled control theory of VSC-FACTS by Park transformation which is the basic control approach in switching type FACTS controllers. The concept of solid-state series compensation without using series capacitors or reactors was introduced by Gyugyi in 1989 [13]. The operation of the SSSC was introduced in 1994 [18] and 1996 [14] by Gyugyi, Schauder and K.Sen.

After developing the basic theory, control and operation of the STATCOM and SSSC by FACTS pioneers in late 1980s and mid 1990s, numerous papers have been published for further control development and validation of the STATCOM and SSSC by digital simulation. The previous investigations and simulations have been performed using either mathematical model of the STATCOM and SSSC [17], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], or a low-pulse converter such as a 6 or 12-pulse converter [31], [32], [33]. The mathematical model, which is usually a simple Laplace domain model, does not represent the exact physical model of the converter and therefore some key aspects of the practical operation such as transient operation, harmonic contents and inherent delays can not be considered which are important in practical applications. The low-pulse converters have the problems of high harmonics contents and are never used in practical FACTS applications and therefore can not be used for in-depth and accurate investigations and simulation of the interconnected power system and FACTS.

The thesis investigated the theory, control, complete digital simulation and design of two novel controllers for the STATCOM and SSSC. The basic theory and control of the

STATCOM and SSSC will be presented in Chapter 2. For full validation and digital simulation purposes a 24-pulse GTO converter with all the required magnetic circuit was modeled. The lowest harmonic content of this converter is of 23th order and therefore is quite acceptable in FACTS applications. Since Pulse Width Modulation (PWM) methods are limited to low and medium voltage power converters, this converter simulates that exact practical approach in large FACTS implementation.

A complete and exact digital simulation of the STATCOM will be presented in Chapter 3 which includes all practical concepts such as using a 24-pulse converter, regulations slope and decoupled control. An exact and complete digital simulation of the SSSC will be presented in Chapter 4 using a 24- pulse converter.

After developing the models of the STATCOM and SSSC, their control and dynamic performance is investigated in great details. It also presents an in-depth investigation of the STATCOM stability. In order to stabilize the STATCOM under various power system operating conditions an Automatic Gain Controller (AGC) is designed and validated by digital simulation. The AGC is a powerful tool to ensure stable operation of the STATCOM.
Dynamic operation of the SSSC is investigated. A new supplementary regulator is designed to enhance the transient operation of the SSSC. The exact modeling of the SSSC made it possible for this in-depth investigation, as the mathematical modeling can not lead to the presented results.

The MATLAB Power System Blockset (PSB) of Simulink was utilized for the complete digital simulation of both the STATCOM and SSSC. They provide a powerful tool to represent the power system and power electronic components such as GTOs as well as signal processing and control components.

2.0 OPERATION AND CONTROL FUNDAMENTALS

The Static Synchronous Compensator (STATCOM) and the Static Synchronous Series Compensator (SSSC) as the shunt and series Voltage-Source Converter-Based FACTS (VSC-FACTS) devices were introduced in Chapter 1.

In this chapter the basic operation and control strategy of the STATCOM and SSSC is presented. The control of VSC-FACTS is based on d-q transformation and decoupled control. Therefore the concept of direct and quadrature axes and Park Transformation is presented. The basic component of VSC-FACTS is a converter capable of generating a three phase, almost sinusoidal voltage. The design fundamentals of a 24-pulse GTO converter, as one of the best choices for power quality reasons, are explained and the complete Matlab/Simulink digital simulation using Power System Blockset (PSB) is presented. This 24-pulse converter is the basic building block of the STATCOM and SSSC and will be used for digital simulation of them in the next chapters.

2.1 STATIC SYNCHROUNOUS COMPENSATOR (STATCOM)

Shunt compensation is well-known concept in AC power systems to control the reactive power flow and hence regulate the bus voltage. As explained in Chapter 1 when the real power demand of the load increases the amount of the required reactive power also increases and shunt compensation is required to provide this additional reactive power demand.

The IEEE definition of the STATCOM is [1]:

STATCOM: *A static synchronous generator operated as a shunt-connected static Var compensator whose capacitive or inductive output current can be controlled independent of the AC voltage system.*

Figure 2.1 shows the basic diagram of the STATCOM. Basically, the STATCOM is a Synchronous Voltage Generator (SVG) that generates a three phase voltage from a dc source in synchronism with the line voltage. The magnitude of the STATCOM voltage can be controlled in order to adjust the amount of reactive power exchange between the STATCOM and the controlled transmission system. Therefore in Figure 2.1, V_s is in phase with V_t and there is no real power exchange between the STATCOM and the transmission system.

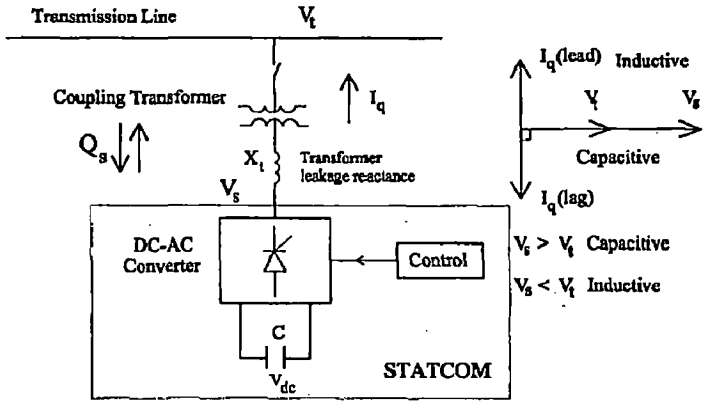


Figure 2.1: Static Synchronous Compensator

However, there is usually a small amount of converter switching and coupling transformer losses that should be supplied by the transmission system. Since V_s and V_t are in phase, the STATCOM current is essentially in quadrature with bus voltage, V_t , and the STATCOM voltage, V_s ,and therefore it is a reactive current, Iq. The magnitude of Iq and the corresponding reactive power exchange between the STATCOM and the transmission system in per unit are:

$$| I_q | = \frac{V_s - V_t}{X_t} \tag{2.1}$$

$$Q_s = V_s I_q = \frac{V_s^2}{X_t}(1 - \frac{V_t}{V_s}) \tag{2.2}$$

If $V_s > V_t$, the STATCOM operates in capacitive mode and supplies reactive power into the transmission system and if $V_s < V_t$, the STATCOM operates in inductive mode and consumes reactive power from the transmission system.

The power rating of the STATCOM depends on the required reactive power compensation at the point of connections. The load flow calculations determine the unregulated bus voltage and how much reactive power is needed to regulate the bus voltage. By knowing the STATCOM power and voltage ratings, the voltage and current ratings of the GTO's can also be determined.

2.1.1 Voltage-Source Converter Operation

The basic building block of the STATCOM is converter that generates a synchronous sinusoidal voltage. For operational, control and economical reasons Voltage-Source Converters (VSC) are currently employed in FACTS applications [1].

The most practical and economical configuration that is currently used and recommended in high power utility applications is multiphase converters. The details of a multiphase converter will be presented later in this chapter. However, the mechanism by which the converter internally generates reactive power can be explained without considering the detailed operation of the solid-state switches, and only by considering the input and output powers of the converter [18]. The key to this explanation resides in the physical fact that since there is no source of internal energy in the converter, the net instantaneous power at the AC output terminals (assuming no switching losses of the converter). If the converter is operated to supply only reactive power, the real power provided by dc capacitor is zero. Furthermore since reactive power at zero frequency (capacitor voltage) is by definition zero, the dc capacitor plays no part in the reactive power generation. In other words, the reactive power is generated only due to interconnection of the AC phases by the converter in such a way that the reactive current of the AC system can flow freely between the phases. However, although reactive power is internally generated by the action of solid-state switches, it is still necessary to have a

relatively small dc capacitor across the terminals of the converter. The need for the dc capacitor is primarily required to satisfy the equality of the instantaneous input and output powers of the converter. The output voltage waveform of the converter is not a perfect sine wave. However the multipulse converter injects a smooth almost sinusoidal current through the tie reactance to the transmission system. As a result the net three phase *instantaneous* power (VA) at the output terminals of the converter has reduced ripple content. Thus in order no to violate the equality of the instantaneous powers, the converter must draw a fluctuating current from the dc capacitor. The presence of the input ripple current components is thus entirely due to the ripple components of the output voltage, which are a function of the output wave form fabrication technique. In a high power converter, using sufficiently high pulse number, the output voltage distortion and capacitor current can be theoretically reduced to any desired value. Thus a perfect converter would generate sinusoidal output voltage and draw pure dc input current without harmonics. In practice due to system unbalance and other imperfections, as well as to economic considerations, these ideal conditions are not achieved, but approximated satisfactorily by converters of sufficiently high pulse numbers (24 or higher). For economical and hardware assembly reasons, 24-pulse or higher converters are usually employed in electric Utility Grid.

2.1.2 Basic Control of the STATCOM

As mentioned earlier, the STATCOM voltage, V_s, is always in phase with transmission line voltage, V_t, and by fast control of the magnitude of V_s the reactive power exchange can be regulated according to compensation level. Since two level, multipulse converters are the most practical and economical converters in FACTS applications, this section deals with this type of converters.

Unlike the PWM and three level converters, two level converters do not have internal capability of voltage magnitude control and only the phase angle of the output AC voltage can

be regulated by gating signals. Therefore the only way to control the magnitude of the AC output voltage is by adjusting the input DC voltage should increase and vice-versa. In other words charging or discharging the dc capacitor voltage control is achieved by a small phase displacement, $\Delta\alpha$, between the STATCOM voltage, V_s, and the transmission system voltage, V_t. If V_s lags V_t, real power flows from transmission system to dc side and the capacitor is charged. Similarly if V_s leads V_t, real power flows from the dc side to the transmission system and the capacitor is discharged. Therefore the real power exchange is a function of phase displacement, $\Delta\alpha$, as shown in Figure 2.2.

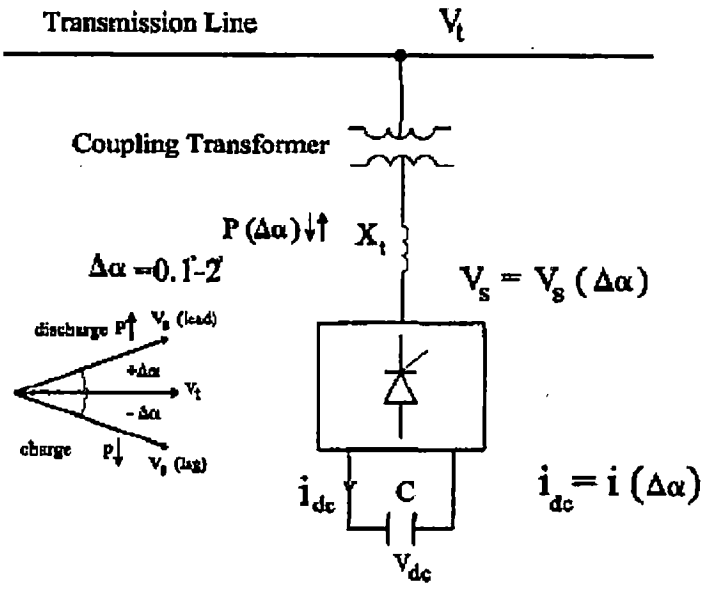


Figure 2.2: Real Power Exchange of the STATCOM

This phase displacement is also required to compensate the converter switching losses by the transmission system. In practice, V_s always lags V_t by a small value (0.1^0-2^0) and a small real power flows from the transmission system to dc capacitor in order to compensate the converter switching and transformer losses. Additional temporary positive or negative phase displacement is required to charge or discharge the capacitor as apart of additional control system requirements.

2.1.3 Vector Control Analysis

The concept of vector control of the VSC-FACTS was developed by Schauder and Mehta [17]. A decoupled control is obtained by using the Park transformation. The AC output current iof the STATCOM can be considered as a two-component current vector. The major part of the current is reactive current and performs the basic function of the STATCOM. Besides, a small portion of the current is real current that compensates for converter switching losses and charges or discharges the dc capacitor. Therefore if the STATCOM current is decomposed into real and reactive components, a decoupled control can be obtained which makes the STATCOM control simple.

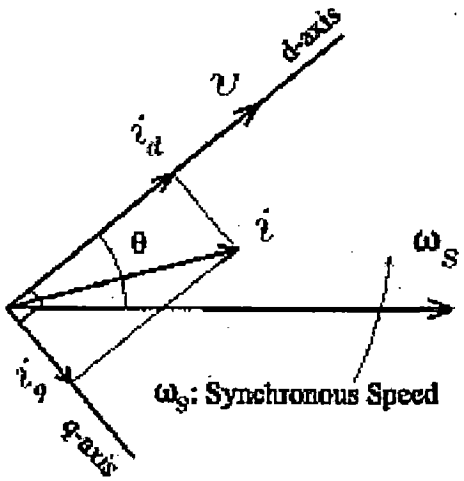


Figure 2.3: Direct and Quadrature Components of Current Vector

In general using the Park transformation, asset of three phase, symmetric variables can be decomposed into direct and quadrature components, also known as d-q transformation. Figure 2.3 shows d-q components of a current vector with respect to a reference voltage vector. The direct and quadrature coordinates within this synchronously rotating reference frame are given by the following time-varying transformation, which is called Park or d-q transformation [17]:

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - 120°) & \cos(\theta + 120°) \\ -\sin\theta & -\sin(\theta - 120°) & -\sin(\theta + 120°) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2.3)$$

Where i_a, i_b and i_c are the three phase currents, i_d and i_q are the direct and quadrature components of current vector with respect to the rotating reference and θ is the phase angle of the rotating reference. I_0 is the zero component of the current vector and for a symmetric three phase variable, is always zero. Under balanced, steady-state conditions, the coordinates of the voltage and current vectors in the synchronous reference frame are constant quantities. This feature is useful for decoupled control strategy of the VSC-FACTS.

By using this transformation and considering the transmission system voltage, V_s, as the rotating reference vector, the STATCOM current can be decomposed into direct axis component, which is in phase with V_t, and quadrature axis component, which is in quadrature with V_t. The d-axis current is the real current and compensates the converter switching and coupling transformer losses as well as charges or discharges the dc capacitor. The q-axis current is the reactive current and performs the basic operation of the STATCOM which is generation or absorption of reactive power.

2.1.4 Reference Signal and Regulation Slope

Since the basic purpose of the STATCOM is to regulate the transmission system voltage by reactive power compensation, line voltage, V_t, is the basic reference signal for the control of the STATCOM operation. It provides an external reference value for the STATCOM control.
In many applications the STATCOM is not a perfect voltage regulator, i.e. it does not provide a fixed voltage for the transmission system, instead, a regulation slope is considered for the voltage and it is allowed to be less than the nominal voltage at full capacitive operation and

higher than the nominal voltage at full inductive operation of the STATCOM. The reasons are [1]: (1) A practical STATCOM has maximum capacitive and inductive current ratings. The linear operation range of the STATCOM can be extended if a regulation slope is allowed. (2) Perfect regulation (zero slope) could result in poorly defined steady state operating point and a tendency of oscillations. (3) A regulation slope tends to enforce automatic load sharing between static compensators, as well as other regulator devices in the grid.

A typical regulation characteristic of the STATCOM is shown in Figure 2.4. The regulation slope, *k*, is defined as:

$$\kappa = \frac{\Delta V_{Cmax}}{I_{Cmax}} = \frac{\Delta V_{Lmax}}{I_{Lmax}} \tag{2.4}$$

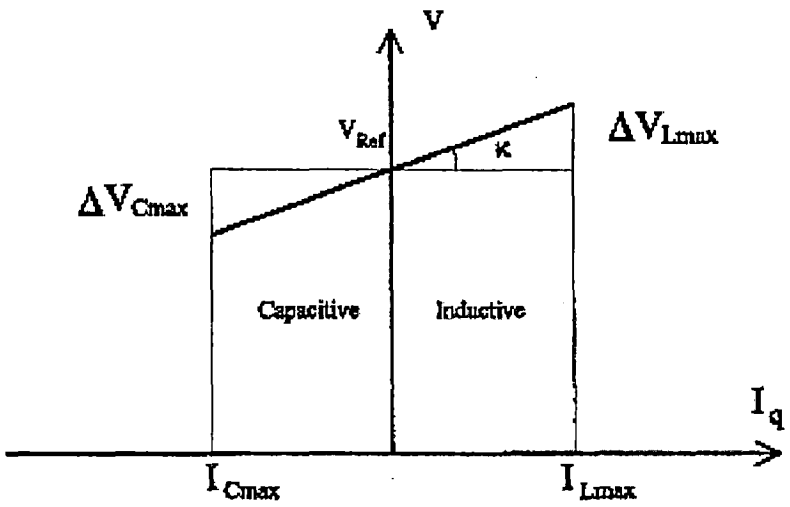


Figure 2.4: Voltage Regulation and Regulation Slope

Where ΔV_{Cmax} is the maximum line voltage drop at full capacitive and ΔV_{Lmax} is the maximum overvoltage at full inductive operation of the STATCOM. I_{Cmax} and I_{Lmax} are the corresponding STATCOM current ratings. The reference voltage with regulation slope, V^*_{Ref}, will be:

$$V^*_{Ref} = V_{Ref} + \kappa I_q \tag{2.5}$$

I_{Lmax} and I_{Cmax} are determined by the STATCOM Var capacity. Depending on the maximum capacitive or reactive power compensation, I_{Lmax} and I_{Cmax} can be determined. The voltage regulation of the STATCOM is linear if the required compensation current is between I_{Cmax} and I_{Lmax} and beyond these currents it is no longer linear and additional capacitive or reactive compensation by parallel capacitor or reactor banks can be added to meet the compensation requirements.

2.1.5 STATCOM Decoupled Control Strategy

As stated earlier, the magnitude and angle of the ac output voltage are the internal parameters of the STATCOM that determine the real and reactive power exchange and therefore control the operation of the STATCOM, while the transmission system voltage is the external reference signal.

In order to synchronize the STATCOM voltage, V_s, with the line voltage, V_t, a Phase-Locked Loop (PLL) system is required. PLL provides the phase angle of the STATCOM bus voltage, θ. This angle is also required for d-q transformation of the STATCOM current. Figure 2.5 shows the control structure of the STATCOM.

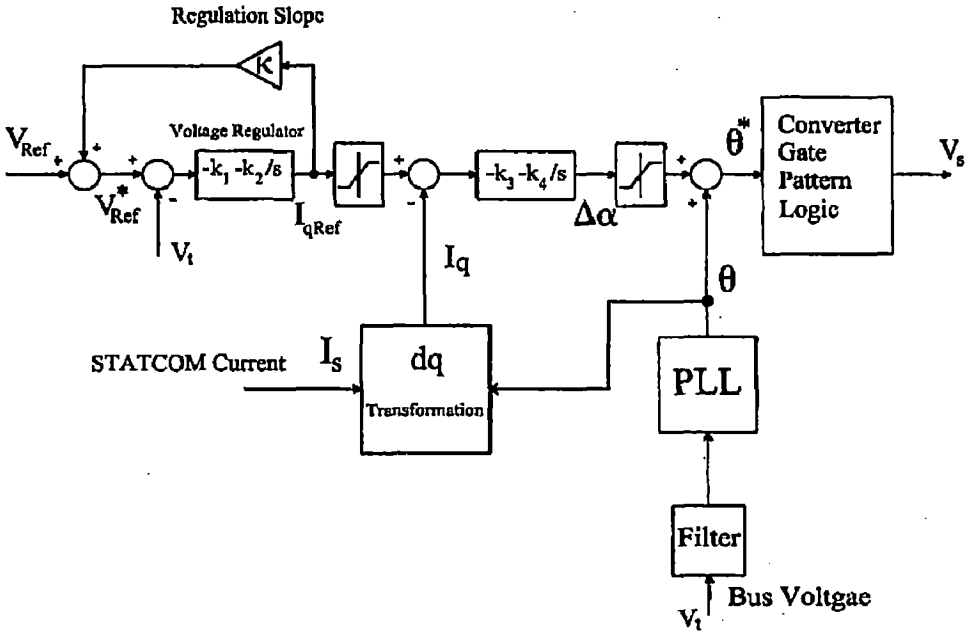


Figure 2.5: Decoupled Control Structure of the STATCOM with Regulation Slope

Transmission system voltage is compared with the reference voltage, V_{Ref} and the voltage regulator, which is a PI controller, determines the required STATCOM q-axis current, I_{qRef}, which should be limited to the STATCOM ratings. PLL system provides the basic synchronization signal, θ, and the STATCOM q-axis current is compared with I_{qRef}. A PI controller determines the required phase displacement, $\Delta\alpha$, in order to charge or discharge the dc side capacitor. The phase angle θ^* is the phase of the AC output voltage. If $\Delta\alpha$ is negative, STATCOM voltage lags V_t and real power flows from the transmission system to the STATCOM and the dc capacitor is charged in order to make V_s higher. If $\Delta\alpha$ is positive, real power flows from the STATCOM to the transmission system and the dc capacitor is discharged in order to make V_s lower.

2.2 STATIC SYNCHRONOUS SERIES COMPENSATOR (SSSC)

The series device of VSC-FACTS is the SSSC and it is basically a Synchronous Voltage Generator (SVG) that generates a three phase voltage in quadrature with the transmission system current. The IEEE definition of the SSSC is [1]:

Static Synchronous Series Compensator: *A static synchronous generator operated without an external energy source as a series compensator whose output voltage is in quadrature with an controllable independently of the line current for the purpose of increasing or decreasing the overall reactive voltage drop across the line and thereby controlling the transmitted electric power.*

It is well-known that a series capacitor cancels a portion of the line series reactance and therefore increases the power transfer capacity of the transmission line as well as transient and steady-state stability limits. Figure 2.6 (a) shows a simple two-machine transmission system with capacitive series compensation and the corresponding phasor diagram in Figure 2.6 (b).

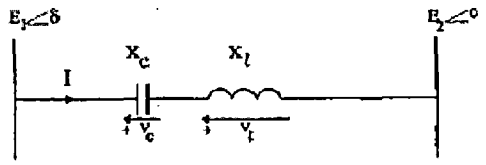


Figure 2.6: (a)Capacitive Series Compensation

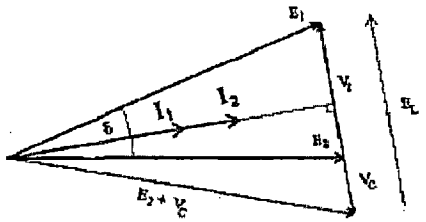


Figure 2.6: (b) Phasor Diagram

From the phasor diagram, the effect of series capacitor can be seen as a voltage source whose voltage, V_c, is in opposite with the voltage drop of the line reactance, V_l. Therefore the total driving voltage, (E_L=E_1-E_2- V_c), increases and hence the line current increases as well [14]. By this explanation the physical nature of the series element is irrelevant as long as it produces the desired compensating voltage. Therefore the compensating element may be considered as an ac voltage source which directly injects as voltage, V_c, in quadrature with the line current and in series the transmission system as shown in Figure 2.7 (a).

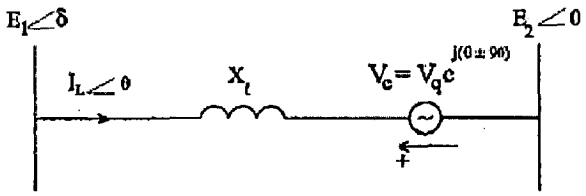
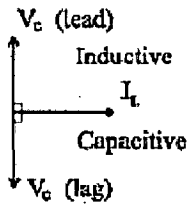


Figure 2.7: (a) Synchronous Series Compensation



(b)

Figure 2.7: (b)Phasor Diagram

If V_c lags the line current by 90^0, a capacitive series compensation is obtained and if V_c leads the line current by 90^0, an inductive series compensation is obtained.

2.2.1 Effect of Capacitive Series Compensation on the Power Flow

The effect of capacitive series compensation on real power flow in a transmission system can be investigated analytically by assuming $|E_1| = |E_2| = E$ in Figure 2.7. The equations for real and reactive power flow without series compensation, as described in Chapter 1 are:

$$P = \frac{E^2}{X_l} \sin\delta \tag{2.6}$$

$$Q = -\frac{E^2}{X_l}(1 - \cos\delta) \tag{2.7}$$

The phasor diagram of the transmission system, when $|E_1| = |E_2| = E$ and V_c lags the line current by 90^0 is shown in Figure 2.8.

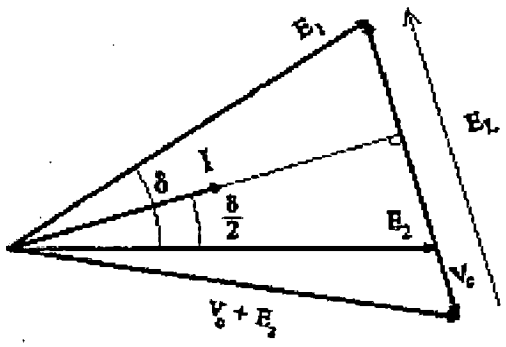


Figure 2.8: Phasor Diagram of Capacitive Synchronous Series Compensation

Since $|E_1| = |E_2|$ and I is perpendicular to EL, the phase angle of current vector is $\delta / 2$. The real and reactive power equations can be obtained as:

$$I = \frac{E\angle\delta - E - V_q\angle(\frac{\delta}{2} - \frac{\pi}{2})}{jX_l} \tag{2.8}$$

$$= \left(\frac{E\sin\delta + V_q\cos\frac{\delta}{2}}{X_l}\right) + j\left(\frac{E - E\cos\delta + V_q\sin\frac{\delta}{2}}{X_l}\right) \tag{2.9}$$

$$E_2 I^* = \left(\frac{E^2\sin\delta + EV_q\cos\frac{\delta}{2}}{X_l}\right) + j\left(\frac{E^2\cos\delta - E^2 - EV_q\sin\frac{\delta}{2}}{X_l}\right) \tag{2.10}$$

$$P_{new} = \frac{E^2}{X_l}\sin\delta + \frac{EV_q}{X_l}\cos\frac{\delta}{2} = P_{old} + \Delta P \tag{2.11}$$

$$Q_{new} = -\frac{E_2}{X_l}(1 - \cos\delta) - \frac{EV_q}{X_l}\sin\frac{\delta}{2} = Q_{old} + \Delta Q \tag{2.12}$$

Where δ is the phase angle between the two bus voltages. Comparing with equations 2.6 and 2.7, the transmitted real power is increased by $(\frac{EV_q}{X_l}\cos\frac{\delta}{2})$ and the transmitted reactive power is increased by$(\frac{EV_q}{X_l}\sin\frac{\delta}{2})$. The additional real power is a function of the magnitude of the injected series voltage, V_q, and is limited by the series device Var capacity.

2.2.2 Voltage-Source Converter-Based SSSC

The basic building block of the SSSC is a voltage-source converter that is capable of generating a synchronous three phase voltage. Like the STATCOM, two level, multiphase converter is the most practical and economical converter for the SSSC.

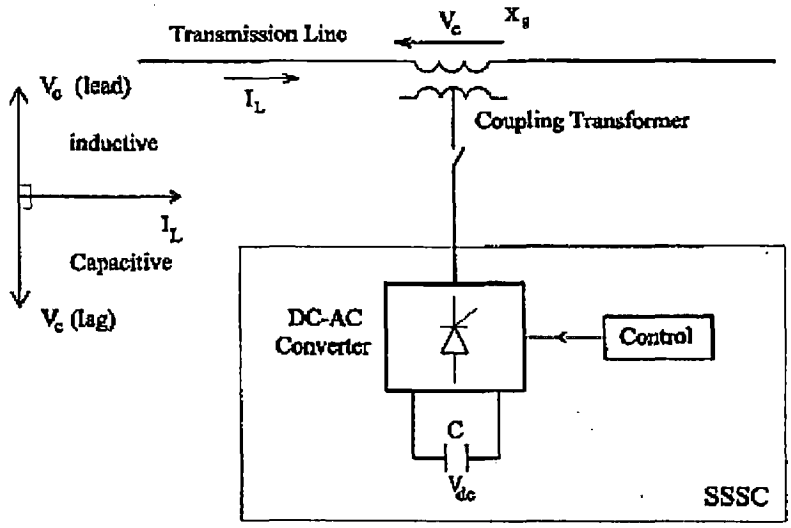


Figure 2.9: Static Synchronous Series Compensator

Figure 2.9 shows the basic diagram of the SSSC. V_c is in quadrature with line current, I_L, there is no real power exchange between the SSSC and the transmission system. There are two operating modes: If V_c lags by I_L by 90^0, capacitive series compensation is obtained and inductive series compensation is obtained if V_c leads the line current by 90^0.

The power and voltage ratings of the SSSC depend on the required series injected reactance, X_s, and the transmission line current. The required X_s is obtained from the power flow calculations and is usually less than 50% of the series line reactance.

For a higher transmission line current a bigger SSSC voltage and thus more reactive power is required. By knowing the range of X_s and the transmission line current, the required SSSC voltage and power can be calculated.

2.2.3 Basic Control Scheme of the SSSC

The main function of the SSSC is to control the real power flow. This can be accomplished either by direct control of the line current (power) or alternatively by indirect control of either the compensating impedance, X_s , or the compensating voltage, Vc [1]. The direct power flow control has the advantage of maintaining the transmitted power in a closed loop manner by the defined reference. However, under some network contingency, the maintenance of the constant power flow may not be either possible or even desirable. Therefore in some applications the impedance (or voltage) control that maintains the impedance characteristic of the line may be preferred from the operating standpoint. The degree of series impedance compensation, S, is usually expressed as the ratio of the series injected reactance, X_s, to the line reactance, X_l , i.e. $S = X_s / X_l$. Therefore for a capacitive series compensation, the line series reactance is $X_{Line} = X_l - X_s$, where $X_s = SX_l$. Similarly, for an inductive series compensation, the line series reactance is $X_{Line} = X_l + X_s$, where $X_s = SX_l$. The basic function of tehcontrol system is to keep the SSSC voltage, V_c, in quadrature with the line current, I_L, and the control the magnitude of

V_c to meet the compensation requirement, which the degree of series compensation. The control structure of the SSSC is shown in Figure 2.10.

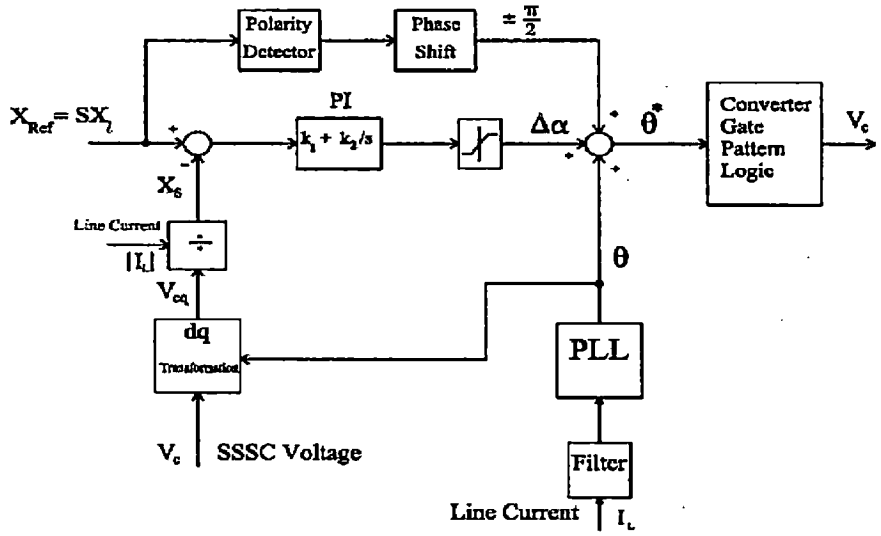


Figure 2.10: Control Structure of the SSSC

The basic synchronization signal, θ, is the phase angle of line current. The SSSC injected impedance is measured as the ratio of q-axis voltage of the SSSC, V_{cq}, to the magnitude of the line current, I_L. This impedance is then compared with the reference compensation impedance, SX_l. A PI controller generates the required phase displacement, Δα, in order to charge or discharge the dc capacitor. A negative Δα yields to the real power flow from the transmission system to the SSSC and charges the dc capacitor, while a positive Δα discharges the dc capacitor. When X_{Ref} is negative, V_c lags I_L by 90^0 plus Δα (capacitive compensation) and when it is positive V_c leads I_L by 90^0 plus Δα (inductive compensation). The final output of the control system is the phase angle of the SSSC output voltage, θ^*.

2.3 DESIGN AND SIMULATION OF A 24-PULSE CONVERTER

It was explained that the two level, multipulse converter as given in 1.3.2 is the most practical and economical converter in the STATCOM and SSSC applications. Figure 2.11 shows the configuration of the three phases, voltage-source, 6-pulse, GTO converter. The gating pulses of the GTOs are such that each is closed for 180^0.

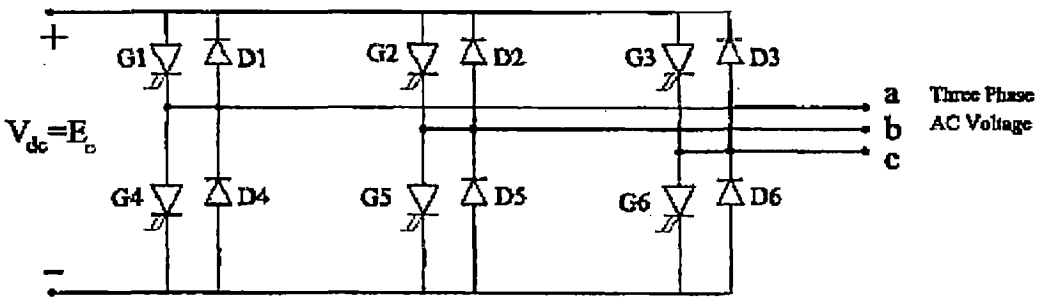


Figure 2.11: Three Phase, 6-Pulse, Voltage-Source GTO Converter

G2 is closed 120^0 after G1 and G3, 120^0 after G2. When a switch in one leg is closed, the other one is open and vice versa. The diodes are to provide current path during the interval that a switch is closed and the inductive load current is not zero [34].

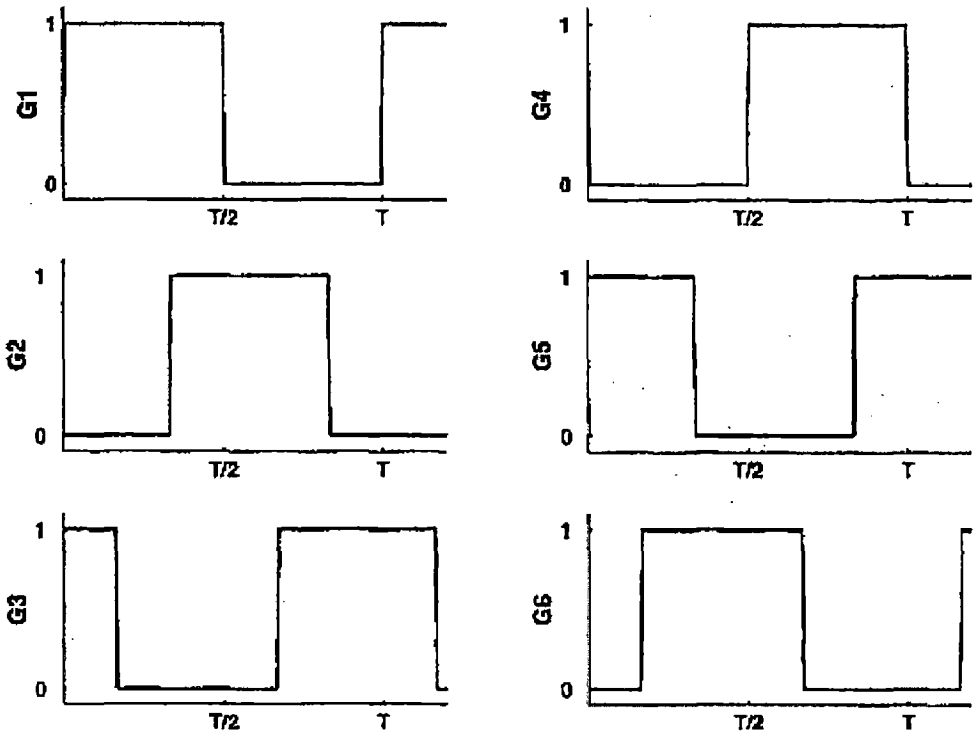


Figure 2.12: Gating Pulses of the 6-Pulse Converter

Figure 2.12 shows the gating pulses of the basic 6-pulse converter, generated by the Simulink. Figure 2.13shows the phase to neutral and phase to phase voltages of the 6-pulse converter. The Fourier expansion of phase to neutral voltage, V_{an}, is:

$$V_{an} = \frac{2E_o}{\pi}(\sin\omega t + \frac{1}{5}\sin 5\omega t + \frac{1}{7}\sin 7\omega t + \frac{1}{11}\sin 11\omega t + \cdots) \tag{2.13}$$

Where E_o is the dc source voltage. Equation 2.13 can be written as:

$$V_{an} = \sum_{n=1,5,7,11,\ldots} \frac{2E_o}{n\pi}\sin n\omega t \tag{2.14}$$

Similarly the Fourier expansion of phase-phase voltage, V_{ab}, is:

$$\begin{aligned} V_{ab} &= \frac{2\sqrt{3}E_o}{\pi}[\sin(\omega t + \frac{\pi}{6}) - \frac{1}{5}\sin 5(\omega t + \frac{\pi}{6}) \\ &\quad -\frac{1}{7}\sin 7(\omega t + \frac{\pi}{6}) + \frac{1}{11}\sin 11(\omega t + \frac{\pi}{6}) + \cdots] \end{aligned} \tag{2.15}$$

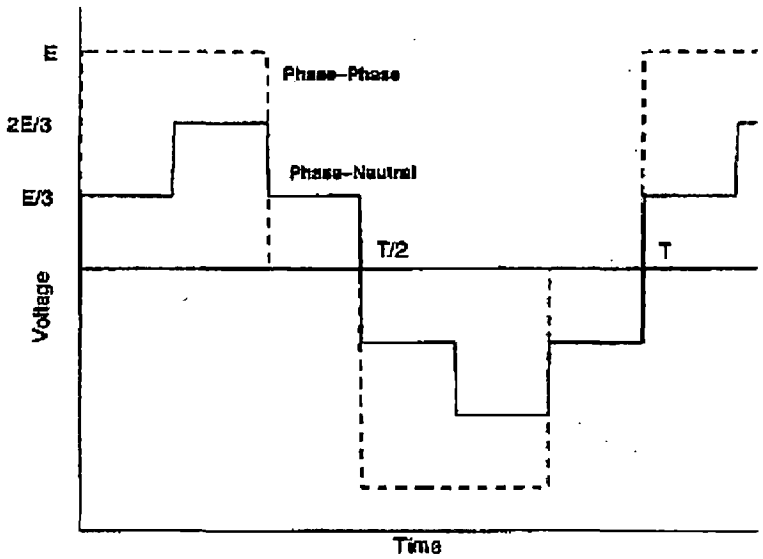


Figure 2.13: Phase-Neutral and Phase-Phase Voltages of the 6-Pulse Converter

Which can be written as:

$$V_{ab} = \sum_{n=1,5,7,11,\ldots} \frac{4E_o}{n\pi}\cos\frac{n\pi}{6}\sin n(\omega t + \frac{\pi}{6}) \tag{2.16}$$

It can be seen that V_{ab} is phase shifted by Π/6 and multiplied by √3 in comparison with Van.

Now shifting V_{ab} by - π/6 and dividing it by √3, then adding to V_{an} gives:

$$\frac{1}{\sqrt{3}}V_{ab}e^{-j\frac{\pi}{6}} + V_{an} = \frac{4E_o}{\pi}(\sin\omega t + \frac{1}{11}\sin 11\omega t + \frac{1}{13}\sin 13\omega t + \cdots) \qquad (2.17)$$

The importance of this process is that only 12k ± 1 harmonics exist in the resulting ac voltage, instead of 6k ± 1 harmonics in a 6-pulse converter and hence a 12-pulse converter is obtained with less harmonic distortion and a waveform closer to sinusoidal. One practical approach to obtain a 12-pulse converter is to combine two 6-pulse converters by two transformers as shown in Figure 2.14. Transformer T1 is a Y-Y transformer and is connected to converter1. The primary of transformer T2 is Δ connected in order to provide phase-phase voltage in the secondary. Gating pulses of converter 2 lag the pulses of converter 1 by 30^0, so that the required time shifting of phase-phase voltage of converter 2 is also multiplied by $1/\sqrt{3}$.

The harmonic contents of a 12-pulse converter may not be acceptable in many FACTS applications, so a 24-pulse converter may be desirable. The phase displacement between two consecutive 6-pulse converters in a multiphase converter configuration is $2\pi/6m$, where m is the total number of 6-pulse converters [30]. Therefore for a 24-pulse converter this phase displacement is 15^0. By combining four 6-pulse converters a 24-pulse converter can be obtained which only has 24k ± 1 harmonics and hence the lowest harmonic will be of 23th order. Figure 2.15 shows the configuration of a 24-pulse converter.

Converter 3 lags converter 1 by 30^0 and converter 4 lags converter 2 by 30^0. Hence converters 1 and 3 make a 12-pulse converter and converters 2 and 4 make the other 12-pulse converter. The two 12-pulse converts are combined to generate the desired 24-pulse voltage.

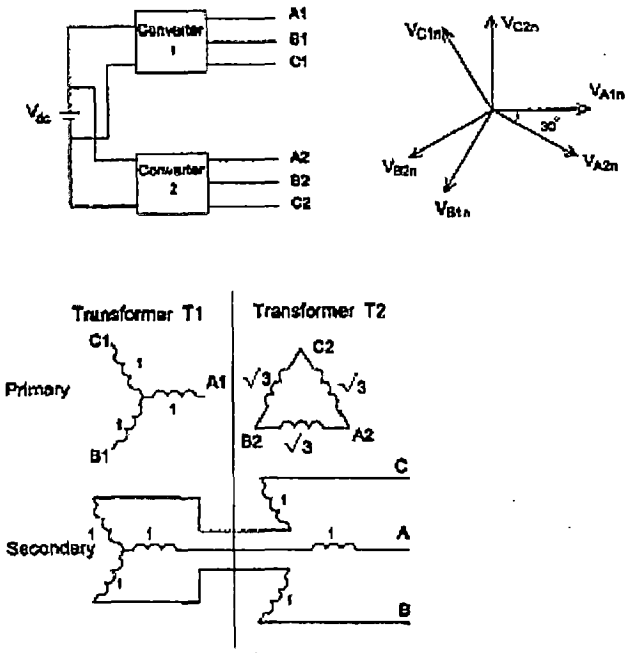


Figure 2.14: Configuration of a 12-Pulse Converter

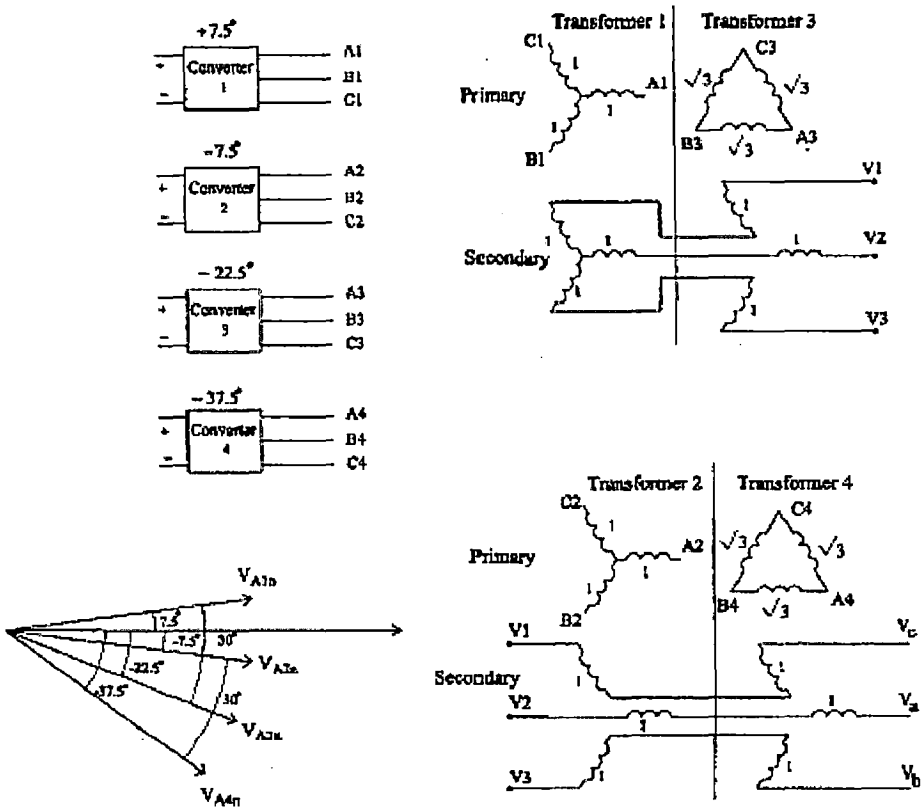


Figure 2.15: Configuration of a 24-Pulse Converter

2.3.1 Modeling and Digital Simulation

Simulink and Power System Blockset (PSB) of Simulink were used to implement a full digital simulation of 12 and 24-pulse converters. The configurations of Figures 2.14 and 2.15 were digitally simulated by Simulink/PSB in order to provide the basic building block of the STATCOM and SSSC that will be used in the next chapters.

Figure 2.16 shows the digital simulation of the 12-pulse converter voltage with the fundamental frequency of 60Hz. Similarly, the digital simulation of the 24-pulse converter voltage is shown in Figure 2.17. It should be noted that the 24-pulse converter was designed with variable phase angle and therefore the phase angle of the output ac voltage can be controlled which is a requirement for the STATCOM and SSSC applications.

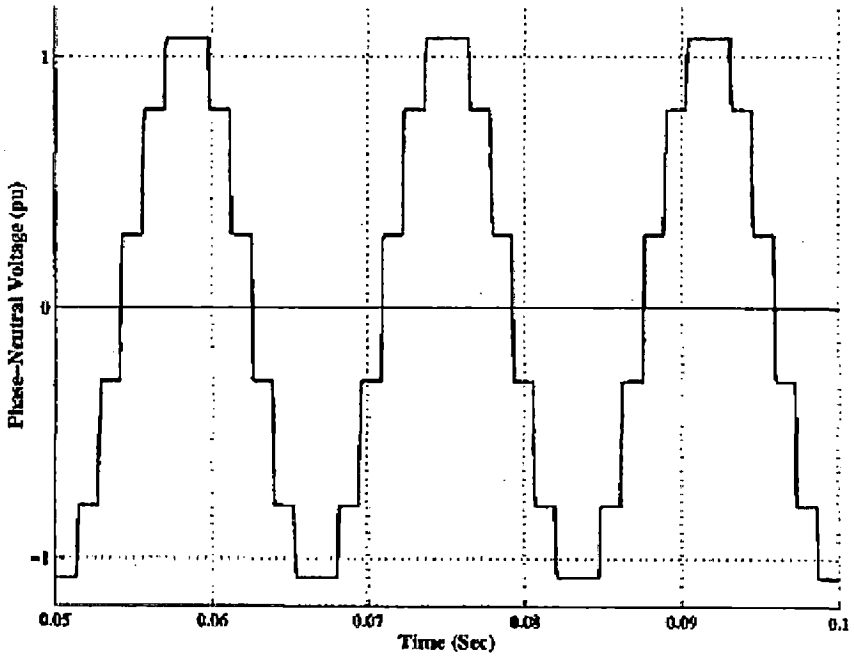


Figure 2.16: PSB Simulation of a 12-Pulse Converter

In order to measure the harmonic contents of the 24-pulse converter, Total Harmonic Distortion (THD) was measured by PSB model of the converter. Defining THD as:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \cdots + V_n^2}}{V_1} = \frac{V_h}{V_1} \qquad (2.18)$$

Where V_1 is rms value of the *i*th harmonic, V_h is rms value of total harmonic content and V_1 is rms value of fundamental harmonic. Figure 2.18 shows the THD measurement of the 24-pulse voltage. THD was measured to be 0.075. Since the total rms value of voltage, V_{rms}, is

$\sqrt{V_1^2 + V_h^2}$

and $V_h = 0.075V_1$, we conclude that:

$$V_{rms} = \sqrt{V_1^2 + V_h^2} = \sqrt{V_1^2 + (0.075V_1)^2} = 1.00280V_1 \qquad (2.19)$$

Or V_1 = 0.997Vrms. Thus it results in only 0.3% of ripple harmonic contents. Therefore the generated 24-pulse voltage at the ac side of the converter can be considered almost a sinusoidal waveform.

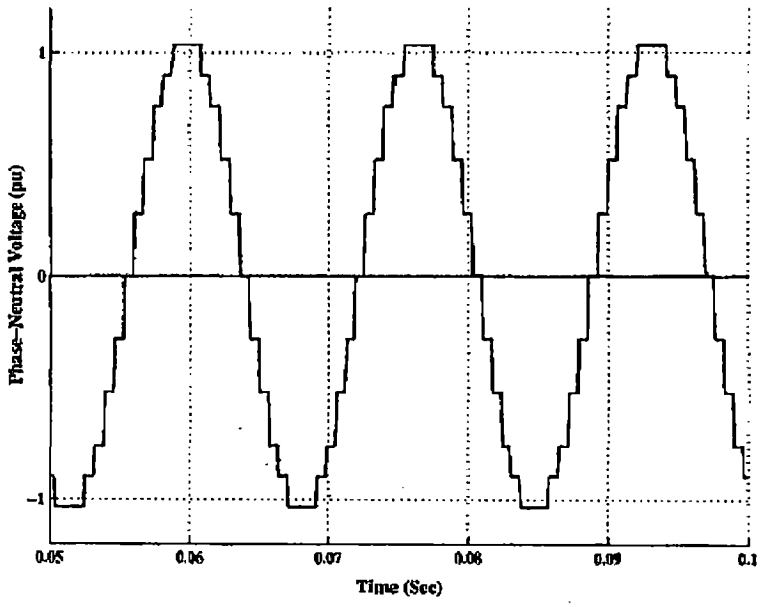


Figure 2.17: PSB Simulation of a 24-Pulse Converter

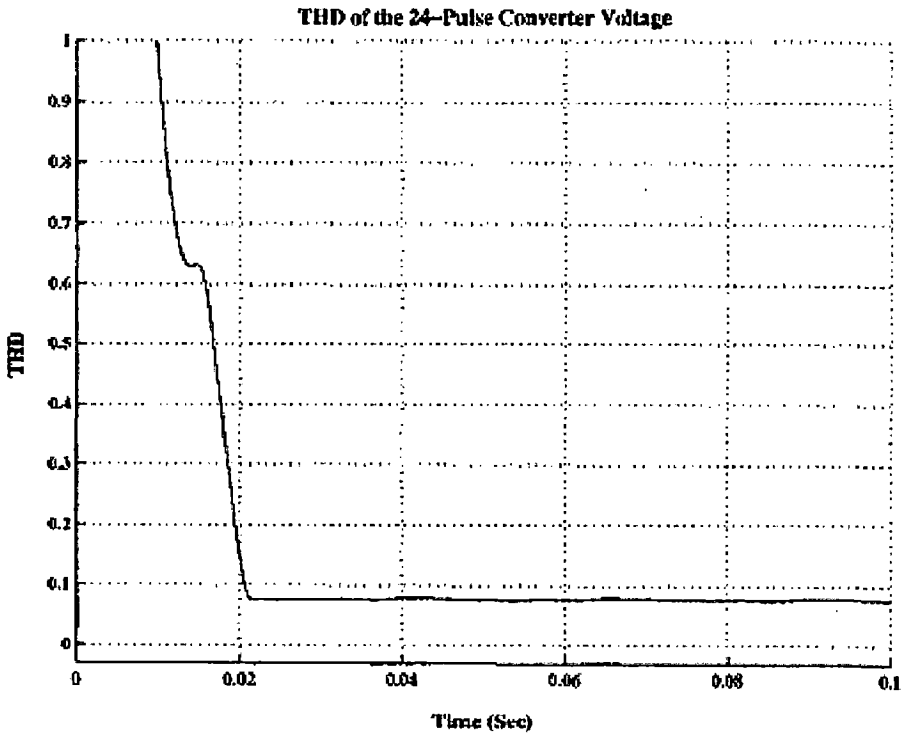


Figure 2.18: THD of the 24-Pulse Voltage

3.0 STATCOM: A COMPLETE DIGITAL SIMULATION STUDY

The operation and control fundamentals of the STATCOM were introduced in Chapter 2. A complete digital simulation of the STATCOM within a power system is presented in this chapter. The digital simulation is performed in MATLAB/Simulink environment using the Power System Blockset (PSB). The basic building block of the STATCOM is a 24-pulse converter whose complete digital simulation was presented in Chapter 2. The control process is based on a decoupled strategy using direct and quadrature components of the STATCOM current. The operation of the STATCOM is validated in both capacitive and inductive modes in a power transmission system.

3.1 POWER SYSTEM DESCRIPTION

The single line diagram of the sample power transmission system that will be used to validate the operation of the STATCOM is shown in Figure 3.1.

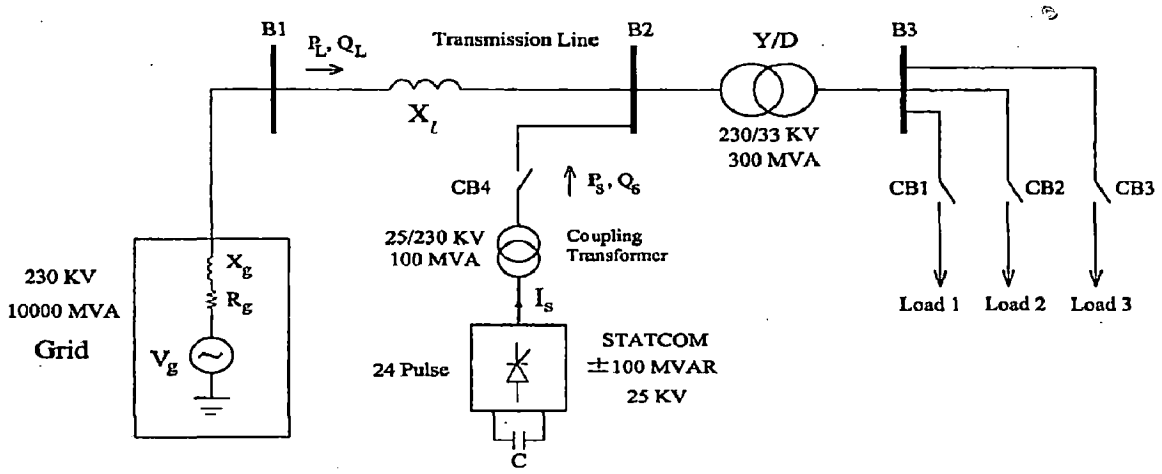


Figure 3.1: Single Line Diagram of the Power Transmission System with the STATCOM

The grid is represented by a 230KV source with 10000 MVA short circuit power with a resistance of 0.1 pu and a reactance of 0.3 pu.

The system parameters are as below:

(a) ***Transmission Line:***

- Reactance, X_l: 0.2 pu (230 KV, 300 MVA)

(b) ***Power Tranformers: (Y/Δ)***

- Rated Voltage: 230/33 KV
- Rated Power: 300 MVA
- Leakage Reactance: 0.01 pu

(c) ***STATCOM:***

- Type of Valves: GTO
- Number of Pulses: 24
- Nominal AC Voltage: 25KV
- Nominal DC Voltage: 2 KV
- Rated Power: ±100 MVAR
- GTOs Forward Resistance: $1m\ \Omega$

(d) ***Capacitor Bank(dc):***

- Total Capacitance: 10 mF
- Rated DC Voltage: 2 KV

(e) ***CouplingTransformer:(Y/Y)***

- Rated Voltage: 25/230 KV
- Rated Power: 100 MVA
- Resistance: 0.001 pu
- Leakage Reactance: 0.08 pu

3.2 CONTROL SYSTEM DESCRIPTION

The decoupled control structure was developed in Chapter 2 and is shown in Figure 3.2. The voltage regulator is a PI controller with $K_p = 0.004$ and $K_i = 3$.

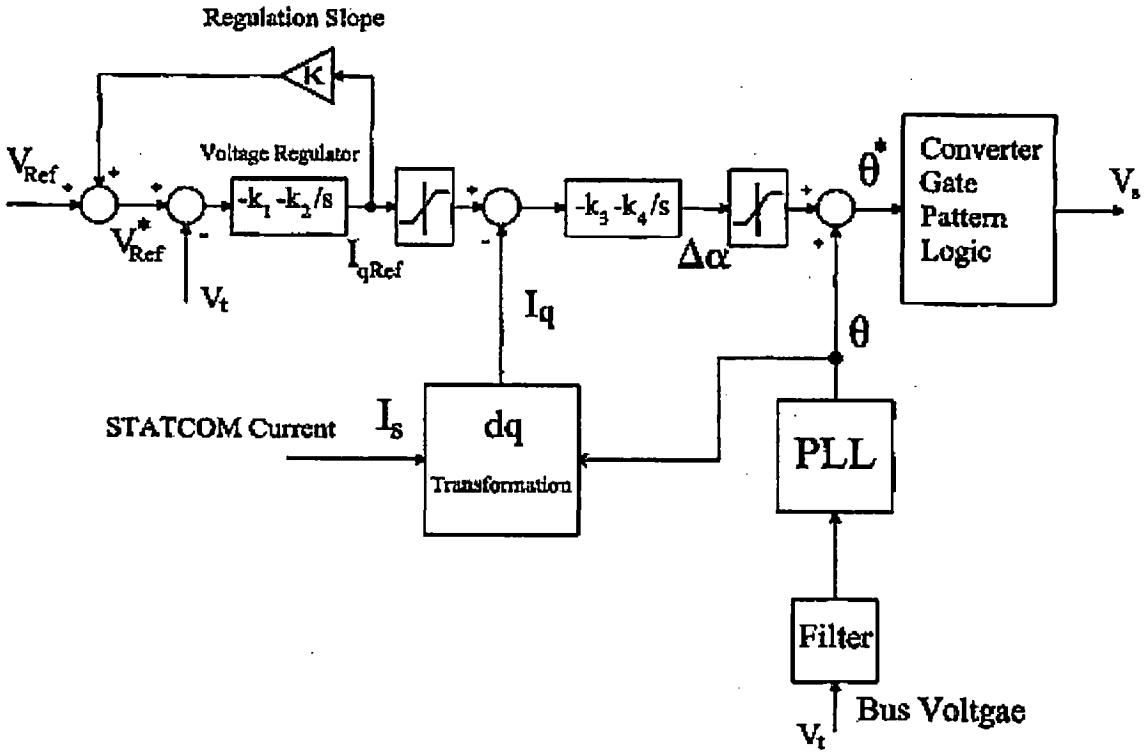


Figure 3.2: STATCOM Decoupled Control Structure

The current regulator is also a PI controller with Kp = 0.005 and Ki = 0.1. The Phase – Locked Loop (PLL) system generates the basic synchronizing signal which is the phase angle of the transmission system voltage, θ, and the regulation slope, *k*, determines the compensation behavior of the STATCOM.

3.2.1 Phase-Locked Loop

Since the operation of the STATCOM is totally dependent on the phase angle of the transmission line voltage (V_t), a precise and fast PLL system is required too generate the synchronizing signal, θ. The PLL that was designed is based on Digital Signal Processing (DSP) of the signal V_t. The zero crossing of V_t is obtained in every cycle and compared with

that of a reference voltage and the phase angle of V_t is obtained. Besides, the total time-varying phase angle of V_t, wt+ θ, is obtained that will be used in Park transformation.

3.2.2 Regulation Slope

As explained in Chapter 2 the regulation slope, *k*, is defined as:

$$\kappa = \frac{\Delta V_{Cmax}}{I_{Cmax}} = \frac{\Delta V_{Lmax}}{I_{Lmax}} \tag{3.1}$$

Where ΔV_{Cmax} is the maximum line voltage drop at full capacitive and ΔV_{Lmax} is the maximum line overvoltage at full inductive operation of the STATCOM, while I_{Cmax} and I_{Lmax} are the corresponding STATCOM currents. For the design purposes ΔV_{Cmax} was selected to be 9 KV. Since the STATCOM current is essentially a reactive current (neglecting the very small active current) the STATCOM power is essentially a reactive power. The STATCOM current at the high voltage side of the coupling transformer (I_{Cmax}) can be obtained from:

$$Q_s = \sqrt{3}\, V_t\, I_{Cmax} \tag{3.2}$$

Where Qs = 100 MVAR and V_t = 221 KV. Therefore:

$$I_{Cmax} = 261\ A\ (rms) \tag{3.3}$$

Since the control is based on decoupled strategy and q-axis current, for convenience, the regulation slope is defined based on I_q ($I_{qCmax} = \sqrt{2}\, I_{Cmax}$). Therefore the regulation slope is:

$$\kappa = \frac{\Delta V_{Cmax}}{I_{qCmax}} = \frac{9000}{261\sqrt{2}} = 24.3\ V/A \tag{3.4}$$

ΔV_{Lmax} and I_{qLmax} can be obtained from the following equations:

$$\kappa = \frac{\Delta V_{Lmax}}{I_{qLmax}} \tag{3.5}$$

$$Q_s = \sqrt{3}\,(230 + \Delta V_{Lmax})\,\frac{I_{qLmax}}{\sqrt{2}} \tag{3.6}$$

Where k = 24.3 V/A and Q_s = 100 MVAR. From the above equations ΔV_{Lmax} and I_{qLmax} are 8.3 KV and 242√2 A, respectively. In summary:

$$\Delta V_{Cmax} = 9\ KV \qquad \Delta V_{Lmax} = 8.3\ KV$$

$$I_{qCmax} = 261\sqrt{2}\ A \qquad I_{qLmax} = 242\sqrt{2}\ A$$

$$\kappa = 24.3\ V/A$$

3.3 DIGITAL SIMULATION

The STATCOM operation in Figure 3.1 was simulated in MATLAB/Simulink by using Power System Blockset (PSB). The basic building block of the STATCOM is a 24-pulse converter whose complete model in Simulink. PSB environment was developed in Chapter 2. In order to validate the operation of the STATCOM and the decoupled control strategy in the power system various combinations of loads were tested. The voltages, currents and powers were measured in Per Unit System. The base MVA is MVA_{base} = 100 and the base voltages are the rated voltages of the grid, transmission line, STATCOM, dc capacitor and the loads, respectively.

3.3.1 Simulation Results

The capacitor bank is pre charged to 1 pu voltage and the STATCOM is initially disconnected from the bus B2. The grid voltage, Vg, is 1.03 pu and only inductive load 1 with P = 1 pu and Q = 0.6 pu (at rated voltage) is in the system. Figures 3.3 and 3.4 show the simulation results. The B2 bus voltage is 0.97 pu for the uncompensated system and the real and reactive powers of the lines are P_L = 0.94 pu and Q_L = 0.56 pu. The simulation steps are explained below:

(i) t = 0.1 Sec

At this time the STATCOM is switched to the power system by closing the breaker CB4.As shown in Figure 3.3 (a) and (c) the STATCOM voltage lags the transmission line voltage by $\Delta\alpha = -0.45^0$ and therefore the dc capacitor voltage increases. The STATCOM is operating in capacitive mode and injects 0.29 pu of reactive power into the power system, as shown in Figure 3.2 (d). As the result, the B2 bus voltage increases to 0.99 pu (Figure 3.3(b)). The STATCOM draws 0.002 pu of real power from the grid to compensate switching and coupling transformer losses. Due to voltage regulation, the line transmitted real power was increased to PL = 0.98pu, while because of the STATCOM reactive power compensation, the transmitted reactive power was decreased to Q_L = 0.3pu. Figure 3.4(b) shows the d-q components of the STATCOM current and it can be seen that the STATCOM current is almost totally a reactive current.

(ii) t = 0.5 Sec

At this time inductive load 2 with P = 1 pu and Q = 0.7 pu (at rated voltage) is switched to the power system at bus B3. Since more reactive power compensation is required, the STATCOM voltage phase displacement increases to $\Delta\alpha = -1.2^0$ and therefore the dc capacitor voltage increases (Figures 3.2 (a) and (c)). Hence the converter voltage increases from 1.038 pu to 1.10 pu in Figure 3.4 (a). The STATCOM injects 0.77 pu of reactive power into the grid, while draws 0.012 pu of real power to compensate the losses. The regulated bus voltage is 0.97 pu. Figure 3.4 (b) shows that the STATCOM d-axis current temporarily increases in order to charge the dc capacitor. It can be verified that the STATCOM regulated the bus voltage according to the regulation slope. From Figure 3.4 (b) the STATCOM q-axis current is 0.8 pu. I_{qbase} can be obtained from $Q_s = \sqrt{3}V\frac{I_{qbase}}{\sqrt{2}}$, with Q_s = 100MVA and V = 230KV. Therefore I_{qbase} = 355A. The equation for the regulation slope, as explained in Chapter 2, is:

$$V^*_{Ref} = V_{Ref} + \kappa I_{qRef} \quad (3.7)$$

Where V_{Ref} = 230 KV, k =24.3 V/A and $I_{qRef} = 0.8I_{qbase}$ = 284A. Therefore V^*_{Ref} = 223.1 KV which is the same as the actual bus voltage at the specified value.

(iii) t = 1 Sec

At this time the capacitive load 3 with P = 0.3pu, Q_C = 0.35pu and Q_L = 0.08pu (at rated voltage) is switched to the power system. Since the capacitive load has a compensative effect on the grid, the STATCOM injects less reactive power into the system. This is achieved by reducing the dc capacitor voltage, with $\Delta\alpha = -0.98^0$ (Figure 3.3 (a)), and as a result the converter voltage drops to 1.08 pu (Figure 3.4 (a)). The regulated bus voltage is 0.975 pu while the STATCOM injects 0.65 pu of reactive power into the system and draws 0.009 pu real power. Figure 3.4 (b) shows that the STATCOM q-axis current decreases.

(iv) t = 1.5 Sec

At this time loads 1 and 2 are rejected (a major disturbance) and only the capacitive load 3 remains in the power system. Since the load is capacitive, the STATCOM operates in inductive mode to regulate the overvoltages at bus B2. The dc capacitor voltage drops below 0.9 pu, with $\Delta\alpha = 0.38^0$, i.e. the STATCOM voltage leads the bus voltage. As a result the converter voltage drops to 0.96 pu. The regulated bus voltage is 1.01 pu while the STATCOM draws 0.29 pu reactive power from the grid (inductive operation). Figure 3.4 (b) shows that since the STATCOM operates in inductive mode, the q-axis current is positive.

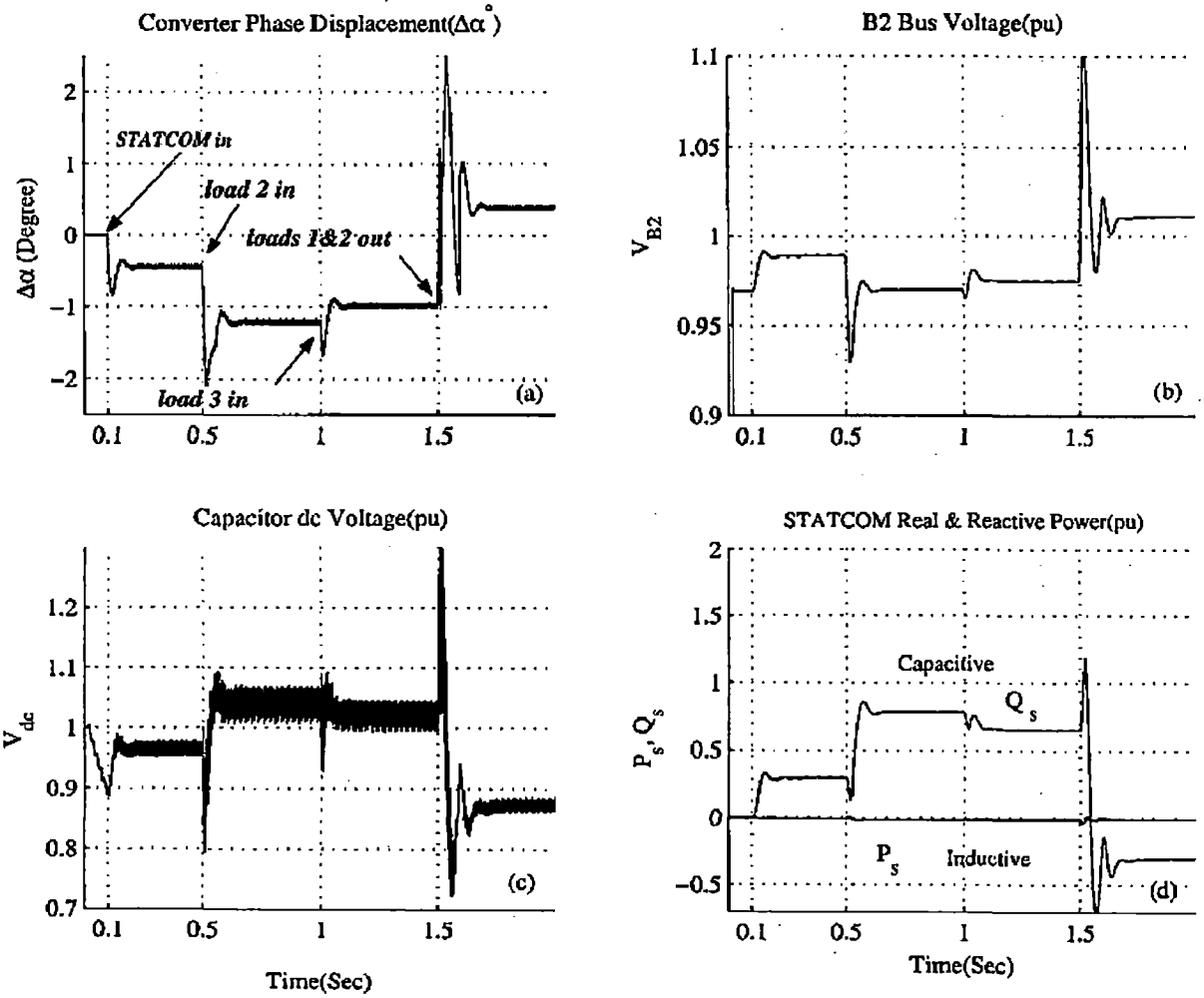


Figure 3.3: STATCOM Simulation Results (1)

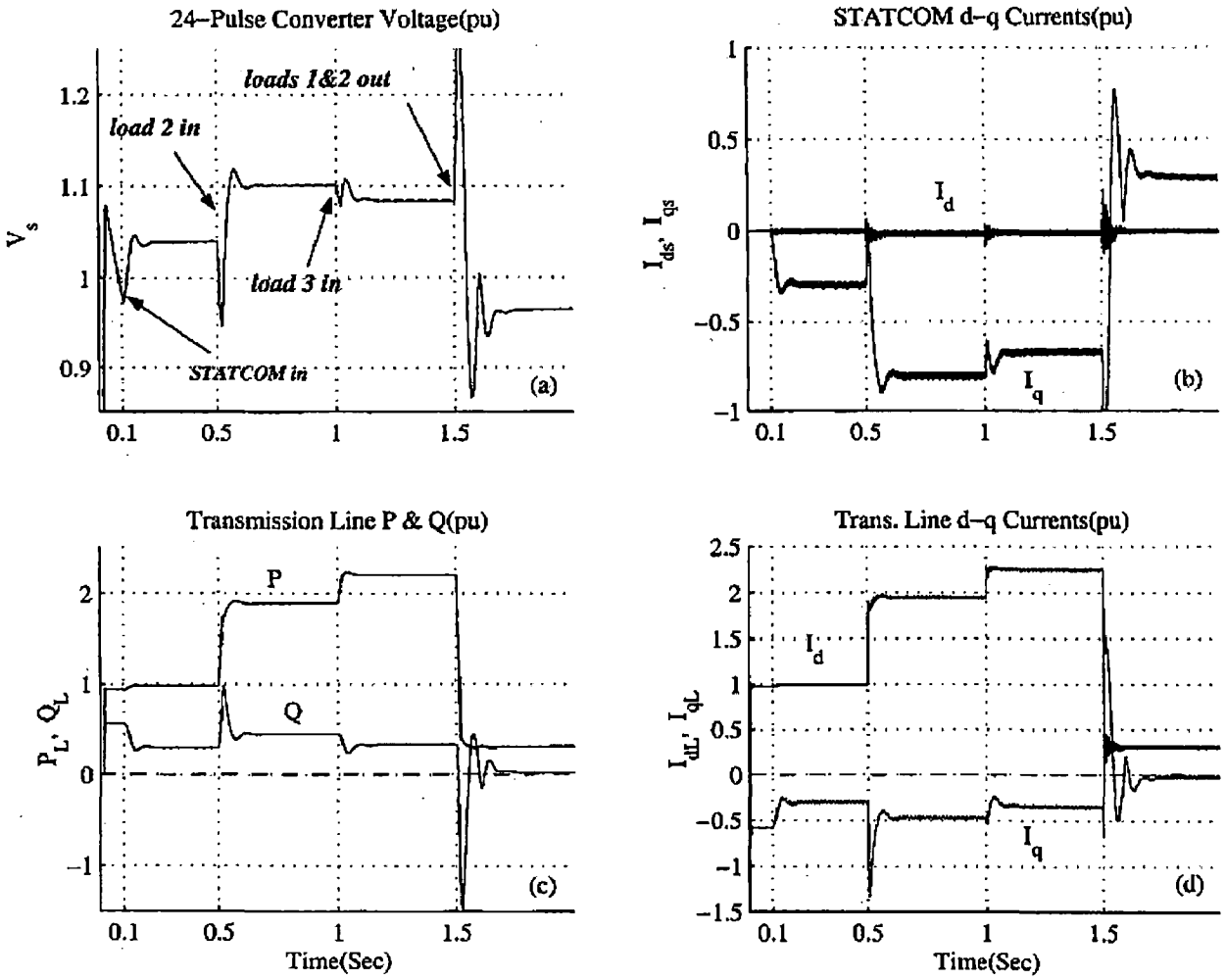


Figure 3.4: STATCOM Simulation Results (2)

Figure 3.5 shows the synchronizing signal, θ, which is generated by the PLL system. The STATCOM voltage and injecting current at the high voltage side of the coupling transformer in two operating modes of the STATCOM are shown in Figure 3.6. The STATCOM current (injecting current) lags the voltage by almost 90^0 in capacitive operation mode and leads the voltage by almost 90^0 in inductive operation mode. Besides, it can be seen that, due to filtering effect of the coupling transformer, the injected STATCOM AC current has very little distortions. Total Harmonic Distortion (THD) of the STATCOM current at the high voltage side of the coupling transformer was measured by PSB to be THD = 0.041, as shown in Figure 3.7. Therefore:

$$I_{rms} = \sqrt{I_1^2 + I_h^2} = \sqrt{I_1^2 + (0.041 I_1)^2} = 1.00084 I_1 \qquad (3.8)$$

Where I_{rms} is the total rms of the current, I_1 is the rms of the fundamental harmonic and I_h is the rms of the total harmonic contents. Therefore the STACOM current meets the power quality requirements with a 24-pulse converter.

The simulation shows that the STATCOM with the 24-pulse converter and decoupled control strategy provides a fast and reliable method for power system compensation and voltage regulation. The response time to major system disturbances (ΔP = 2pu) is about 0.2 Sec, while the STATCOM operation mode switches from capacitive to inductive. This fast reliable control is provided by power electronic components such as high power GTOs. By using a high pulse converter, such as the 24-pulse converter in this simulation, the power quality and harmonic problems are ensured to satisfactory levels.

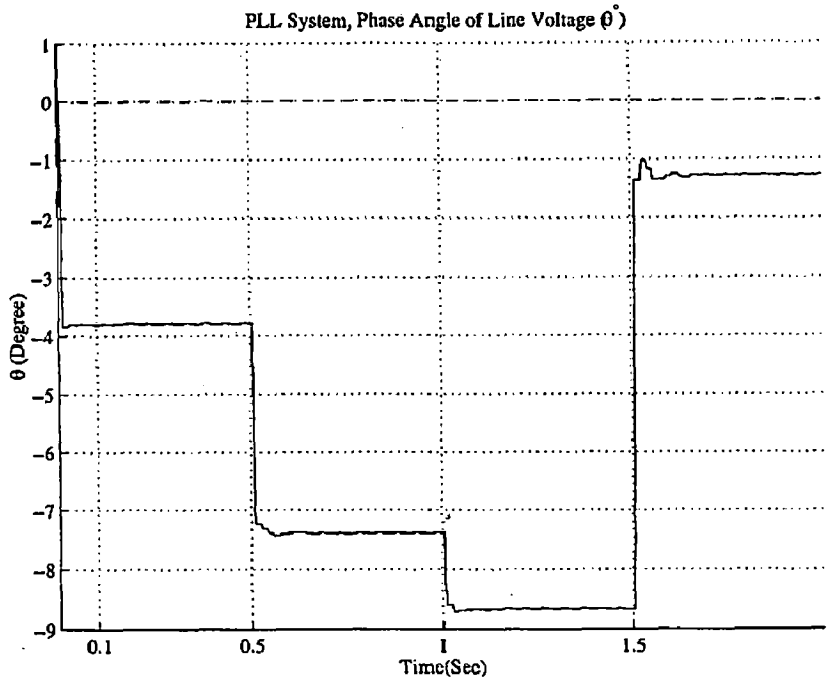


Figure 3.5: Synchronizing Signal, θ, Generated by PLL

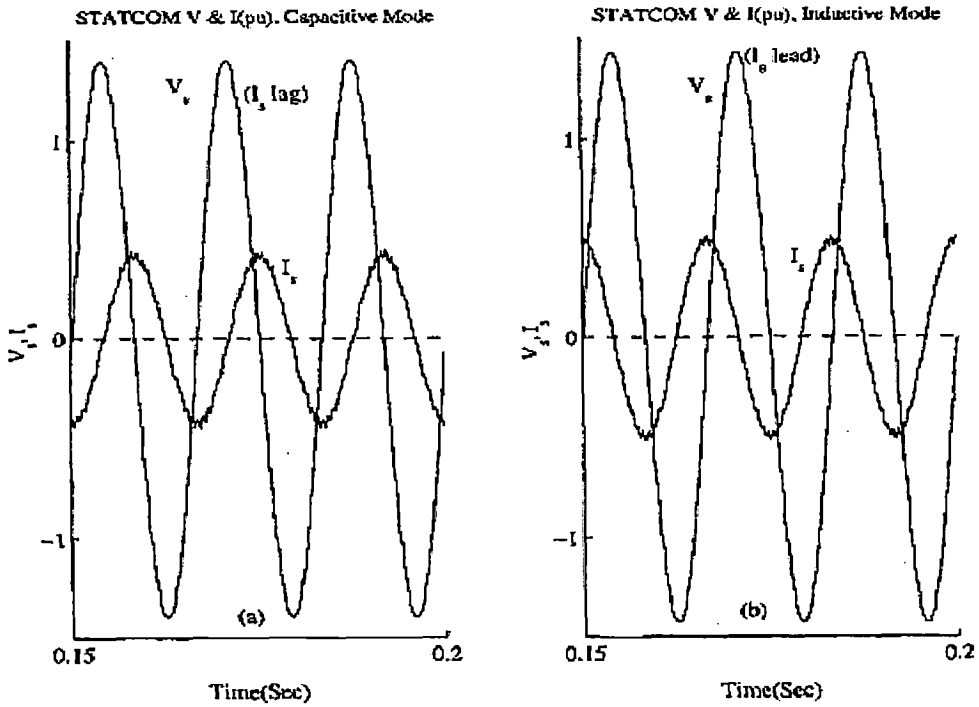


Figure 3.6: STATCOM Voltage and Current

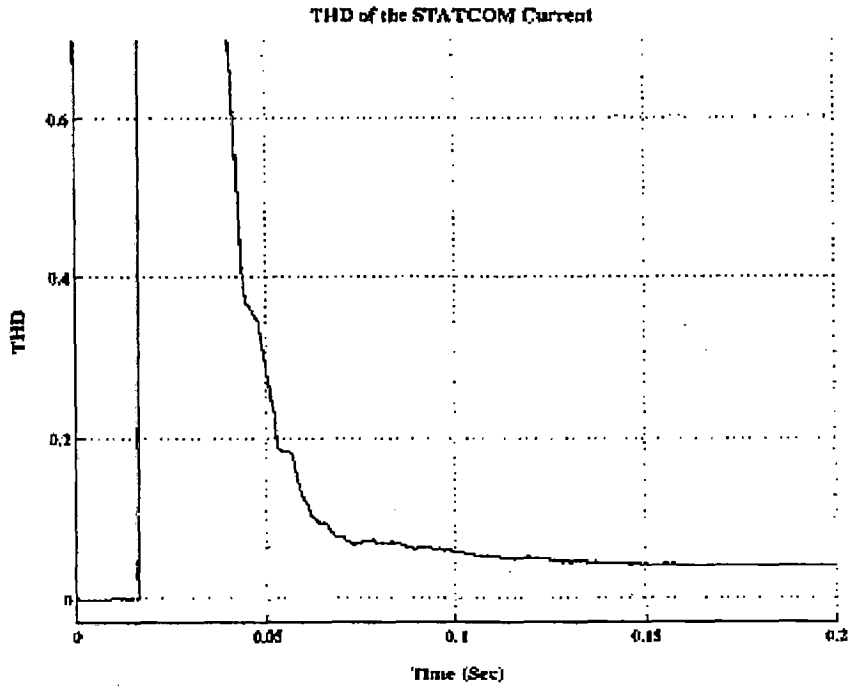


Figure 3.7: THD of the STATCOM Current (THD = 0.041)

3. A STATCOM STABILITY ENHANCEMENT

The operation of the STATCOM in various operating modes was simulated in Chapter 3. The objective was to verify the performance of the 24-pulse converter with the decoupled control strategy. In this finding, the control system of the STATCOM is investigated in great details and it is shown that the STATCOM may be become unstable or operate with sustained oscillations even if it performs well in some conditions. Two major factors that may cause instability and oscillations are introduced and a new supplementary control loop is designed to ensure stable response of the STATCOM. The new supplementary control design is validated by digital simulation and it is shown that it prevents instability of the STATCOM.

3. A.1 Dynamic Performance of the STATCOM

Figure A.1 shows the power system representation as seen from the STATCOM. X_{eq} is the Thevenin equivalent system reactance as seen by the STATCOM bus (including coupling transformer), V_{eq} is the equivalent system voltage and V_t is the STATCOM bus voltage.

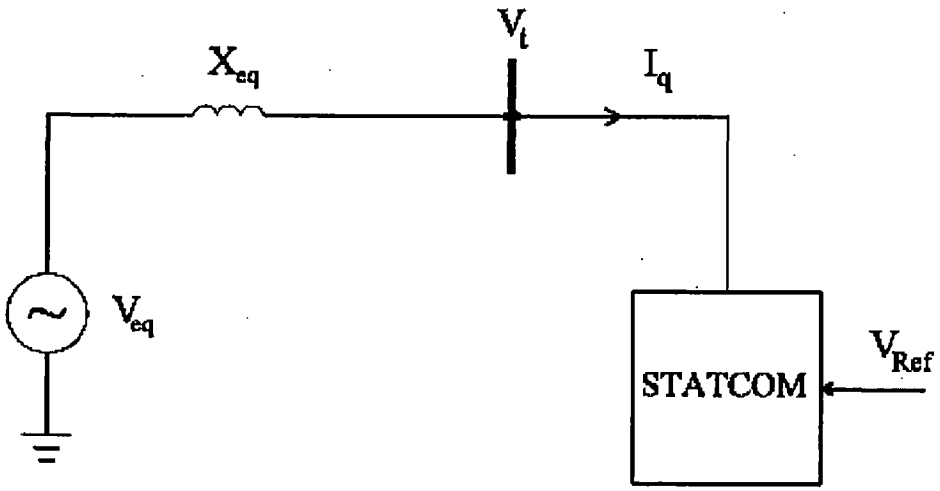


Figure A.1: Power System Representation with STATCOM

It is notable that X_{eq} and V_{eq} are not fixed and vary as the load varies or due to generator outages or line switchings. If the STATCOM operates in capacitive mode the bus voltage, V_t, is obtained as:

$$V_{eq}\angle 0 = V_t\angle 0 + (jI_q)(jX_{eq}) \tag{A.1}$$

$$V_t = V_{eq} + I_q X_{eq} \tag{A.2}$$

A block diagram can be developed to represent the system in Figure A.1. The STATCOM is essentially a reactive current source that responds to I_{qRef} with a delay time to Td which is usually less than 1ms for a converter. Therefore for dynamic studies, the STATCOM is considered as a transportation lag and can be modeled as [1],[19], [20],[24]:

$$G(s) = e^{-T_d s} \tag{A.3}$$

Where G(s) is the STATCOM model and Td is the transportation lag. Since Td is very small, it can be replaced with a first order approximation as:

$$G(s) \simeq \frac{1}{1+T_d s} \tag{A.4}$$

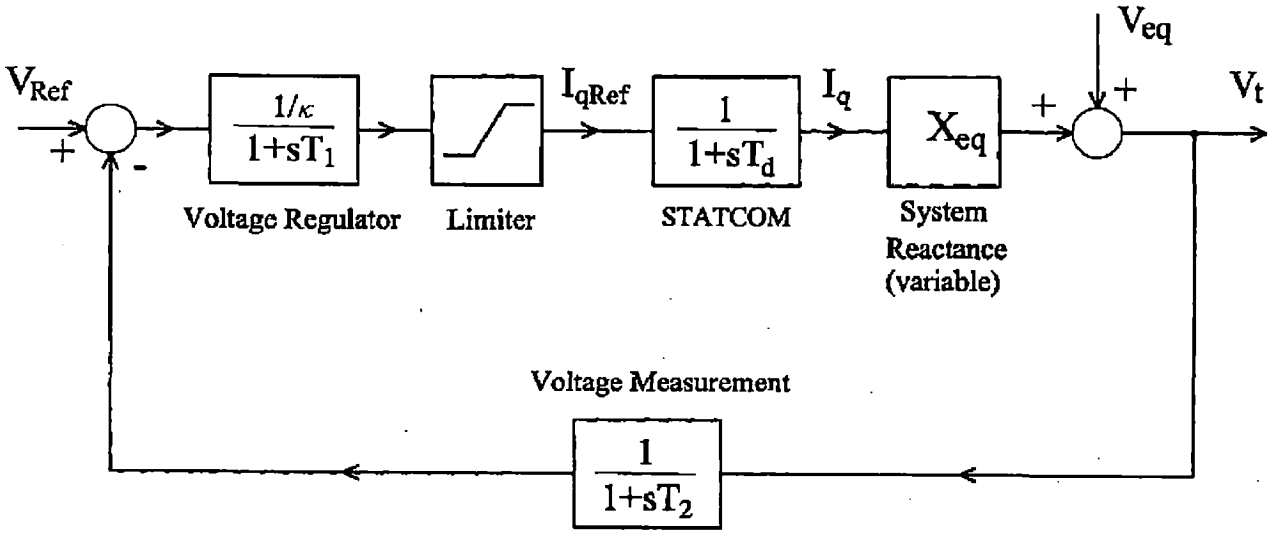


Figure A.2: Basic Block Diagram Representation of the STATCOM

Figure A.2 shows the block diagram representation of the STATCOM [1],[20]. Voltage regulator gives the required reactive current, I_{qRef}, with a transportation lag, T_1, which is about 10-50 ms for a PI controller [1], whiles the regulation slope, k, is about 1-5%. The transportation lag for the voltage measurement is about one voltage cycle or 16 ms for f = 60Hz.

3. A.2 EFFECT OF THE POWER SYSTEM STRENGTH

As seen is Figure A.2 the power system reactance, X_{eq}, is a part of feedback loop and therefore the STATCOM response time and stability is a function of power system strength or equivalent reactance [1],[2],[20],[26]. A power system is considered strong when its short circuit capacity is high or its impedance is low. Similarly a power system seen from the STATCOM bus is considered weak when its short circuit capacity is low or its impedance is high. The system strength determines the degree of voltage variation due to STATCOM reactive current injection and therefore affects the gain around the feedback loop in Figure A.2. If the system impedance is increased (weak system) the amount of voltage change due to STATCOM reactive current is increased. In other words, the loop gain increases and the STATCOM tends to become unstable. On the other hand, if the system impedance is decreased (strong system) the amount of voltage change due to reactive current injection is decreased and the system becomes more stable, although the response is slower than the weak system. Therefore system strength affects greatly the response time and the stability margin of the STATCOM. As stated earlier the power system reactance, X_{eq}, varies as the loads are added or rejected, or when a generator or line outage occurs. Therefore the voltage regulator that operates well in one system condition, may become unstable or result in oscillations when a major load is removed or a transmission line outage occurs. On the other hand, if the voltage regulator gain is reduced to give a fast and stable response for a weak system, it would result in a very sluggish response with a strong system.

3. A.2.1 Digital Simulation

To demonstrate the effect of the power system strength on the voltage regulator and the STATCOM stability, we consider again the power system of Chapter 3, as shown in Figure A.3.

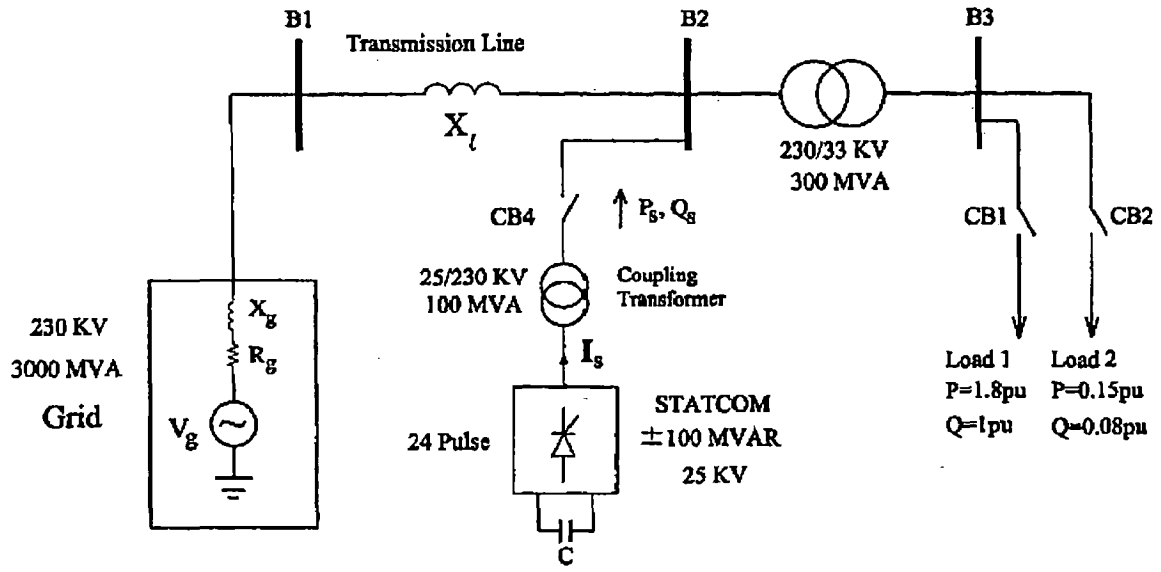


Figure A.3: Single Line Diagram of Power Transmission System with the STATCOM

The power system parameters are the same as that of Chapter 3, except for the loads and the grid short circuit capacity which is 3000 MVA. Load 1 is an inductive load with P = 1.8 pu and Q = 1 pu (at rated voltage) and load 2 is an inductive load with P = 0.15 pu and Q = 0.08 pu (at rated voltage). The voltage regulator parameters are the same as Chapter 3 with Kp = 0.005 and Ki = 3. The simulation results are shown in Figure A.4 and are explained below:

(a) t = 0.1 Sec

At this time the STATCOM is switched to bus B2, while both loads are in the system. The STATCOM operates in capacitive mode and supplies reactive power to bus B2. Therefore bus voltage increases due to reactive power compensation. Figure A.4 (a) shows the output of the voltage regulator, I_{qRef}. The voltage regulator is stable with a fast response. The system is considered a strong system with low impedance.

(b) t = 0.4 Sec

At this time load 1 is rejected and only load 2 is in the system. Now the power system is a weak system with low short circuit capacity. As seen in Figure A.4 (a) the voltage regulator exhibits strong oscillations and therefore the bus voltage oscillates. This can be explained as the voltage regulator gain is the same as for the strong system, while the loop gain was increased significantly due to load rejection.

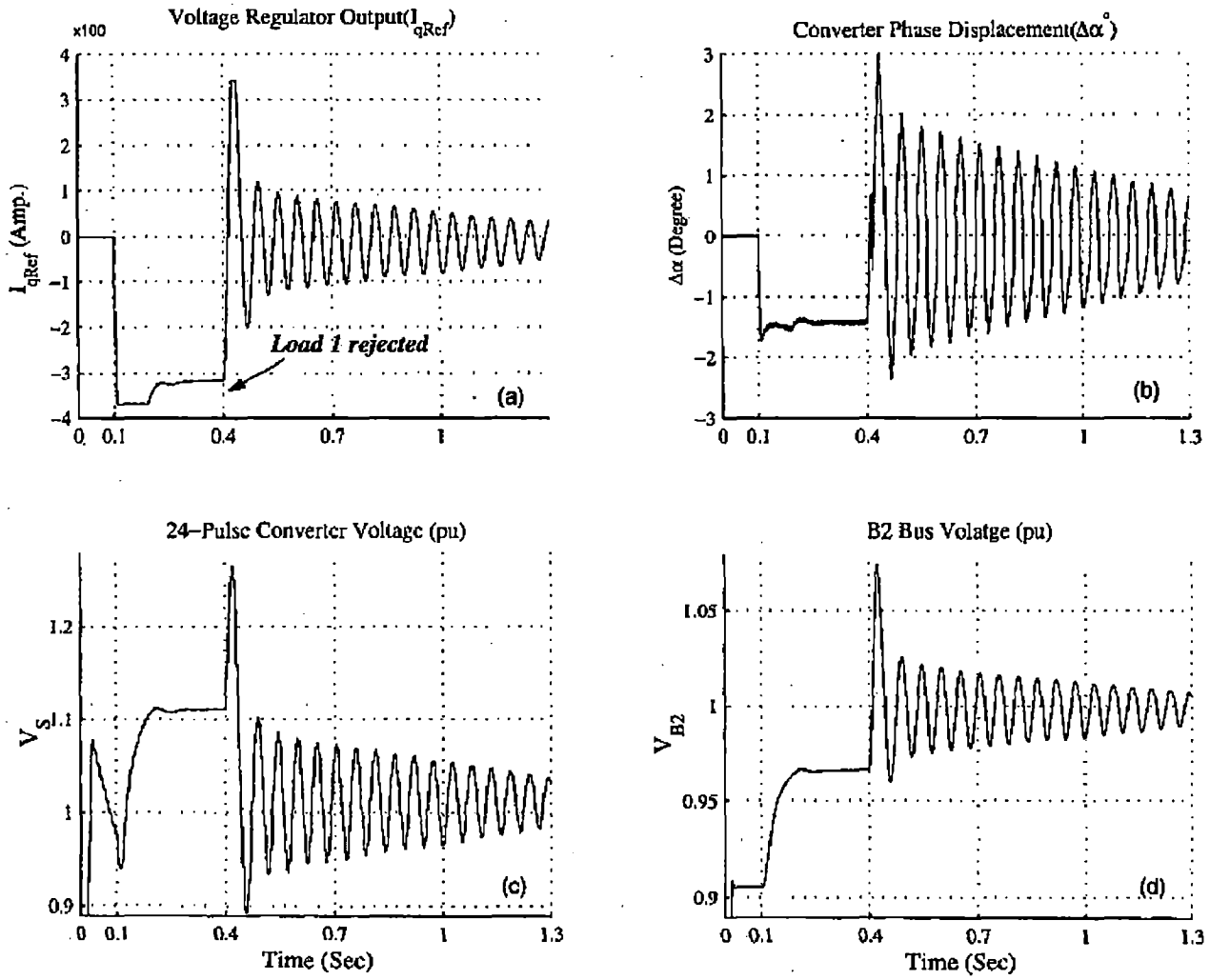


Figure A.4: Demonstration of the STATCOM Response for a Weak Power System

3. A.3 EFFECT OF THE PHASE-LOCKED LOOP

As explained in Chapter 3, the Phase-Locked Loop (PLL) provides the synchronizing signal of the STATCOM which is the phase angle of the STATCOM bus voltage,. It is obtained from comparing the zero-crossing of the STATCOM bus voltage with that of a reference voltage

with zero phase angle. In the case of a sudden change in power system, such as adding or removing of a load or system voltage variations, it takes at least half a period of voltage (8 ms for f=60 Hz) for the PLL to be synchronized with the new phase angle, in addition to signal processing delay time. During this time, the STATCOM operates at the previous phase angle while the bus voltage phase angle has already changed. Depending on the amount of phase angle change and whether it is increased or decreased, an uncontrolled reactive power exchange occurs between the STATCOM and the power system [35]. Besides, in the case of a weak power system, the phase angle of the busvoltage can change greatly in one period, while the PLL is not synchronized with the bus voltage yet. This delay time in PLL may lead to more oscillations in voltage regulator. This effect is significant when the STATCOM operates at high reactive currents.

Since all the previous simulations of the STATCOM have been performed based on the Laplace domain model of the STATCOM, and not the actual GTO converter, the effect of the PLL delay time has not been demonstrated by digital simulation so far. Thanks to newly developed modeling of the STATCOM, it was possible to demonstrate the actual process of the STATCOM step changes and to explain the effect of the PLL delay on the STATCOM stability.

To demonstrate the effect of PLL delay time, the results of the digital simulation in Chapter3 are shown again in Figure A.5 and A>6.

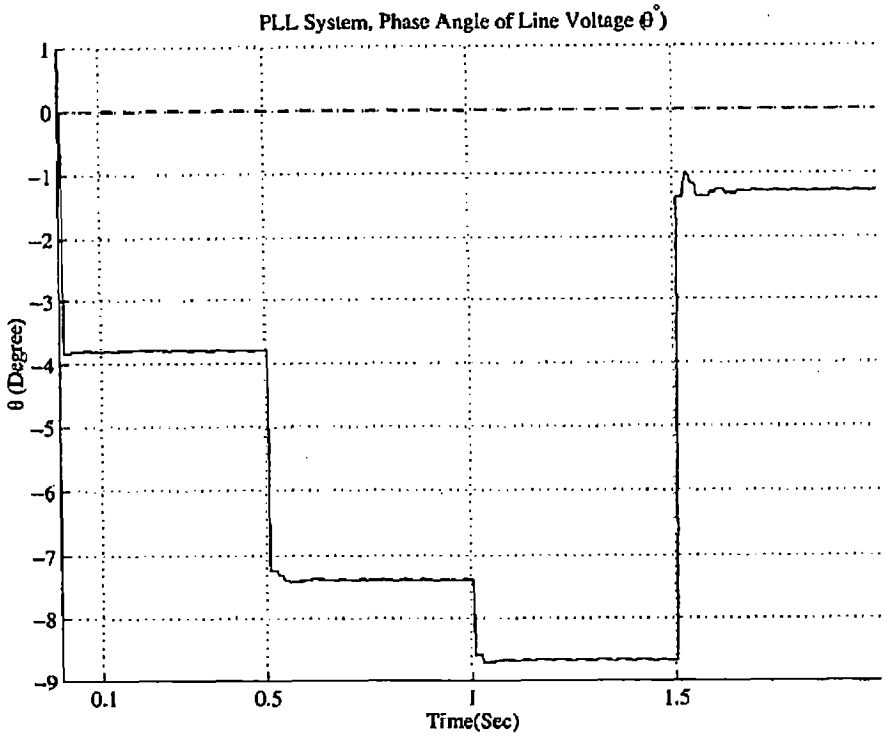


Figure A.5: PLL Synchronizing Signal

At t = 0.5 Sec, an inductive load is switched too the power system and the STATCOM is supposed to inject more reactive power. However due to the PLL delay time, the STATCOM voltage leads the bus voltage for more than half a cycle and therefore the STATCOM dc capacitor is discharged as the real power flows from the STATCOM to the power system. Thus the 24-pulse converter voltage and the injected reactive power drop at t = 0.5 Sec (Figures A.6 (b) and (c)). As the result, the bus voltage drops significantly (Figure A.6 (d)) and thus the voltage regulator output, I_{qRef}, jumps to a very high capacitive value (Figure A.6 (a)). The STATCOM compensates for the required reactive power after the PLL delay and operates as expected, however PLL delay caused an additional oscillation which can be significant for a weak power system. As another observation, we look at t = 1.5 Sec. At this time two inductive loads are rejected and only a capacitive load remains. The STATCOM is supposed to operate in inductive mode, however due to PLL delay the STATCOM voltage lags the bus voltage for a while and the real power flows from the power system and the STATCOM dc capacitor is charged significantly. Thus the STATCOM injects more capacitive reactive power (Figure

A.6(c)) and the voltage increases greatly (Figure A.6 (d)). This causes an additional strong oscillation that may lead to more oscillations or instability in a weak power system.

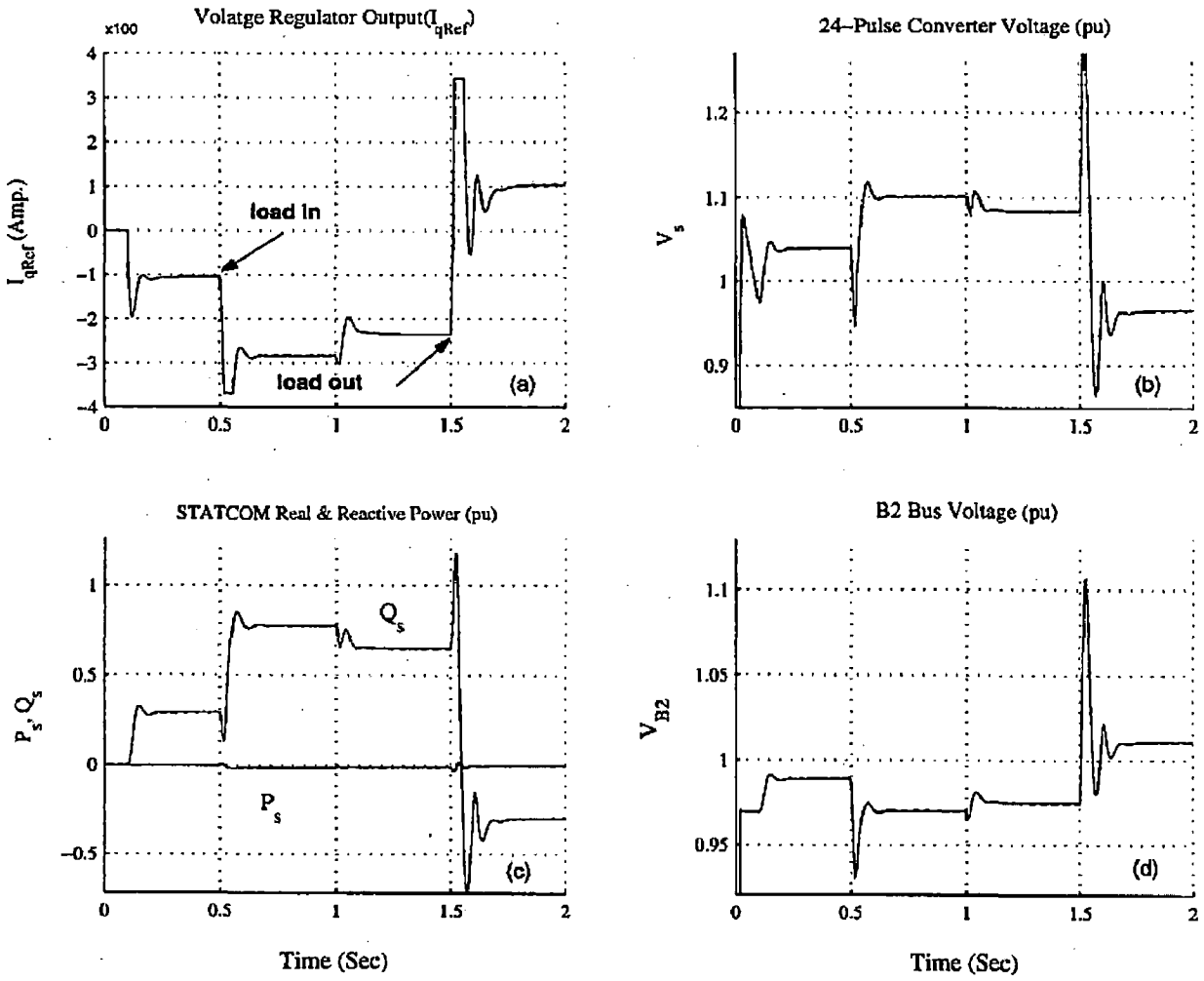


Figure A.6: Demonstration of the Effect of PLL Delay on the STATCOM Response

3. A.4 AUTOMATIC GAIN CONTROLLER

It was shown that the power system strength has a significant effect on the overall STATCOM stability and while the STATCOM can operate well for a strong power system, it may become unstable with a weak power system. Besides, the PLL delay time may lead to oscillations. Since the system strength changes the loop gain significantly, it would be desirable to dynamically adjust the voltage regulator gain in order to prevent instability or oscillatory behavior of the STATCOM. The key is to detect the voltage regulator oscillations and reduce its gain until the system is stable. An Automatic Gain Controller (AGC) was designed to reduce the voltage regulator gain during the oscillations and not to affect the STATCOM in normal operation. Thus the voltage regulator gain is set up to give a fast response for a strong power system (high gain) and in the case of a weak system the AGC gain is dynamically adjusted to prevent instability. The proposed AGC in this thesis is a variable gain in series with voltage regulator and is comprised of three elements: Oscillation Detector, PLL Oscillation Eliminator and Gain Reduce [35]. Figure A.7 shows the STATCOM block diagram with the AGC.

(a) Oscillation Detector

In order to detect any oscillations of the voltage regulator, its output, I_{qref}, is monitored continuously and the maximum and minimum of I_{qRef} ($max.I_{qRef}$, $min.I_{qRef}$) are computed in an interval of Δt. The difference between $max.I_{qRef}$ and $min.I_{qRef}$ determines the degree of oscillations or ΔI_{qRef}. Based on ΔI_{qRef} a variable gain, k, will be in effect in series with the voltage regulator to reduce its overall effective gain. One important aspect of the Oscillation Detector design is to select the time, Δt, because if its is too long or too short the oscillations may not be detected properly. Since the voltage regulator input is the bus voltage error, e_v, the measurement block delay should be considered in Δt, which is about one period of voltage. On the other hand, the delay time of the PLL system is at least half a period which should be

considered in order to avoid oscillations due to PLL delay. Other delays such as the STATCOM response delay and signal processing time of the AGC should also be considered. It follows that Δt can not be smaller than two voltage periods or 33 ms for f = 60 Hz. So the time interval, Δt was selected to be 40 ms.

(b) PLL Oscillation Eliminator

In the case of a sudden change in the power system, there will be one or more oscillations due to the PLL inherent delay time. In order to prevent the AGC from acting on these oscillations, PLL Oscillation Eliminator always ignores the first ΔI_{qRef} that is more than 1 A. In this way, we ensure that the AGC does respond to the PLL oscillation. This is essential as the PLL oscillations may be vary large and very short duration and any AGC action on them may result in false gain reduction.

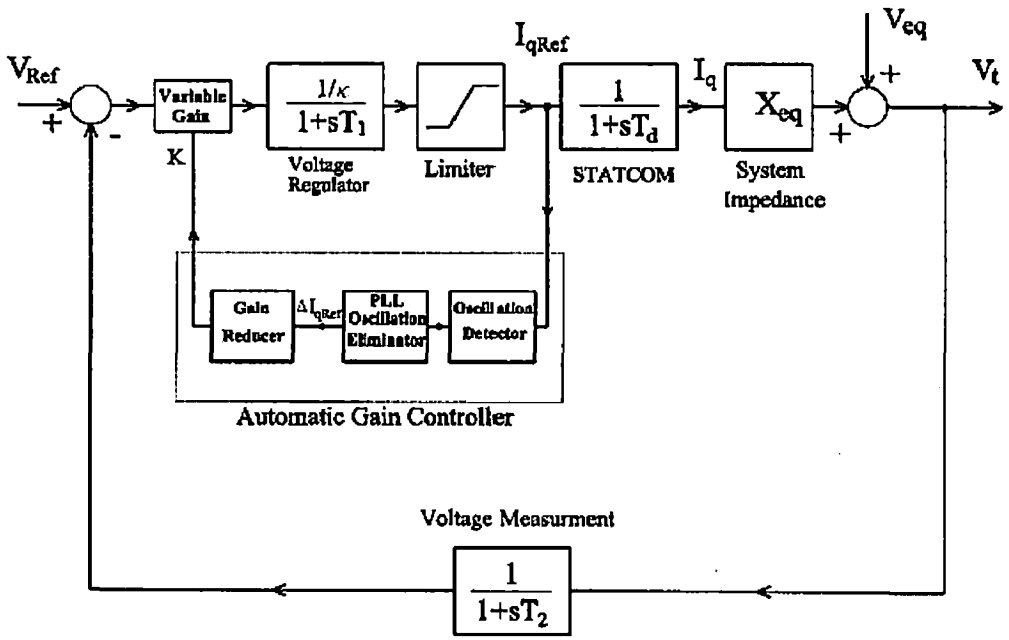


Figure A.7: Block Diagram of the STATCOM with the AGC

(c) Gain Reducer

After computing ΔI_{qRef} and eliminating the unwanted oscillations, a variable gain, $0 < k \leq 1$, is applied in series with the voltage regulator. This variable gain is a function of ΔI_{qRef} and

should be smaller for larger ΔI_{qRef} and vice versa. A nonlinear function to meet the above requirements was selected as:

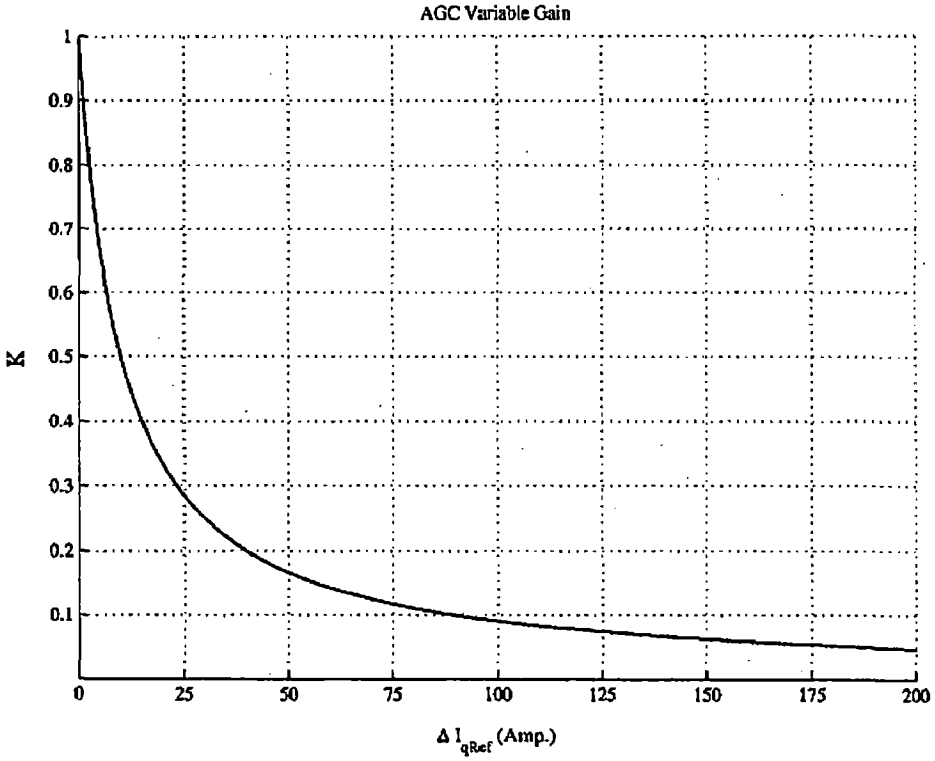


Figure A.8: Variable Gain of the AGC Versus ΔI_{qRef}

Figure A.8 shows the Gain Reducer output, *k*, versus ΔI_{qRef}. It can be easily verified that for $\Delta I_{qRef} = 0$, a unity gain is applied and it drops sharply for $\Delta I_{qRef} < 50A$ in order to stabilize the system fast.

3. A.4.1 Digital Simulation of the AGC

In order to verify the dynamic performance of the AGC in stabilizing the STATCOM, a digital simulation by Simulink/PSB software was conducted. In Section A2.1 it was shown that the STATCOM operates with strong oscillations when load 1 was rejected. Here the scenario is to verify the performance of the AGC in the same system of Figure A.3. The power system and STATCOM parameters are the same, except that the AGC was added to the STATCOM control system. The STATCOM switched to bus B2 at t = 0.1 Sec and at t = 0.4 Sec load 1 is rejected. The simulation results are shown in Figure A.9.

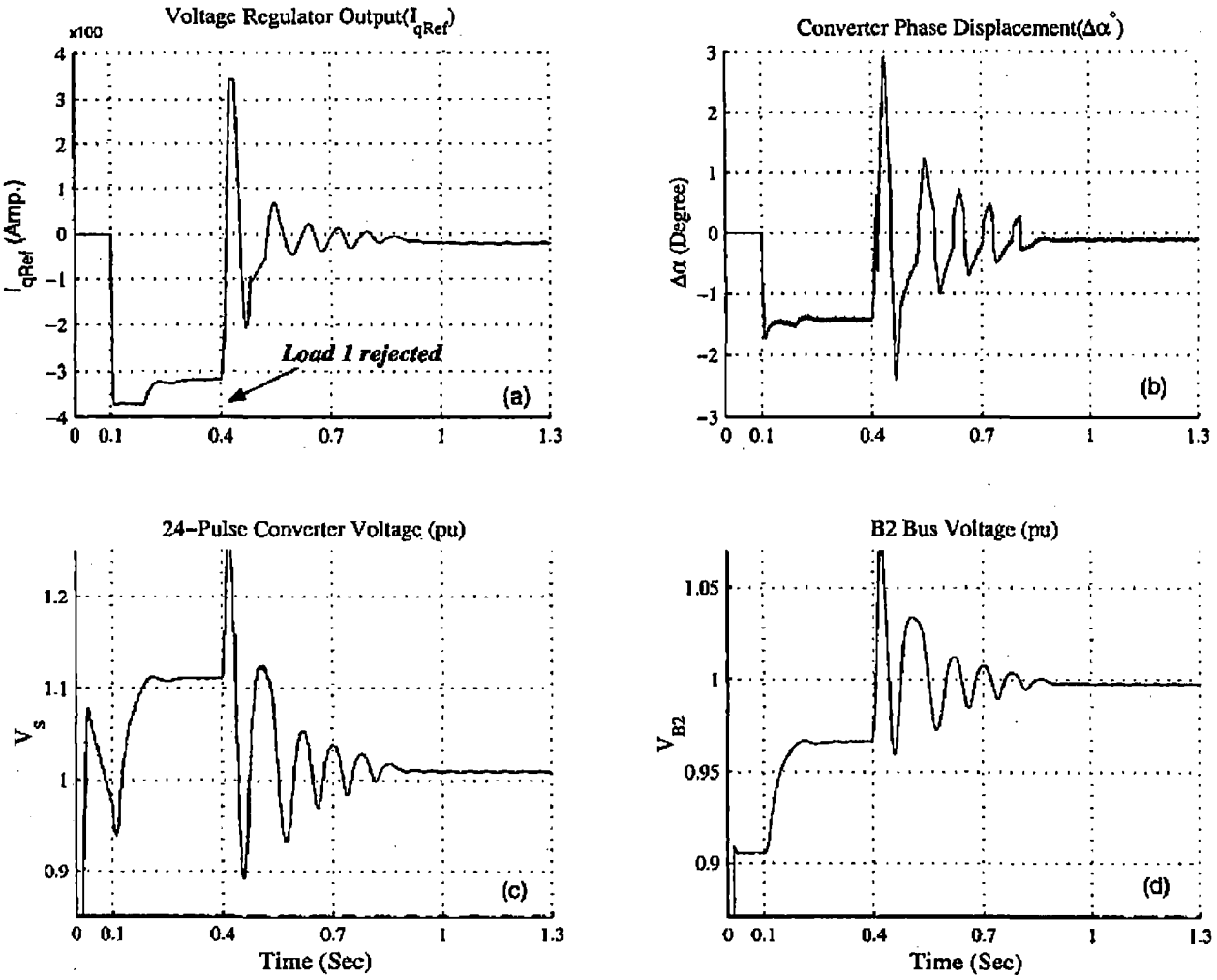


Figure A.9: Digital Simulation of the Effect of the AGC on STATCOM Stabilization

Figure A.9 (a) shows that the voltage regulator is stabilized after a few oscillations and as the result the converter voltage and thus the STATCOM bus voltage are stabilized (Figures A.9 (c) and (d)) while they continued to oscillate in Figure A.4. In order to further demonstrate the effect of the AGC, the simulation results of Section A.2.1 (without the AGC) are shown together with that of the STATCOM with AGC in Figure A.10. The thick line shows the simulation results with the AGC and the thin line is without the AGC. While the STATCOM without the AGC continues to oscillate until the need of the simulation (t = 1.3 Sec), the system with the AGC stops oscillating at t = 0.55 Sec. As expected the AGC does not affect the

STATCOM operation when there is no oscillation in voltage regulator and the results are the same before t = 0.4 Sec. The thick line is with the AGC and the thin line is without the AGC.

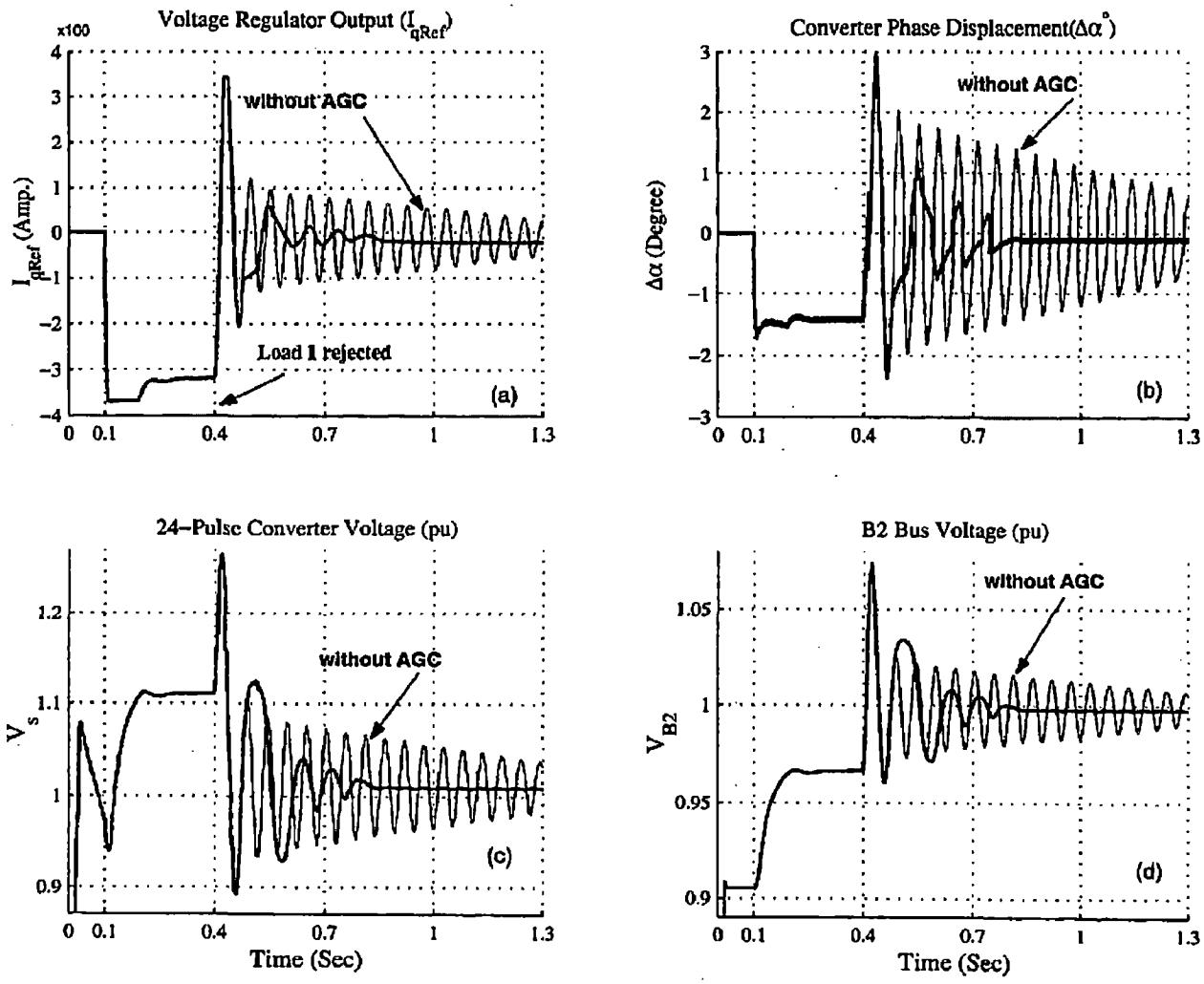


Figure A.10: Demonstration of the STATCOM Response With and Without the AGC

Figure A.11 shows ΔI_{qRef} computed by the AGC for Δt = 40ms and the variable gain, k. Figure A.11 (a) is the output of the Oscillation Detector and Figure (b) shows the output of the PLL Oscillations Eliminator. It is notable that some oscillations were ignored as they are caused by PLL delay time. Figure (c) shows the AGC variable gain, $0 < k \leq 1$. It can be seen that k is very small after t = 0.4 Sec and gradually gets closer to unity as the oscillations become smaller.

3. A.5 CONCLUSION

While the AGC does not affect the normal STATCOM operation, it is powerful and effective tool to stabilize the STATCOM and prevent strong oscillation due to weak power system. Thus the voltage regulator gain is set up to give fast response for the strong power system and the AGC performs the stabilization of the STATCOM in case of a weak power system. As the power system parameters, V_{eq} and X_{eq} may change suddenly due to faults, load switchings or system outages, the AGC ensures stable and reliable compensation of the power system by the STATCOM. However the AGC does not guarantee the optimum voltage regulator gain for the fastest response of the STATCOM. The optimum gain depends on the equivalent power system reactance which may vary from one load to the other one and other power system condition such as transmission line or generator outages.

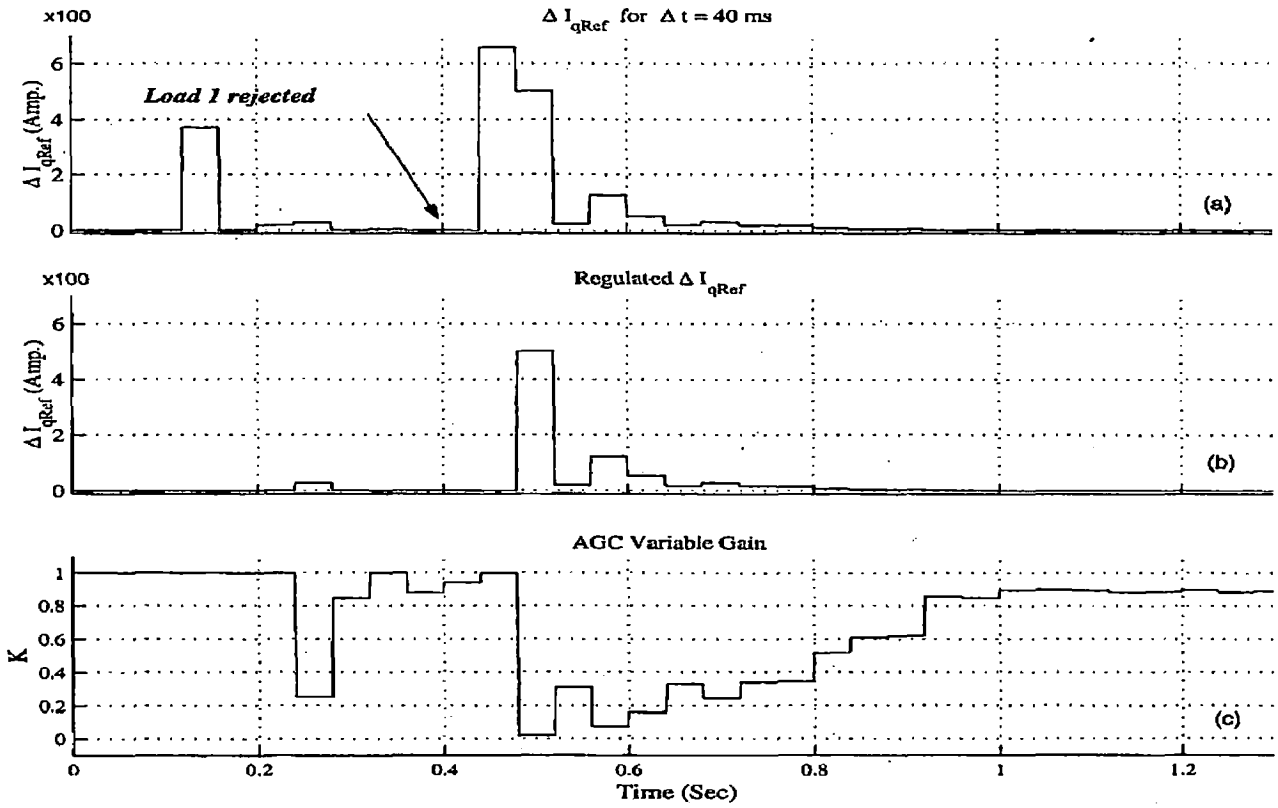


Figure A.11: AGC Simulation Results

4.0 SSSC: A COMPLETE DIGITAL SIMULATION STUDY

A complete digital simulation of the Static Synchronous Series Compensator (SSSC) within a power system, based on the operation and control fundamentals developed in Chapter 2, is presented in this chapter. The digital simulation is performed in MATLAB/Simulink environment using the Power System Block Set (PSB). The 24-pulse GTO-based converter developed in Chapter 2 is the basic building block of the SSSC and the operation of the SSSC is validated in both capacitive and inductive modes.

4.1 SYSTEM DESCRIPTION

4.1.1 Power System

Figure 4.1 shows the single line diagram of a radial transmission system with the SSSC compensation. The grid is represented by a 230kV source with 10000MVA short circuit capacity, Rg = 0.1pu and Xg = 0.3pu.

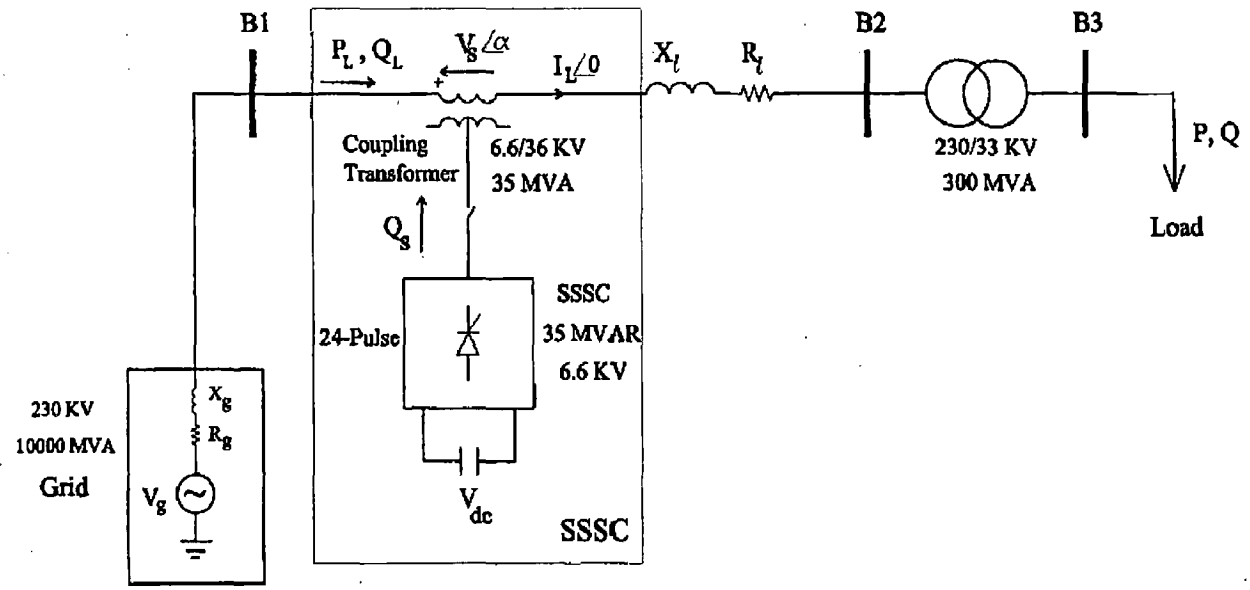


Figure 4.1: Single Line Diagram of the Power Transmission System with the SSSC

The system parameters are given as below:

(a) Transmission Line:

- Reactance, X_l: 0.25 pu (230 KV, 300 MVA)
- Resistance, R_l: 0.05 pu

(b) Power Tranformers: (Y/Δ)

- Rated Voltage: 230/33 KV
- Rated Power: 300 MVA
- Leakage Reactance: 0.01 pu

(c) SSSC:

- Type of Valves: GTO
- Number of Pulses: 24
- Nominal AC Voltage: 6.6 KV
- Nominal DC Voltage: 1 KV
- Rated Power: ±35 MVAR
- GTOs Forward Resistance: $1m\ \Omega$

(d) Capacitor Bank (dc):

- Total Capacitance: 10 mF
- Rated DC Voltage: 1 KV

(e) Coupling Transformer :(Y/Y)

- Rated Voltage: 6.6/36 KV
- Rated Power: 35 MVA
- Resistance: 0.001 pu
- Leakage Reactance: 0.02 pu

4.1.2 Control System

The control system was developed in Chapter 2 and is shown again in Figure 4.2. The PI controller parameters are: $Kp = 20$ and $Ki = 4$. The PLL system is synchronized with the line current, I_L, and generates the basic synchronizing signal, θ.

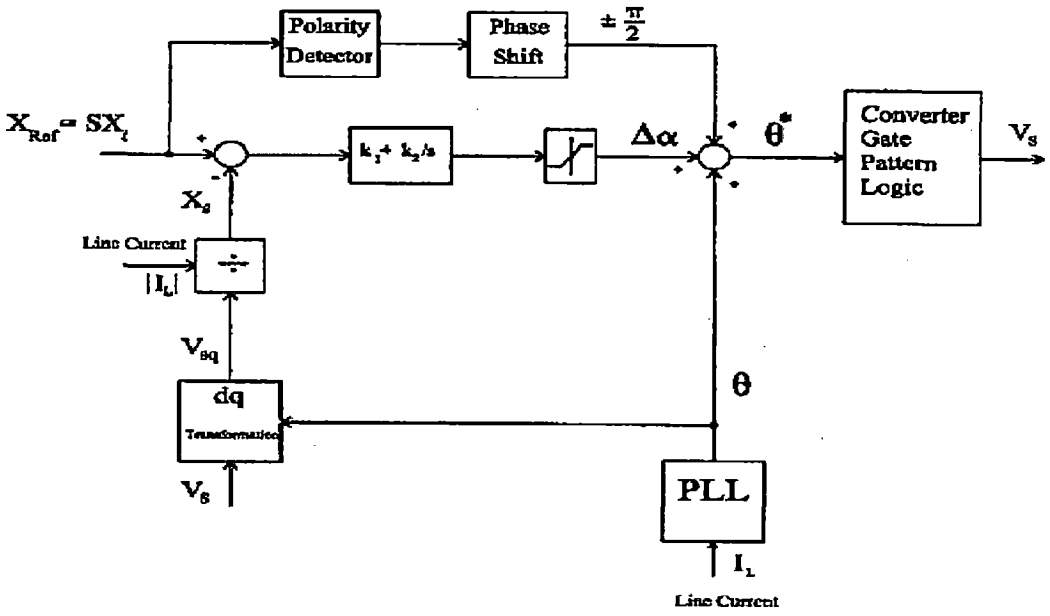


Figure 4.2: Basic Control Structure of the SSSC

4.2 DIGITAL SIMULATION

The operation of the SSSC in Figure4.1 was simulated with MATLAB/Simulink by using the Power System Blockset. The 24-pulse converter model developed in Chapter 2 was used as the basic building block of the SSSC. In order to make the system quantities easier to compare, all the measurements are in Per Unit system with $MVA_{base} = 100$ and the rated voltage of the each part of the power system. The simulation results are presented in two parts: capacitive and inductive operating mode of the SSSC.

4.2.1 Capacitive Operation

The grid voltage, Vg, is 1.01 pu and the load is an inductive load with P = 2 pu and Q = 1.2 (at rated voltage). The SSSC is switched to the transmission line at t = 0.15 Sec with a level of compensation S = 60%, i.e. the SSSC was set to compensate 60 percent of the series

transmission line reactance by injecting a capacitive reactance. Therefore $X_{Ref} = -0.6\ X_l$ or $X_{Ref} = -0.15$pu.

The simulation results are shown in Figures 4.3 and 4.4. The dc capacitor is discharged while at t = 0.15 Sec the SSSC is switched to the power system and the capacitor is charged by the power flow from the transmission line to the SSSC (Fig.4.3(c)). Since the SSSC is in capacitive mode, the injected voltage, Vs, lags the line current by 900, as shown in Figure 4.3 (a). Avery small deviation from -900 lets the real power flow from the line to SSSC in order to compensate for the coupling transformer and the switching losses. The effect of the capacitive series compensation on the power flow and the bus voltage can be seen in Figures 4.4(a) and (b), respectively. The B2 bus voltage increased from 0.87pu to 0.94 pu and therefore the transmitted real power increased from 1.49 pu to 1.72 pu. Figure 4.4(c) shows the SSSC injected voltage and the line current. It can be seen that the SSSC voltage, Vs, lags the line current, IL, by 900 and the Total Harmonic Distortion (THD) of the SSSC voltage is 0.092, as shown in Figure 4.4(d). As explained in Chapter 2, it can be concluded that:

Where V_{rms} is the total rms value of the voltage, V_h is the rms value of the total harmonic contents and V1 is the rms value of the fundamental harmonic. Therefore $V_1 = 0.995$Vrms and only 0.5% of the SSSC voltage is due to harmonics.

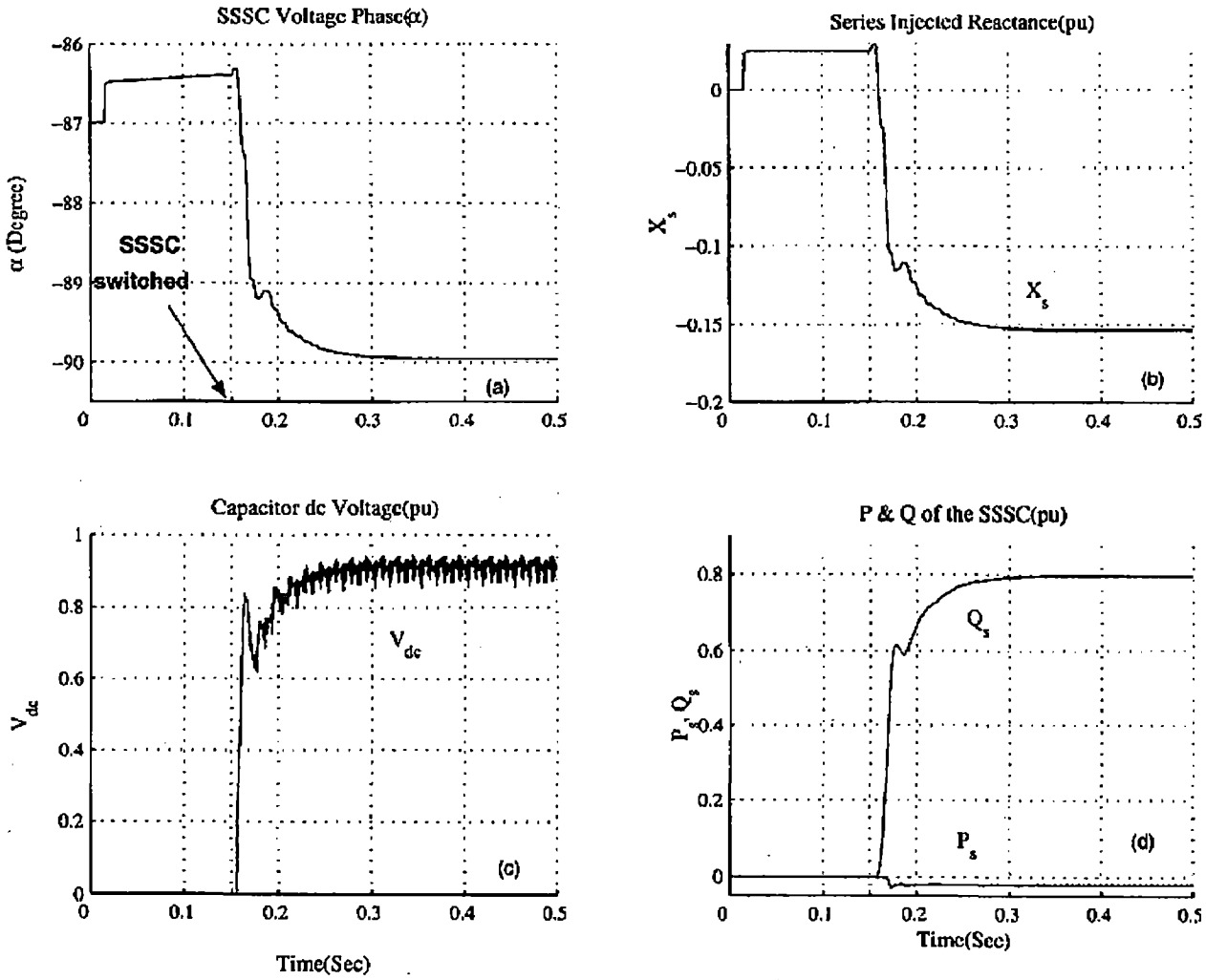


Figure 4.3: Digital Simulation Results of the SSSC in Capacitive Mode (1)

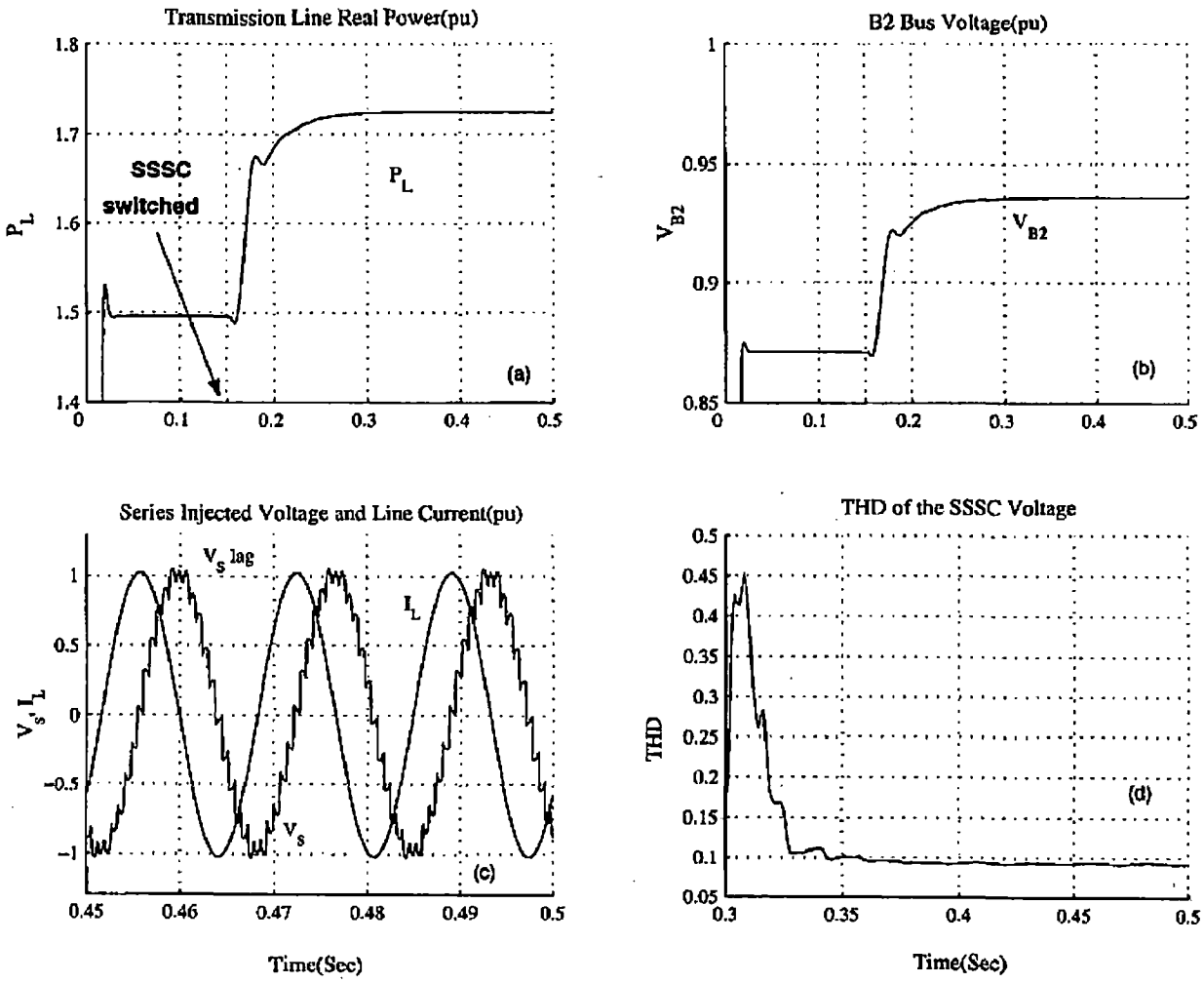


Figure 4.4: Digital Simulation Results of the SSSC in Capacitive Mode (2)

4.2.2 Inductive Operation

The grid voltage, Vg, is 1.04 pu. This can be considered as a slightly overvoltage due to low load level that may occur in some hours of the day. The load is an inductive load with P = 1.5 pu and Q = 0.05pu. In case of an overvoltage, an inductive series compensation is required to decrease the voltage at load bus. The SSSC was set to operate with S = 100%, i.e. the SSSC was set to inject an inductive reactance equal to the line reactance. Therefore X_{Ref} = 0.25pu.

The simulation results are shown in Figures 4.5 and 4.6. The SSSC is switched to the power system at t = 0.15 Sec and the dc capacitor is charged by the real power flow from the transmission line to the capacitor. The series injected voltage, Vs, leads the line current, IL, by 900 as the SSSC operates in inductive mode (Figure. 4.5 (a)). The effect of the inductive

compensation on the power flow and the bus voltage is shown in Figures 4.6(a) and (b). The B2 bus voltage drops from 1.017 pu to 1.001 pu and therefore the transmitted real power drops from 1.55pu to 1.51pu, which is the rated power of the load. Figure 4.6 (c) shows the series injected voltage, V_s, and the line current, I_L. It shows that V_s leads I_L by 90^0.

The digital simulation shows that the SSSC provides a fast and reliable series compensation that can operate in both capacitive and inductive modes. This fast and reliable device is based on multipulse, GTO converters, such as the 24-pulse converter in this simulation. As the THD measurement shows, the harmonic contents and therefore power quality are ensured to a satisfactory level.

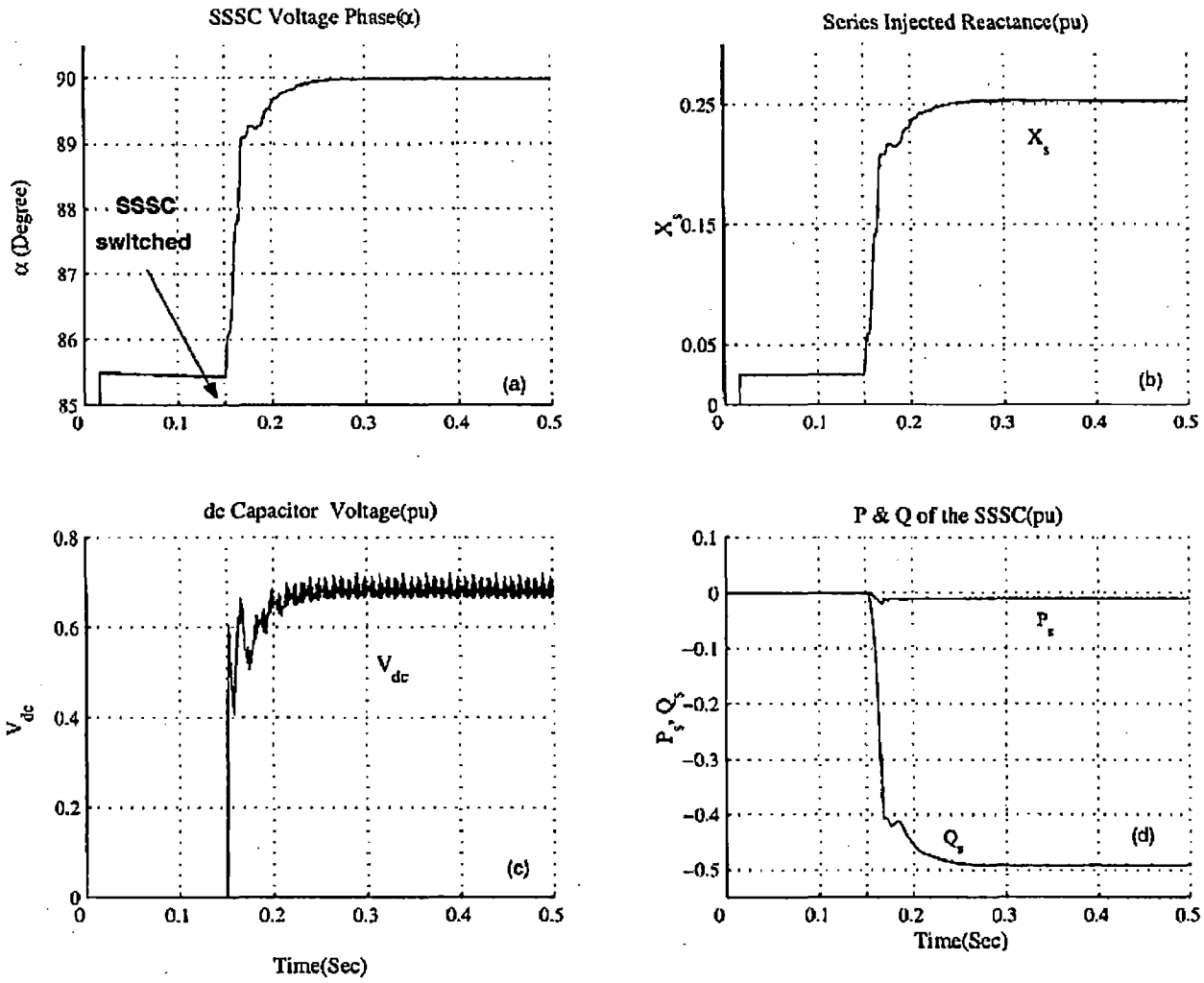


Figure 4.5: Digital Simulation Results of the SSSC in Inductive Mode (1)

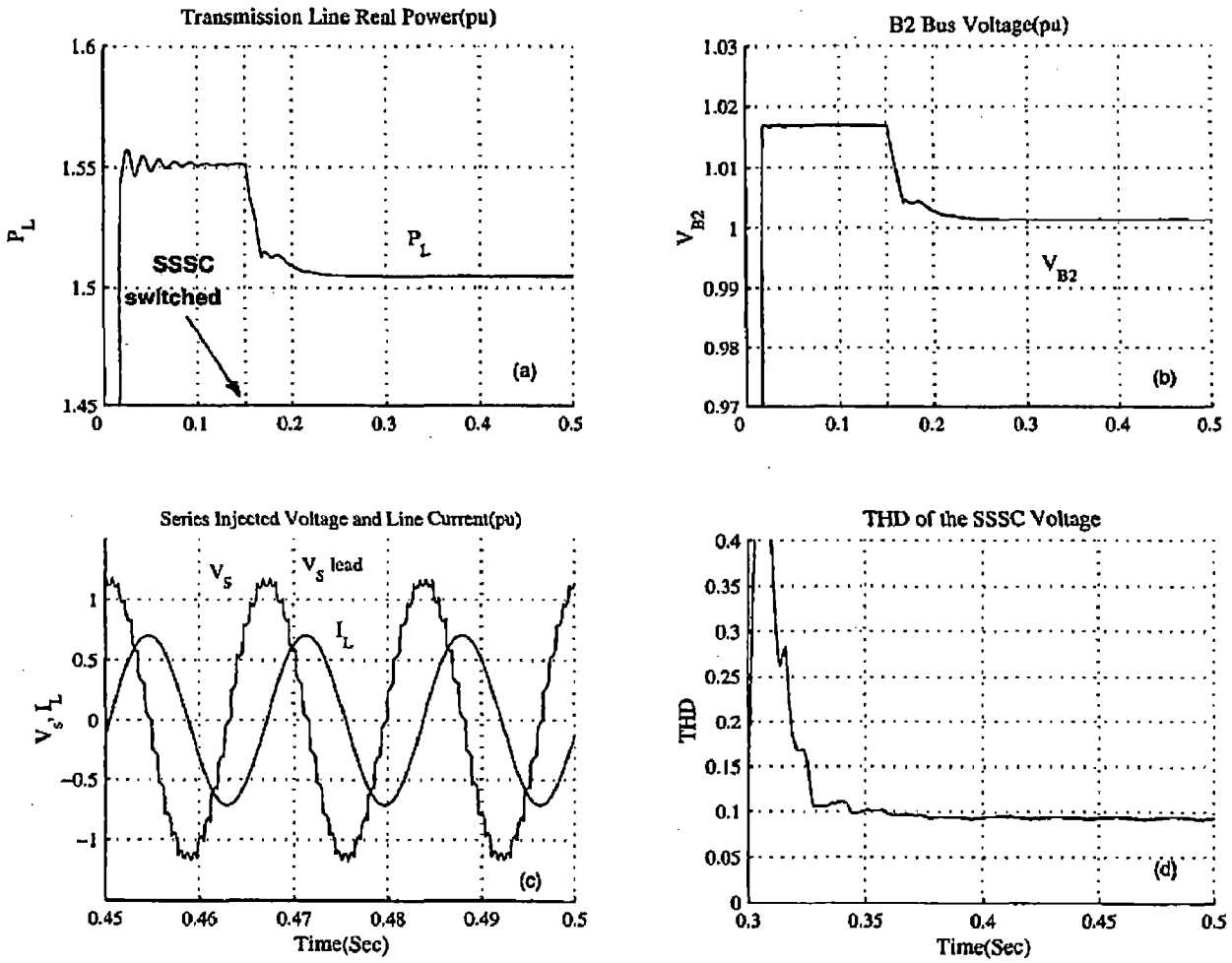


Figure 4.6: Digital Simulation Results of the SSSC in Inductive Mode (2)

4. B DYNAMIC PERFORMANCE OF THE SSSC

The digital simulation of the SSSC, using a 24-pulse converter was performed in Chapter 4. In this Appendix, the operation of the SSSC control system when major loads are added to or rejected from the power system is investigated in great detail. Supported by digital simulation, it is shown that the Phase-Locked Loop (PLL) delay can degrade the dynamic response of the SSSC. On order to enhance the transient performance of the SSSC, anovel auxiliary regulator was designed, using the dc capacitor voltage. The effect of the new auxiliary regulator is validated by digital simulation, using MATLAB/Simulink and Power System Blockset.

4. B.1 DYNAMIC OPERATION OF THE SSSC

When a major load is added to or rejected from the power system, the transmission line current varies and as the result, the SSSC output voltage and therefore its reactive power has to change so that it can maintain the required X_{Ref}. If the line current increases, the SSSC series injected voltage, Vs, has to increase and if the line current decreases, Vs has to decrease. The SSSC can maintain X_{Ref} as load varies, as long as the required reactive power,Q_s, does not exceed its power rating.

4. B.1.1 Digital Simulation

Figure B.1 shows the single line diagram of a power transmission system with the SSSC compensation. The power system and the SSSC parameters are the same as that of Chapter 4, but with two different loads. Load 1 is an inductive load with P = 1.5 pu and Q = 0.8 pu (at rate voltage) and load 2 is another inductive load with P = 1.2 pu and Q = 0.75 pu. The SSSC operates in capacitive mode with X_{Ref} = -0.1pu. The simulation results are shown in Figure B.2. Since the transient operation of the SSSC is under investigation, only dc capacitor voltage, V_{dc}, SSSC reactive power, Q_s and the injected series reactance, X_s, are shown.

The SSSC is switched at t = 0.1 Sec, while only load 1 is in the power system. At t = 0.3 Sec, load 2 is switched to the bus B3 and is rejected later at t = 0.6 Sec.

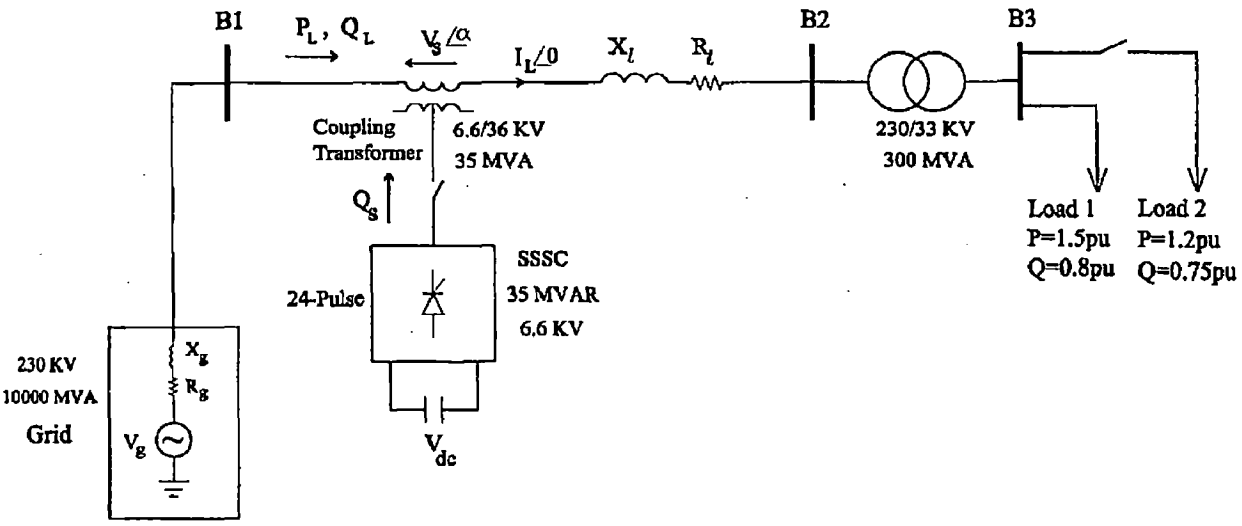


Figure B.1: Single Line Diagram of the Power Transmission System with SSSC

Figure B.2 shows that at load switching instants (t = 0.3 Sec and t = 0.6 Sec) the dc capacitor voltage exhibits very fast with large overshoot. Similarly, at t = 0.6 Sec, V_{dc} has to decrease, but it first increases and then drops very fast with large undershoot.

Figure B.4. Shows the PLL synchronizing phase angle, which is the phase angle of the line current. In order to investigate the effect of the PLL on the transient response of the SSSC, the PLL phase angle and the dc capacitor voltage at switching instants are shown in Figure B.3. As shown in Figure B.3 (a), at t = 0.30 Sec load 2 is added, but the PLL phase angle does not change until t = 0.31 Sec. This delay is because the PLL needs at least half a period of the line current plus the signal processing time for the new phase angle. The PLL operation is based on the zero crossing of the transmission line current. When the phase angle of the line current changes, it takes at least half a cycle to detect the new phase angle and therefore an inherent delay of at least 8ms is a part of the PLL operation. Similarly, as shown in Figure B.3 (b), load 2 is rejected at t = 0.60 Sec, but the PLL phase angle does not change until t = 0.61 Sec. During the time that the PLL is not exactly synchronized with the line current, real power exchange

occurs between the dc capacitor and the transmission line and leads to uncontrolled charging or discharging of the dc capacitor and the therefore oscillatory behavior of the SSSC at switching instants [36].

The effect of the PLL delay on the transient response of the SSSC was investigated by exact simulation. The large and fast variations of the dc capacitor result in large and fast variations in the series injected reactance, Xs, as shown in Figure B.2(c) and therefore it has direct effect on power system parameters such as line current is distorted or contains high frequency ripple. The noise content affects the PLL performance. In this case, other approaches such as appropriate filtering should be employed for better PLL performance.

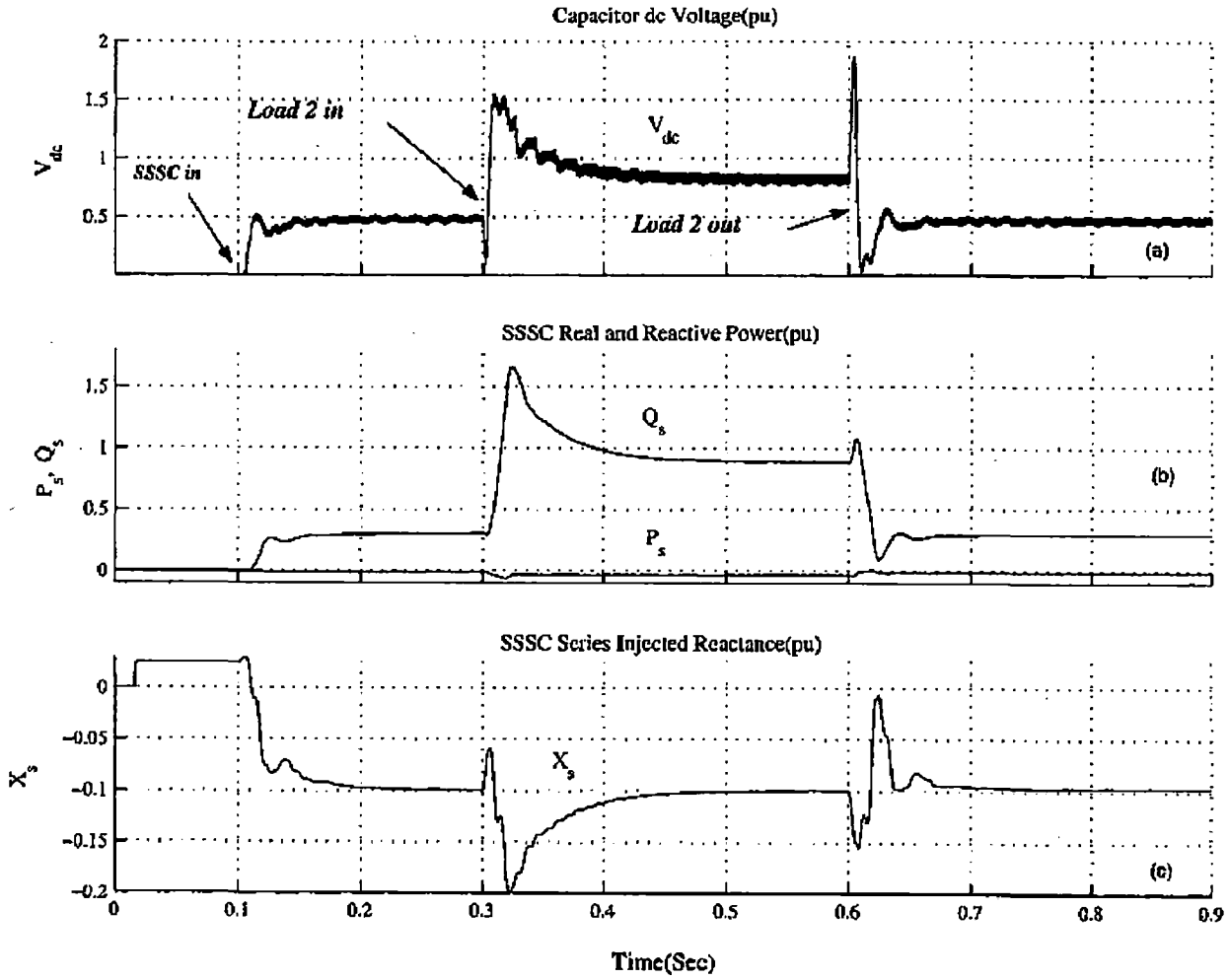


Figure B.2: Simulation Results of the SSSC Response to Load Switchings

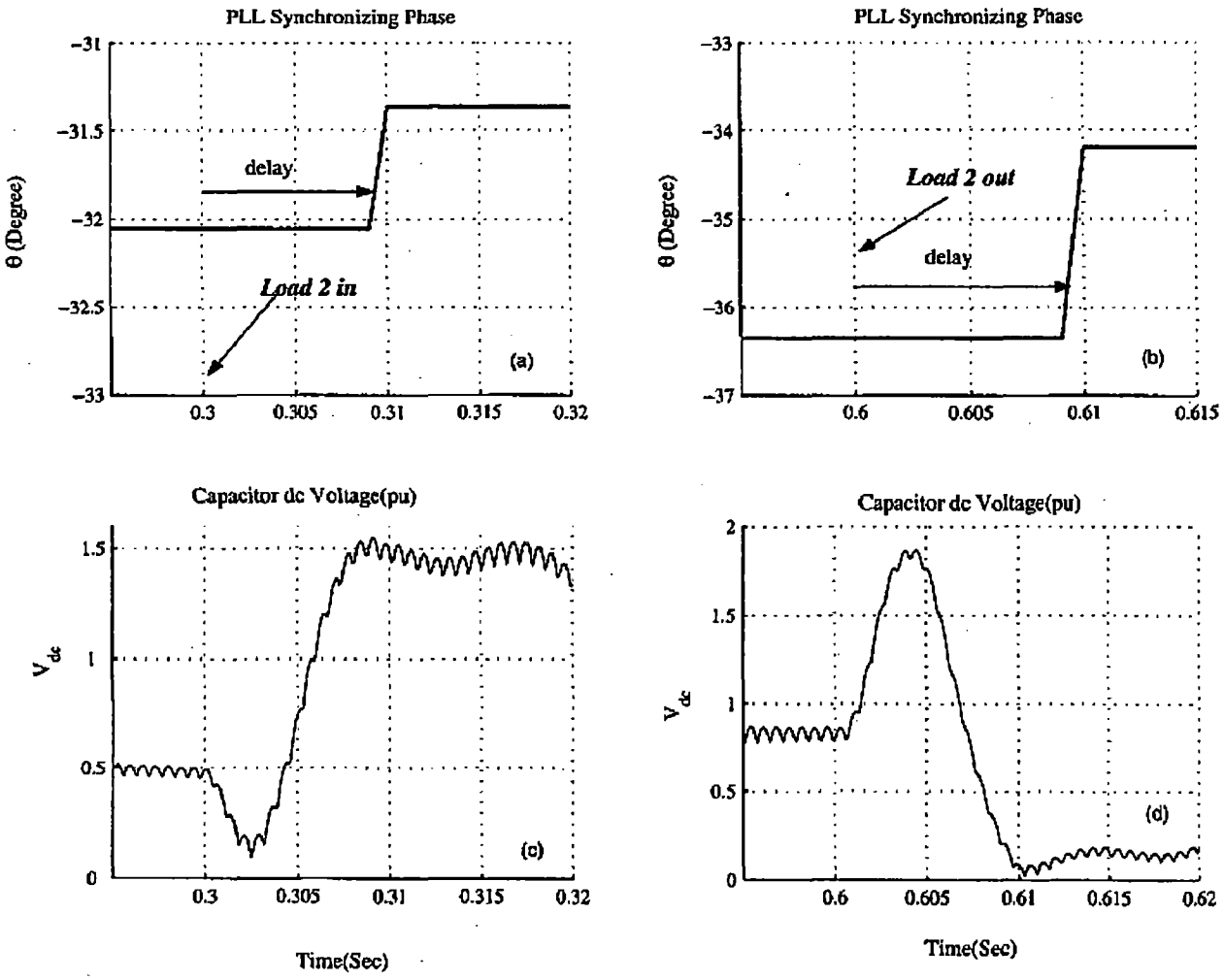


Figure B.3: PLL Phase Angle and dc Capacitor Voltage, Load Switching

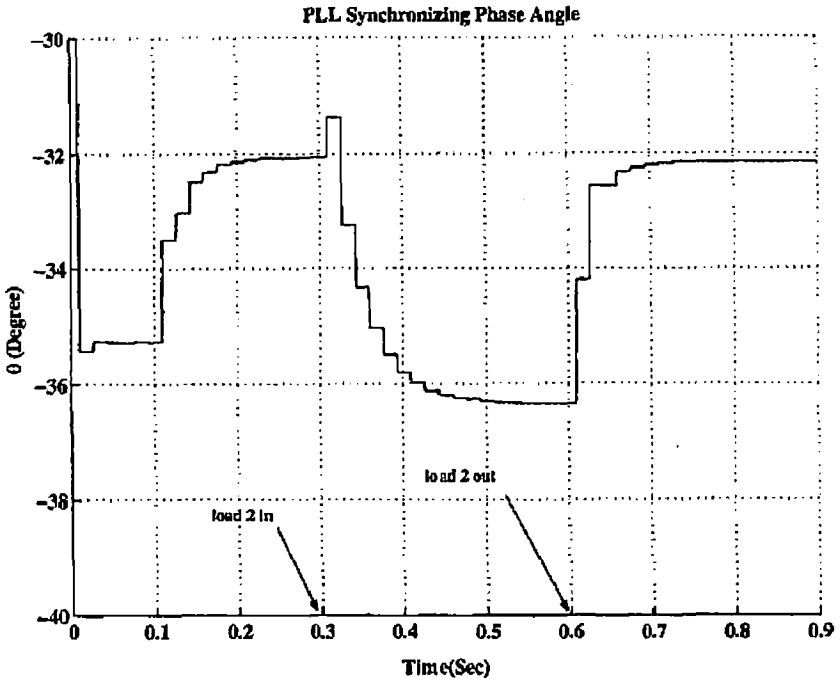


Figure B.4: PLL Synchronizing Phase Angle of the SSSC

4. B.2 AUXILIARY CONTROL DESIGN

A novel auxiliary regulator, using the dc capacitor voltage, was developed to enhance the dynamic performance of the SSSC. One critical design aspect is to select the appropriate control signal. Since the process of losing the synchronization and rapid variations of the dc capacitor voltage occurs very fast, the SSSC series injected voltage, Vs, or reactive power, Qs, can not be selected as the calculation time is long. However, the dc capacitor voltage is readily available and can be measured very fast. Besides, it is an exact sign of losing synchronization and rapid variations due to PLL delay [36].

The key element is the rate of the variations of V_{dc} or ΔV_{dc} / Δt. For a fixed interval of Δt, the variations of V_{dc} can be measured and a rapid change of V_{dc} occurs when $| \Delta V_{dc} |$ is greater than a threshold, k. The value Δt and k depend on the dc capacitor size and the SSSC parameters such as rating power. Besides, Δt and k are not independent, a smaller Δt requires a smaller k, because the rate of variations of Vdc is smaller for shorter Δt. A key factor is to detect the rapid variations very fast, as it happens in only a few milli seconds. Therefore Δt

should be very small and about 1ms. For this short duration, a ΔVdc of over 0.05 pu can be considered fast and due to PLL delay. The exact values of Δt and k are function of the SSSC characteristics and may be obtained by some trial and error for the best result.

After detecting the rapid variations of V_{dc}, the strategy is to correct the phase angle of the SSSC voltage, θ, in accordance with the sign of the variations. If $\Delta V_{dc} > 0$, the dc capacitor is charging very fast. This happens when V_s lags the line current, I_L, by a small amount of less than 90^0 for capacitive operation, or V_s leads I_L by an amount of less than 90^0 for inductive operation. In these cases the real power flows from the transmission line to the dc capacitor. Thus if a small phase angle, Δφ, is added to θ the process of rapid increasing of V_{dc} can be made slower. This phase angle should be small and about 1^0 - 2.5^0, in order to ensure that the SSSC would not be unstable. Similarly if $\Delta V_{dc} < - k < 0$, the dc capacitor is discharging very fast and it shows that V_s lags I_L by an amount of slightly more than 90^0 for capacitive operation, or V_s leads I_L by slightly more than 90^0 for inductive operation. Thus the real power flows from the dc capacitor to the transmission line. In the case, if a small negative phase angle,- Δφ, is added to θ,the process of rapid dc capacitor discharging can become slower [36].

Figure B.5 shows the block diagram of the auxiliary regulator for the SSSC transient enhancement.

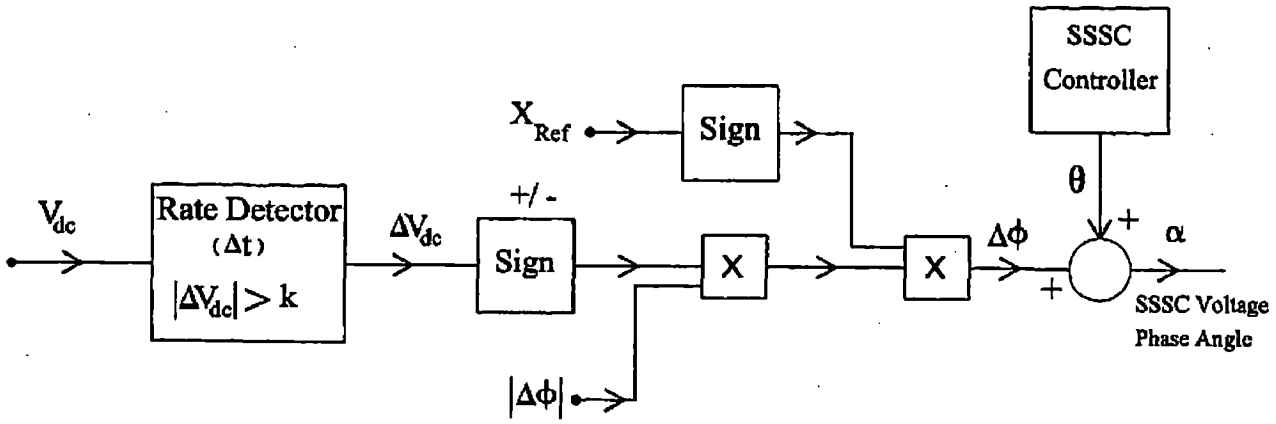


Figure B.5: Block Diagram of the Auxiliary Regulator for the SSSC

V_{dc} is measured in intervals of Δt and if $| \Delta V_{dc} | > k$ the output of the Rate Detector becomes nonzero. Depending on the sign of ΔV_{dc} a positive or negative constant phase angle, $\Delta\varphi$, is selected. The final sign of $\Delta\varphi$, is determined by the operating mode of the SSSC. The auxiliary regulator operates only when $| \Delta V_{dc} | > k$ and other than that a zero angle will be added to θ. Therefore it does not affect the normal operation of the SSSC and only in the case of the PLL delay, improves the dynamic performance of the SSSC.

4. B.2.1 Digital Simulation

In order to validate the new auxiliary regulator, an exact digital simulation was performed, using the system in Figure B.1, while the SSSC is equipped with the new auxiliary regulator. The simulation steps are the same as that of Section B.1.1. ΔV_{dc} is measured in every 0.8 ms ($\Delta t = 0.8$ms) and the threshold k, is set to 0.1 pu, i.e. the output of the Rate Detector is nonzero when $| \Delta V_{dc} | > 0.1$pu. The constant phase angle, $\Delta\varphi$, is set to 2.3^0, which can be selected based on trail and error for the best result.

The simulation results for V_{dc}, Q_s and X_s are shown in Figure B.6 along with the simulation results without the auxiliary regulator from Section B.1.1. The thick line shows the results with and the thin line shows the results without the auxiliary regulator. While the new regulator does not affect the SSSC in normal operation, the results are different at switching instants, t = 0.3 Sec and t = 0.6 Sec. it can be verified that V_{dc} exhibits smaller and slower variations when load 2 is added or rejected. Therefore the SSSC reactive power, Q_s, and series injected, X_s, have much smaller and slower variations that yield to more stable power system.

The thick line is with, and the thin line is without the auxiliary regulator.

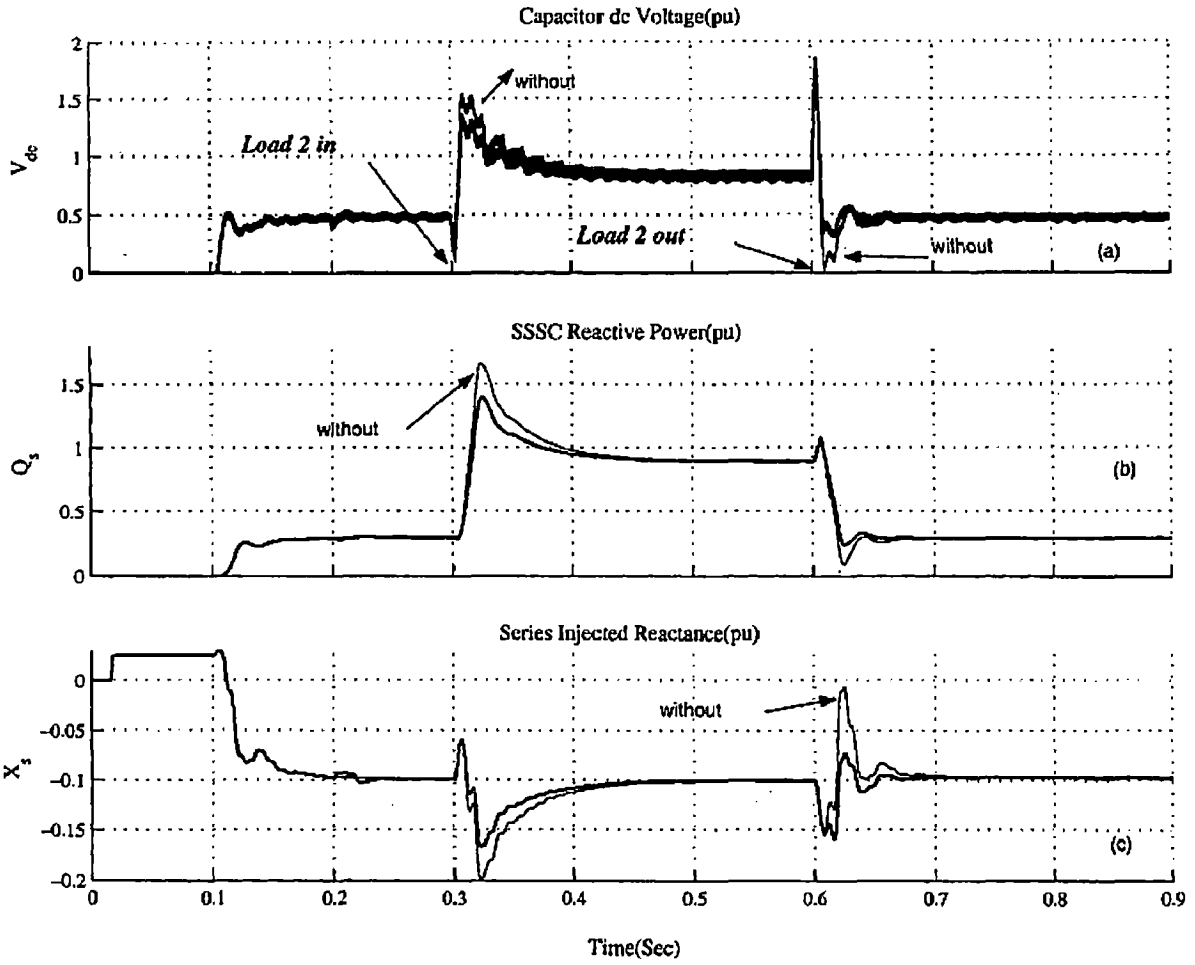


Figure B.6: Simulation of the SSSC with and without the Auxiliary Regulator

Figure B.7 and B.8 show the simulation results at switching instants, t = 0.3 Sec and t = 0.6 Sec. The thick line is with and the thin line is without the auxiliary regulator. They clearly show the effect of the new regulator on the SSSC dynamics in more details.

Figure B.9 shows the auxiliary regulator phase angle, $\Delta\varphi$, at switching instants. It comes into effect only when $|\Delta V_{dc}|$ exceeds the threshold, k.

4. B.3 CONCLUSION

The auxiliary regulator, using the dc capacitor voltage, is an effective tool to improve the dynamic performance of the SSSC. Since it is based on the dc capacitor voltage, it can be easily implemented at the SSSC location and proves to be effective in reducing the transient variations of the power system, such as line current and bus voltage. However, the uncontrolled

variations in dc capacitor voltage, as the main reason for the SSSC oscillatory operation, can not be fully prevented. The main reason is the transmission line current transient at load switching instants which causes a quasi dynamic line current. This dynamic characteristic of the line current causes an uncontrolled real power exchange between the SSSC and the transmission system, even if they are exactly in phase. So the new auxiliary regulator will damp and reduce the fast real power exchange between the SSSC and the transmission system and therefore reduce the oscillations of the dc capacitor voltage.

The thick line is with, and the thin line is without the auxiliary regulator.

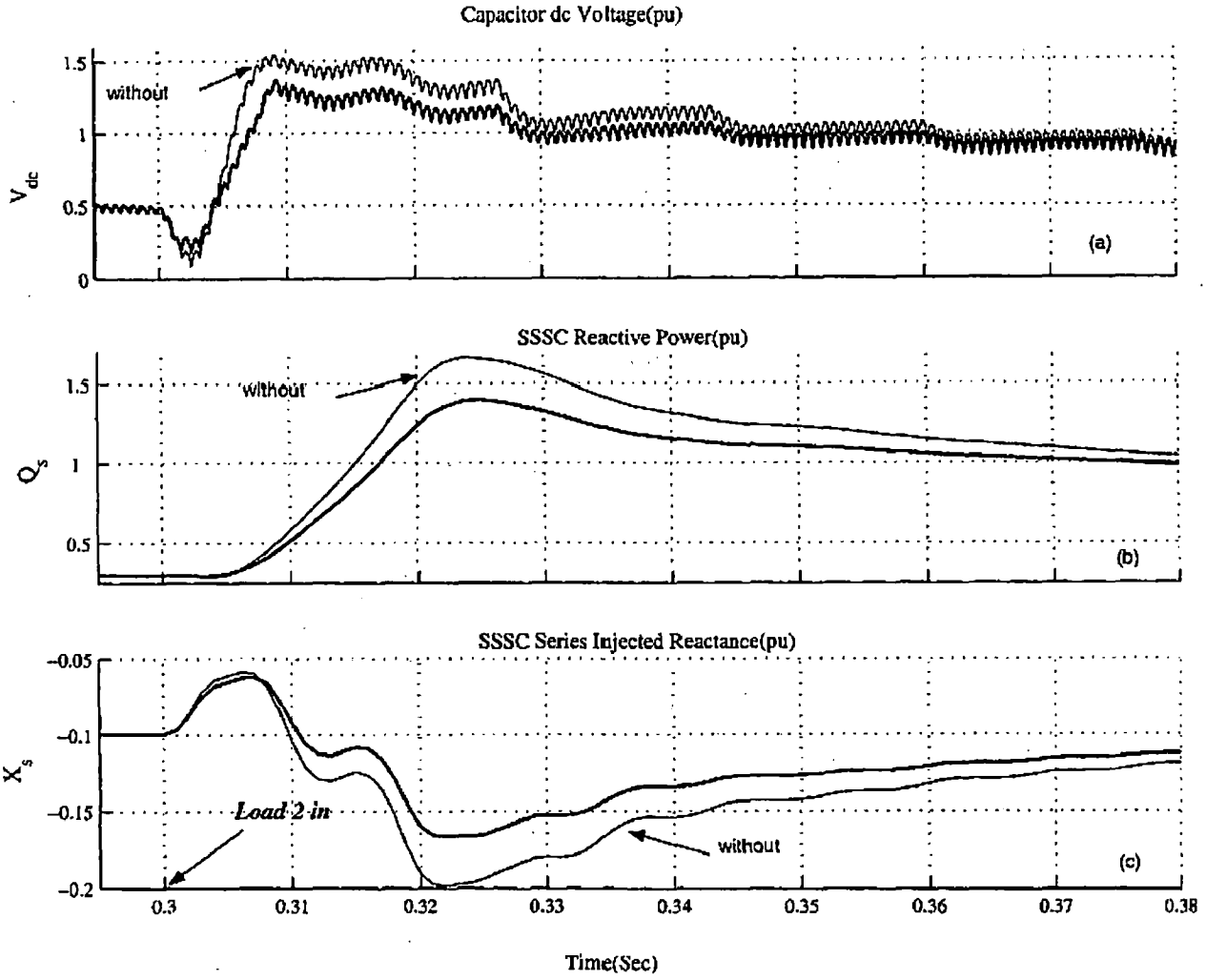


Figure B.7: SSSC Performance with and without the Auxiliary Regulator (Load Switched in)

The thick line is with, and the thin line is without the auxiliary regulator.

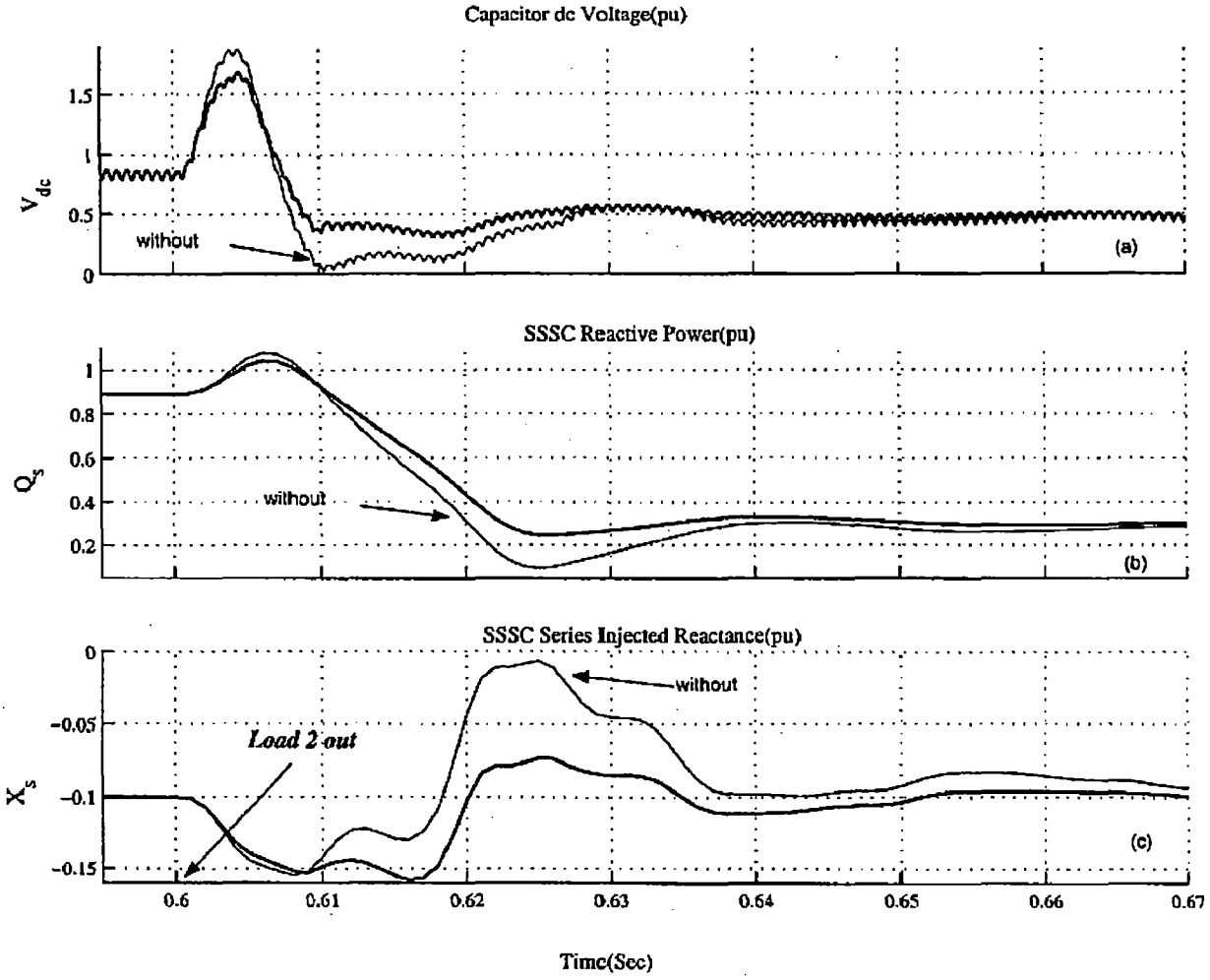


Figure B.8: SSSC Performance with and without the Auxiliary Regulator (Load Switched out)

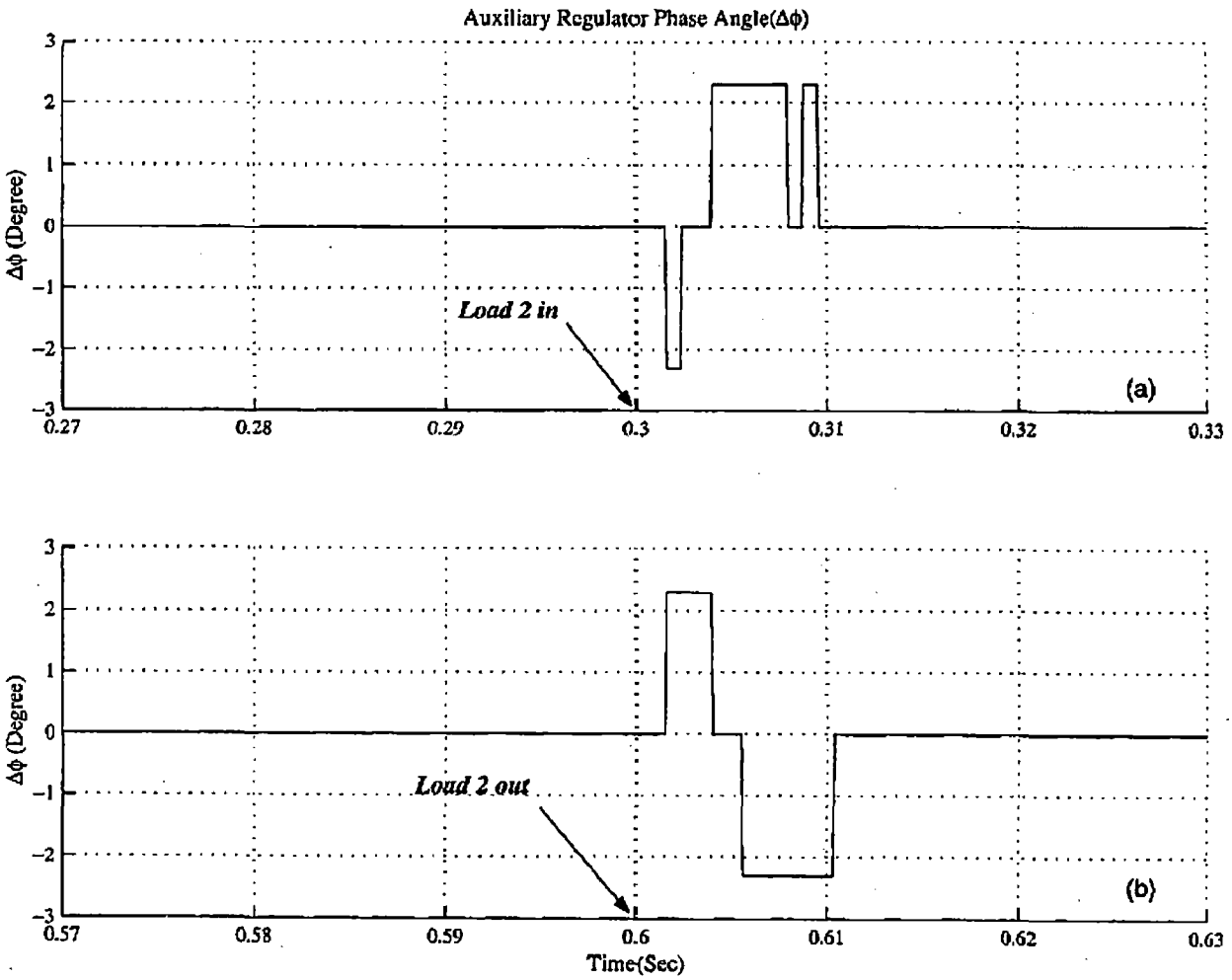


Figure B.9: Auxiliary Regulator Phase Angle, Δφ, at Switching Instants

4. C POWER SYSTEM BLOCKSET (PSB)/SIMULINK MODELS

4. C.1 24-PULSE CONVERTER

The configuration of a 24-pulse converter was presented in Chapter 2. In order to model the converter, four GTO, six-pulse Universal Bridges of the PSB were employed with the required four coupling transformers. The Universal Bridge is the basic six-pulse DC-AC converter and the self-commutated solid state switches were selected as GTO.

The basic delay unit which applies a variable phase angle delay to the gate pulses of a GTO is shown in Figure C.1.

By combining three of the phase angle delay units, the required six gating pulses for a six-pulse, DC-AC, GTO converter is obtained as shown in Figure C.2.

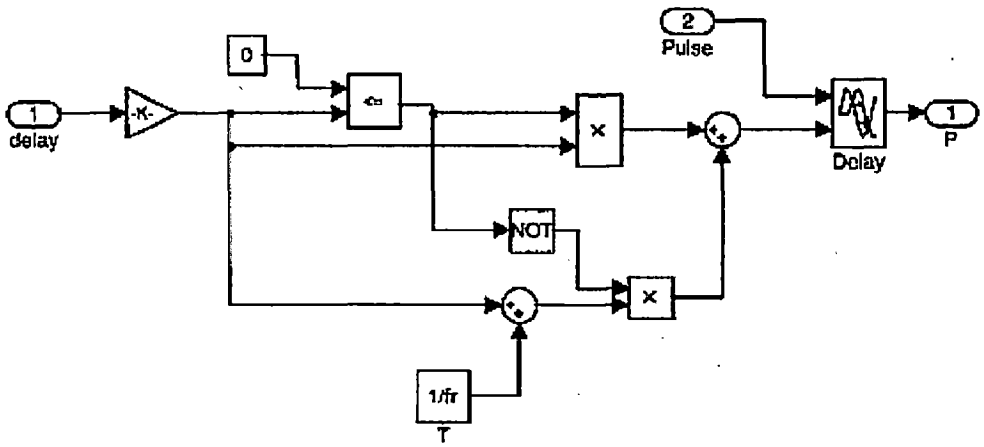


Figure C.1: Basic Phase Angle Delay Unit for the GTO Pulses

Figure C.3 shows the six-pulse converter, with variable phase angle delay, using the Universal Bridge of PSB. It is a complete six-pulse, GTO converter, as the basic building block of a 12 or 24 converter.

A 12-pulse converter is obtained by combining two six-pulse converters, with appropriate phase angles and transformer ratios, as described in Chapter 2. Figure C.4 shows the PSB model of the 12-pulse GTO converter.

Finally, by combining two 12-pulse converters, 24-pulse, GTO converter with variable phase angle delay is obtained which is the basic building block of the STATCOM and SSSC. Figure C.5 shows the PSB model of the 24-pulse converter.

Since each GTO and free-wheeling diode is modeled as a nonlinear switch and there are many such switches in a 24-pulse converter, a discrete solver be used for digital simulation. For the 24-pulse converter, a variable step discrete solver with step size of 10 μSec provides accurate result.

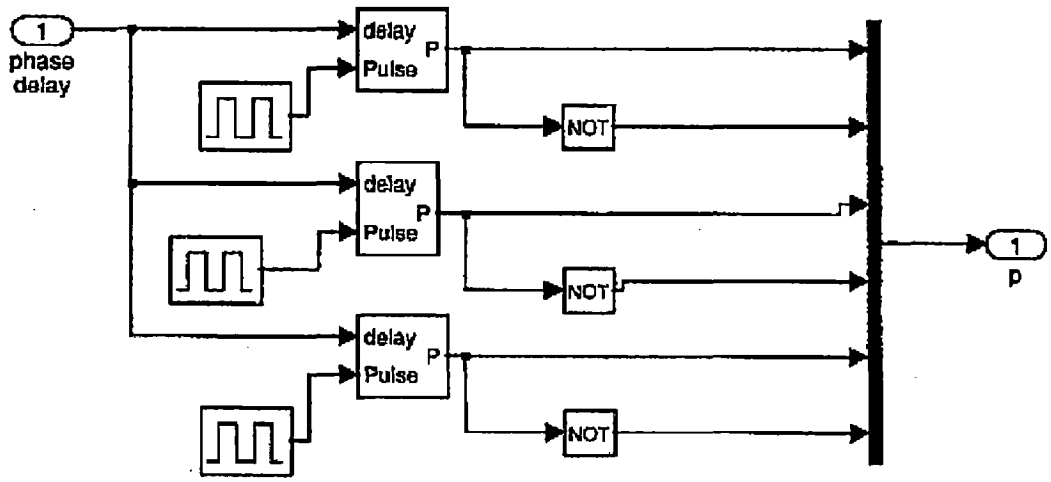


Figure C.2: Gate Pulse Generator of a Six-Pulse Converter with Variable Phase Angle Delay

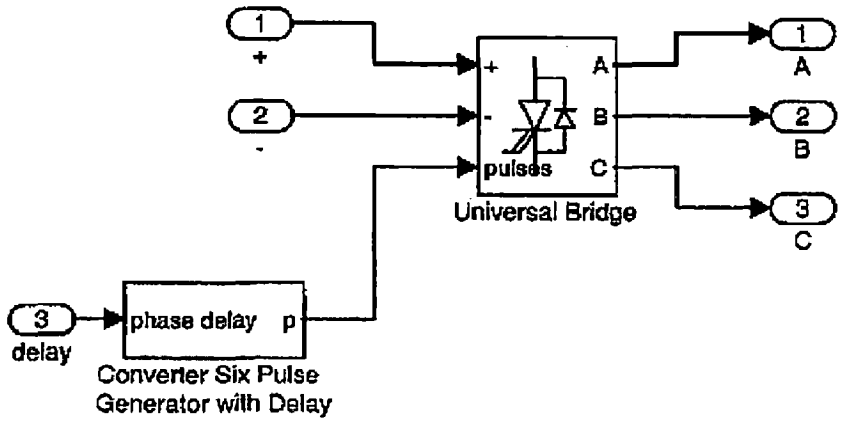


Figure C.3: Six-Pulse GTO Converter with Variable Phase Angle Delay

The inputs to the converter are the dc input voltage (1,2) and the gating pulses that come from the pulse generator block.

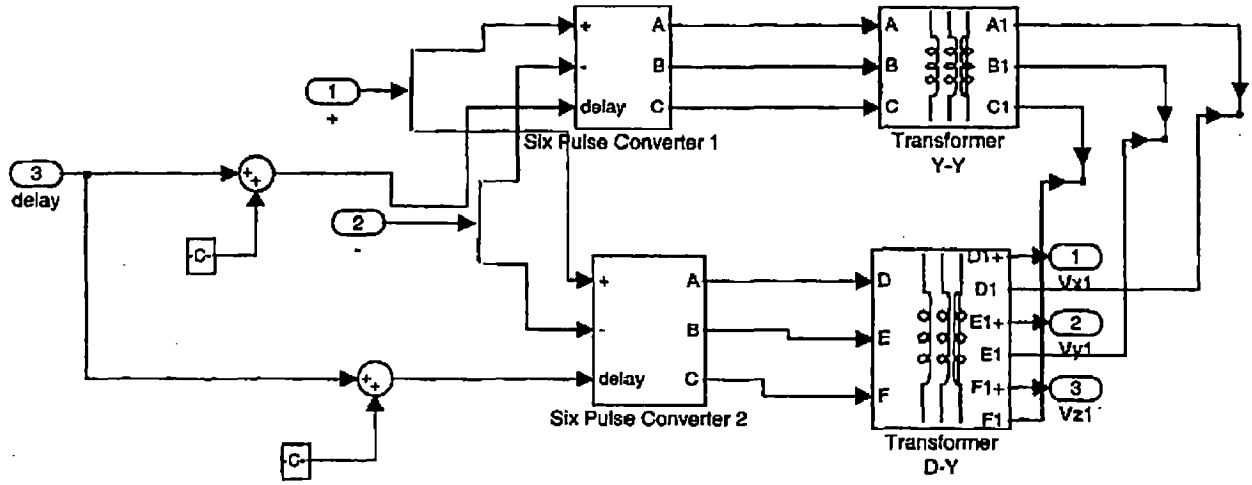


Figure C.4: PSB Model of the 12-Pulse Converter

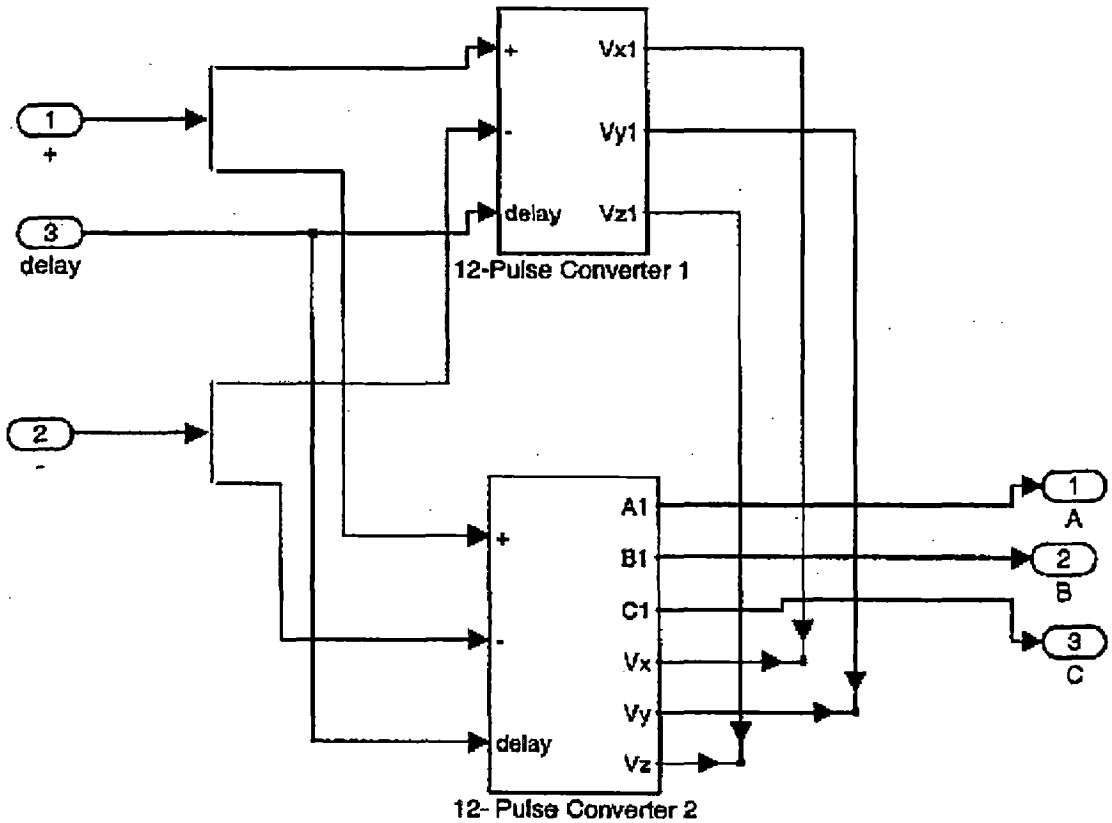


Figure C.5: PSB Model of the 24-Pulse Converter

4. C.2 STATCOM

By using the 24-pulse converter model, the STATCOM can be modeled within a power transmission system. Figure C.6 shows the Phase-Locked Loop (PLL) model. It provides the synchronizing signal for the STATCOM which is the phase angle of the STATCOM bus voltage. The zero crossing of the bus voltage is compared with the zero crossing of a reference sine wave and the phase angle is obtained. A step size of 1 μSec is required to get an accurate result with a voltage frequency of 60Hz. Figure C.7 shows the STATCOM model within a power transmission system. This model was used to get the results of Chapter 3 and Appendix A. It consists of many PSB and Simulink blocks and some block systems consist of other subsystems that are not shown here. Since there are many nonlinear switches in the system such as GTO's and diodes of the 24-pulse converter, only a discrete method can solve the system equations. Therefore the whole system was discretized with the step size of 1 μSec. For the dq transformation, transformers and loads, the PSB provides the required blocks.

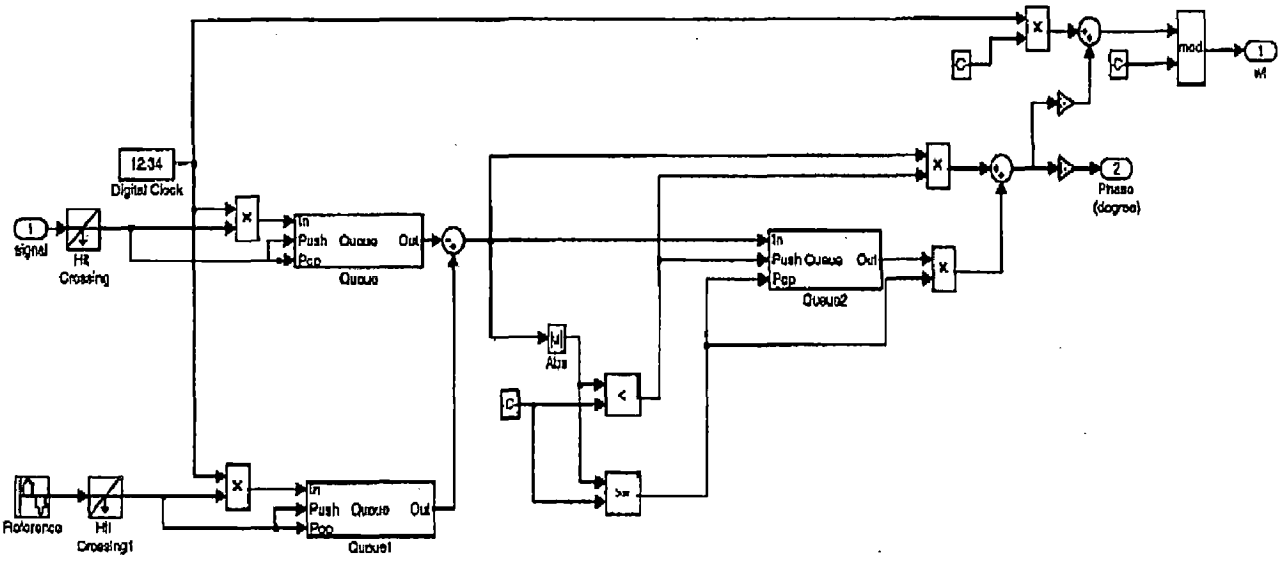


Figure C.6: Phase-Locked Loop Model

Input 1 is the input signal whose zero crossing is compared with the zero crossing of a Reference signal and the phase angle is calculated. Output 1 is wt of the input signal which is

used for d-q transformation and output 2 is the phase angle of the input which is the synchronization signal.

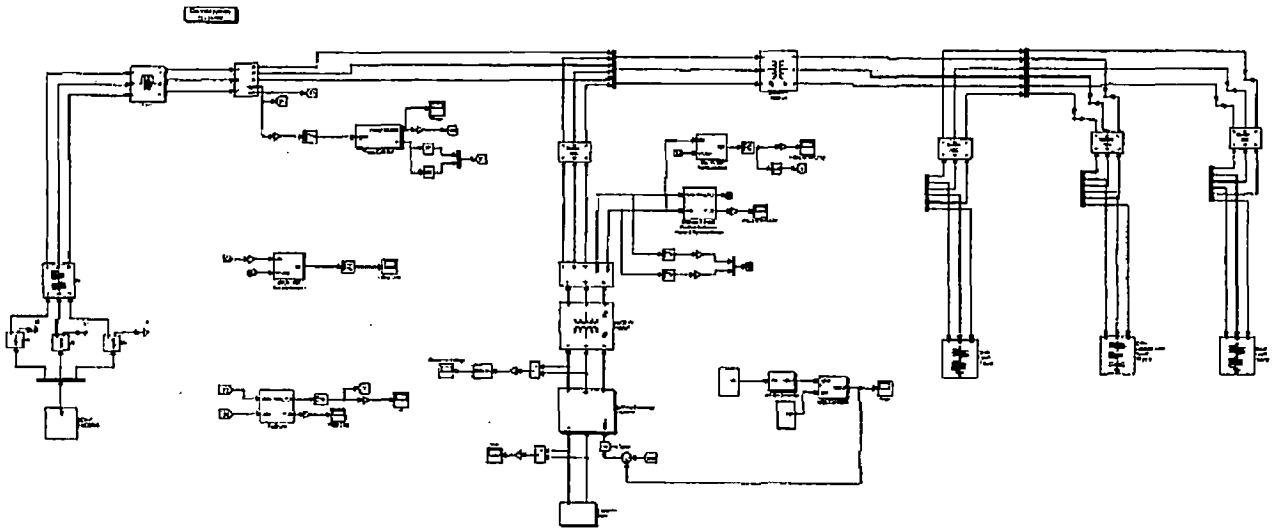


Figure C.7: STATCOM Model within a Power Transmission System

4. C.3 SSSC

By using the 24-pulse converter model, the SSSC can be modeled within a power transmission system. Figure C.8 shows the SSSC model within a power transmission system. This model was used to obtain the results of Chapter 4 and Appendix B. it consists of many PSB and Simulink blocks and some block systems consists of other subsystems that are not shown here.

4. C.4 AUTOMATIC GAIN CONTROLLER (AGC)

Figure C.9 shows the AGC model that was used in Appendix B. The maximum and minimum of voltage regulator output, I_{qRef}, are obtained in intervals of 40 ms and after eliminating the oscillation due to PLL delay, by Unit Delay block, based on ΔI_{qRef} a variable gain, K, is applied, ,by Nonlinear Gain block. The details of Unit Delay and Nonlinear Gain blocks are not shown here.

4. C.5 AUXILIARY REGULATOR

Figure C.10 shows the auxiliary regulator model that was used in Appendix B. The dc capacitor voltage, Vdc, in monitored and its rate of change is obtained in intervals of 0.8ms. If rate of change exceeds 0.1pu, depending on the SSSC mode of operation and the sign of change, a positive or negative phase angle, $\Delta\varphi$, is selected. This phase angle would be added to the SSSC voltage phase angle. The details of Phase Compensator block are not shown here.

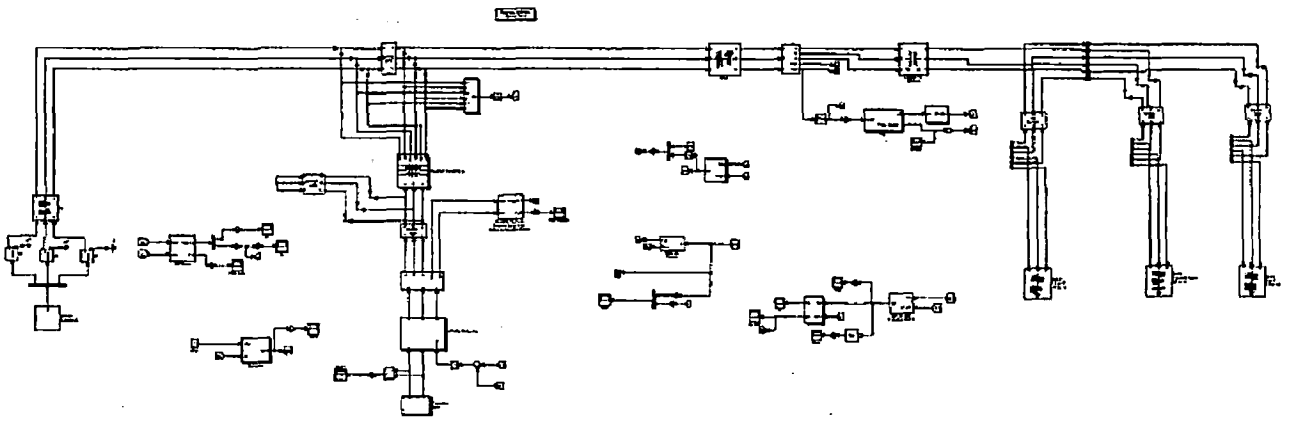


Figure C.8: SSSC Model within a Power Transmission System

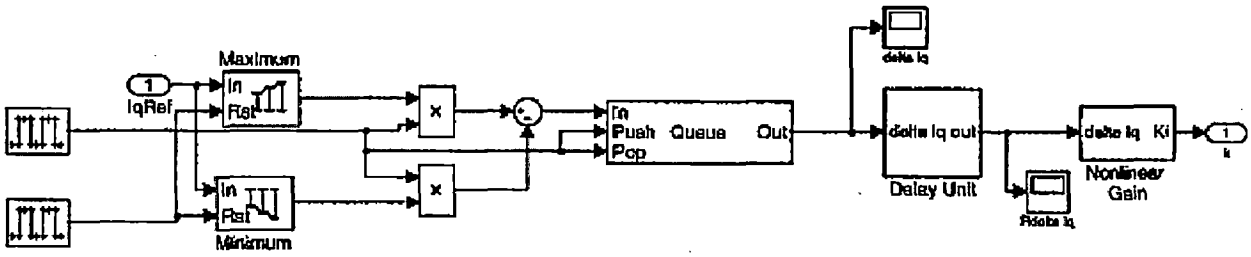


Figure C.9: Automatic Gain Controller Model

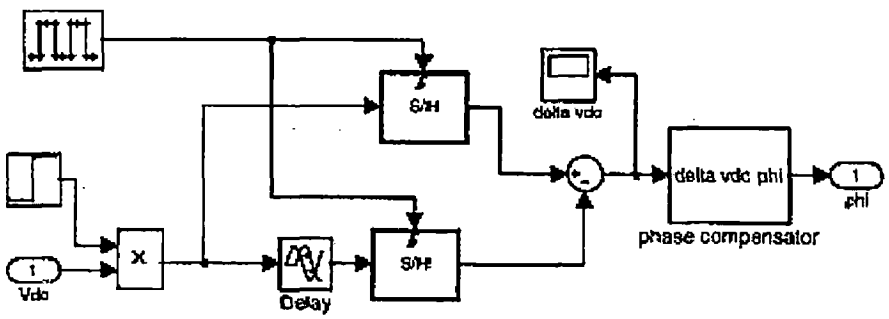


Figure C.10: Auxiliary Regulator Model

5.0 THYRISTOR –CONTROLLED REACTOR (TCR)

It is not only required to meet the demand for electrical energy but also to improve its quality. Today, power quality studies are becoming a growing concern. The present paper focuses on two parameters affecting power quality – harmonics and voltage stability. Static VAR compensators (SVCs) are applied on transmission systems to improve voltage control and system stability during both normal and contingency system conditions. Most SVCs use a thyristor-controlled reactor configuration to provide continuous control of the reactive power compensation level. The thyristor-controlled reactor (TCR) produces harmonic currents because thyristors only allow conduction in the reactor for a portion of the cycle.

Harmonic current magnitudes vary as the firing angle of the thyristors is varied. A comprehensive harmonic study includes evaluation of possible harmonic concerns over the full range of firing angles and possible system conditions. Generally, harmonic filtering is accomplished with capacitors connected in parallel with the TCRs. For transmission applications, the filters might include tuned filters at the fifth and seventh harmonics along with a high pass filter for higher order components.

Use of a static compensator with a thyristor-controlled reactor (TCR) has been known to be an effective and reliable means to ensure power system voltage stability. This device is essentially a variable reactor that can adjust its reactive power consumption. The adjustment is realised through the firing angles of thyristors that normally operate in partial conducting states, and thereby produce harmonics (Miller 1982). The generated harmonics depend critically on the control characteristics of a static VAR compensator (SVC) with a fixed-capacitor thyristor-controlled reactor (FC-TCR). However, this makes the firing angles dependent on the network load flow conditions and harmonic voltage distributions (Xu *et al*

1991). Poor selection of firing angles can lead to increase in the amount of effective harmonic production of the TCR. From the operation point of view of the system, we need to model the harmonics accurately (Uzunoglu *et al* 1999).

In the literature, work on stability analyses has mostly been done on transients. In this study, however, steady-state stability analysis of a system including the harmonics of FC-TCR has been carried out employing a new algorithm. This paper aims to determine the effects of non-sinusoidal quantities on voltage stability, due to a FC-TCR, by means of a synthesis of harmonic power flow analysis and voltage stability analysis based on the Newton–Raphson method.

5.1 THYRISTOR –CONTROLLED RECTOR AS HARMONIC SOURCE

Thyristor-controlled reactors, which have the ability to ensure continuous and fast reactive power and voltage control, can increase the performance of the system in different ways such as control of transient over-voltages at the power frequency, prevent ion of voltage collapse, increase in transient stability and decrease in system oscillations. Static VAR compensators consisting of thyristor-controlled reactors are used for balancing the three-phase systems.

The basic static VAR system (SVS) consists of a static switch in series with an inductor. This is normally called a phase-controlled reactor or thyristor-controlled reactor (TCR). This basic TCR is illustrated in figure 1a. The thyristor-controlled reactor consists of a reactor in series with two parallel inverse thyristors. The two inverse parallel thyristors are gated symmetrically. They control the time for which the reactor conducts and thus control the fundamental component of the current. The thyristors conduct on alternate half-cycles of the supply frequency depending on the firing angle α or conduction angle σ, which is measured from a zero crossing of voltage.

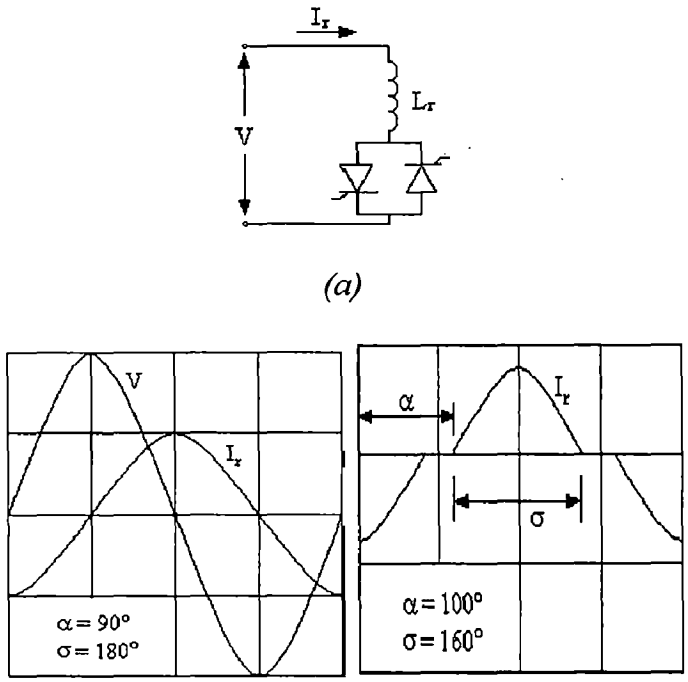


Figure 5.1 : (a) Main Elements of a TCR. (b) Voltage and Current Waveforms in a TCR.

The relation between firing angle and conduction angle as follows:

$$\sigma = 2(\pi - \alpha) \tag{5.1}$$

Full conduction is obtained with a firing angle of 90°. Under this condition, the current is reactive and its waveform is purely sinusoidal. There is a partial conduction between $90^0$and 180^0 as shown in figure 1b (Miller 1982). The firing angle is not allowed to have values between 0^0 and 90^0, causing asymmetrical currents including DC components. When the firing angle α increases from 90^0 to 180^0, the waveform of the current goes away from the original sinusoidal form. For the condition of balanced loading, TCR produces odd harmonics. In a three-phase system where the TCR's are _-connected there are no triplet harmonics injected into the power system (Lasseter & Lee 1982). However, TCR circuits should not be operated at points near resonance as they would generate conditions causing effective harmonic production (Bohmann & Lasseter 1986).

5.2 STABILITY AND HARMONICS

It is necessary to pay attention to energy system stability in the planning, management, and control of electrical power systems for more reliable and "quality" energy (Anderson & Fouad 1994). Stability in an energy system is defined as the ability of returning to the earlier operating condition after a distortion effect (Begovic & Phadke 1992). In voltage stability, the amplitude values of the load bus voltages of the system should be kept between determined limit values in both steady-state and transient conditions.

Continuous decrease in the source voltage due to increase in load demand or change in system conditions, causes voltage instability in a system. The main reason for instability is insufficient reactive power not corresponding to the demand. In order to prevent this deficiency, static VAR compensator including TCR should be used (Indulkar *et al* 1989). Owing to the use of power electronics for static VAR compensation, the power system suffers from instability under some operating conditions (Uzunoglu *et al* 2000). Due to the nonlinear characteristics of TCR, a new algorithm based on harmonic power flow should be developed to perform steady-state voltage stability analysis.

5.2.1 Harmonic Power Flow Algorithm

Network voltages and currents can be expressed by Fourier series for the harmonic power flow analysis, which was developed by Xia & Heydt (1982). Voltages and nonlinear element parameters form the bus variable vector (Φ), given in

$$[X] = \left[[\dot{V}^{(1)}], [\dot{V}^{(5)}], \ldots, [\dot{V}^{(L)}], [\phi]\right]^T . \tag{5.2}$$

In this equation, L is the maximum harmonic order. The mismatch of real and reactive powers for the linear buses (while $k \in \{2, \ldots, (m-1)\}$) is defined as,

$$\left.\begin{aligned} \Delta P_k &= (P_k)_{SP} + F_{r,k}^{(1)} \\ \Delta Q_k &= (Q_k)_{SP} + F_{i,k}^{(1)} \end{aligned}\right\}, \tag{5.3}$$

where m is the first nonlinear load number and the first bus is the slack bus in this number. $(P_k)_{SP}$ and $(Q_k)_{SP}$ are real and reactive powers at bus k respectively, and $F^{(1)}_{r,k}$ and $F^{(1)}_{i,k}$ are the line fundamental real and reactive powers. The mismatch of real and reactive powers can be calculated for nonlinear buses as,

$$\left.\begin{aligned}\Delta P_k^{\text{nonlin}} &= (P_k)_{SP} + \sum_{h=1}^{L} F_{r,k}^{(h)} \\ \Delta Q_k^{\text{nonlin}} &= (Q_k)_{SP} + \sum_{h=1}^{L} F_{i,k}^{(h)}\end{aligned}\right\}, \tag{5.4}$$

where $k \in \{m, m+1, \ldots, n\}$ and n is total number of the buses in the system. $F^{(h)}_{r,k}$ and $F^{(h)}_{i,k}$ can be calculated from (for $h = 1, 5, 7, \ldots, L$),

$$\left.\begin{aligned}F_{r,k}^{(h)} &= V_k^{(h)} \sum_{j=1}^{n} Y_{jk}^{(h)} \cdot V_j^{(h)} \cdot \cos\left(\delta_k^{(h)} - \theta_{kj}^{(h)} - \delta_j^{(h)}\right) \\ F_{i,k}^{(h)} &= V_k^{(h)} \sum_{j=1}^{n} Y_{jk}^{(h)} \cdot V_j^{(h)} \cdot \sin\left(\delta_k^{(h)} - \theta_{kj}^{(h)} - \delta_j^{(h)}\right)\end{aligned}\right\}. \tag{5.5}$$

The harmonic phasor voltage the for k^{th} bus is $\dot{V}_k^{(h)} = V_k^{(h)} \angle \delta_k^{(h)}$ and element (k, j) of the bus admittance matrix calculated for the h^{th} harmonic frequency is shown in phasor notation as

$$\dot{Y}_{kj}^{(h)} = Y_{kj}^{(h)} \angle \theta_{kj}^{(h)}.$$

Here, the mismatch vector for the harmonic power flow is defined as (Grady 1983),

$$[\Delta \mathbf{M}] = \left[[\Delta W], [\Delta I^{(5)}], [\Delta I^{(7)}], \ldots, [\Delta I^{(L)}], [\Delta I^{(1)}]\right]^T, \tag{5.6}$$

where ΔW is the mismatch power vector and $\Delta I^{(h)}$ is the mismatch current vector for the h^{th} harmonic. The mismatch power is given by

$$\begin{aligned}[\Delta W] = \big[&\Delta P_2, \Delta Q_2, \ldots, \Delta P_{m-1}, \Delta P_m^{\text{nonlin}}, \\ &\Delta Q_m^{\text{nonlin}}, \ldots, \Delta P_n^{\text{nonlin}}, \Delta Q_n^{\text{nonlin}}\big].\end{aligned} \tag{5.7}$$

The mismatch current vector for the fundamental component $(h = 1)$ and the harmonic component $(h = 5, 7, \ldots, L)$, which are the elements of the mismatch vector is given respectively by

$$[\Delta I^{(1)}] = \left[\left(I_{r,m}^{(1)} + g_{r,m}^{(1)}\right), \left(I_{i,m}^{(1)} + g_{i,m}^{(1)}\right), \left(I_{r,m+1}^{(1)} + g_{r,m+1}^{(1)}\right), \left(I_{i,m+1}^{(1)} + g_{i,m+1}^{(1)}\right), \ldots, \left(I_{r,n}^{(1)} + g_{r,n}^{(1)}\right), \left(I_{i,n}^{(1)} + g_{i,n}^{(1)}\right)\right]^r,$$

$$[\Delta I^{(h)}] = \left[I_{r,1}^{(h)}, I_{i,1}^{(h)}, \ldots, I_{r,m-1}^{(h)}, I_{i,m-1}^{(h)}, \left(I_{r,m}^{(h)} + g_{r,m}^{(h)}\right), \left(I_{i,m}^{(h)} + g_{i,m}^{(h)}\right), \left(I_{r,m+1}^{(h)} + g_{r,m+1}^{(h)}\right), \left(I_{i,m+1}^{(h)} + g_{i,m+1}^{(h)}\right), \ldots, \left(I_{r,n}^{(h)} + g_{r,n}^{(h)}\right), \left(I_{i,n}^{(h)} + g_{i,n}^{(h)}\right)\right]^r. \quad (5.8)$$

In these equations, $I^{(h)}{}_{r,k}$ and $I^{(h)}{}_{i,k}$ are to be zero for the harmonic components at linear buses $(k = 1, 2, \ldots, m-1)$.

The Newton–Raphson method is implemented to obtain the correction vector by using the Jakobian matrix. When the mismatch goes to zero for every term of mismatch vector, a solution can be obtained (Arrillaga *et al* 1983). Thus, by using the Newton–Raphson method, we can get the solution with the desired tolerance (in this study, the tolerance for the mismatch is taken as 0·0001 per unit. The correction vector is given as

$$[\Delta \mathbf{X}] = [\mathbf{J}]^{-1}.[\Delta \mathbf{M}] \quad (5.9)$$

The harmonic power flow analysis algorithm is given in appendix A (Masoum 1991).

5.3 TCR ANALYSIS METHOD

The values obtained from linear power flow analysis are used in steady-state voltage stability analysis performed with conventional methods. It is required to develop a new algorithm to analyse steady-state voltage stability in case the system has a nonlinear element. Synthesis of the harmonic power flow algorithm and the voltage stability algorithm is done, and a new algorithm is developed to realize this analysis (Uzunoglu *et al* 2002). When the Jakobian of a Newton–Raphson power flow becomes singular, the steadystate voltage stability limit (critical point) of the system can be determined easily and rapidly.

By using data obtained from harmonic power flow, the critical values are calculated for fundamental and harmonic components separately. According to this method, critical

transmission angle, δ_{critical}, critical load voltage, V_{critical}, and critical load power, P_{critical}, are given by (Indulkar 1989)

$$\delta_{\text{critical}}^{(h)} = 1/2 \tan^{-1}(K_1/K_2), \tag{5.10}$$

where,

$$K_1 = a_1^{(h)}\left(b_2^{(h)} - b_1^{(h)} \tan\varphi^{(h)}\right) + a_2^{(h)}\left(b_1^{(h)} + b_2^{(h)} \tan\varphi^{(h)}\right), \tag{5.11}$$

$$K_2 = a_1^{(h)}\left(b_1^{(h)} + b_2^{(h)} \tan\varphi^{(h)}\right) + a_2^{(h)}\left(-b_2^{(h)} + b_1^{(h)} \tan\varphi^{(h)}\right), \tag{5.12}$$

$$V_{\text{critical}}^{(h)} = V_s^{(h)}/2 \cdot K_4, \tag{5.13}$$

and

$$P_{\text{critical}}^{(h)} = \left\{\left(V_s^{(h)}\right)^2 \cdot \left[2K_3K_4 - \left(a_1^{(h)}b_1^{(h)} + a_2^{(h)}b_2^{(h)}\right)\right]\right\} \Big/ \left\{4 \cdot (K_4)^2 \cdot \left[\left(b_1^{(h)}\right)^2 + \left(b_2^{(h)}\right)^2\right]\right\}, \tag{5.14}$$

where,

$$K_3 = b_1^{(h)} \cos\delta_{\text{critical}}^{(h)} + b_2^{(h)} \sin\delta_{\text{critical}}^{(h)}, \tag{5.15}$$

$$K_4 = a_1^{(h)} \cos\delta_{\text{critical}}^{(h)} + a_2^{(h)} \sin\delta_{\text{critical}}^{(h)}, \tag{5.16}$$

where h = 1, 5, 7, . . . ,L. TCR is modelled suitably for the algorithm developed for the analysis. TCR's current for harmonic components is defined as (Bohmann & Lasseter 1989)

$$I_r^{(h)} = \left\{2 \cdot V_r^{(h)}/h.X_r^{(1)}\right\}\left\{\cos\left(\delta_r^{(h)}\right) - \cos\{h \cdot ((\pi - \sigma)/2)\} + j \cdot \left[\sin\left(\delta_r^{(h)}\right) - \sin\{h \cdot ((\pi - \sigma)/2)\}\right]\right\}, \tag{5.17}$$

where Vr is reactor terminal voltage, δr is its angle, σ is thyristor conduction angle, Xr is the reactance of the reactor, and h is the harmonic order. Also, reactor admitance depending on thyristor conduction angle can be defined as follows (Bohmann & Lasseter 1986),

$$Y_r^{(h)}(\sigma) = -j\{\sigma - [\sin(h\sigma)]/h\} / \left\{hX_r^{(h)}\pi\right\}. \tag{5.18}$$

Equivalent suseptance is calculated by using the capacitor reactance of FC-TCR as,

$$B^{(h)}(\sigma) = \left[Y_r^{(h)}(\sigma) - \left(1/X_c^{(h)}\right)\right]. \tag{5.19}$$

In this study, the steady-state voltage stability analysis for power system including FC-TCR was done by the following solution algorithm:

Step 1: The harmonic power flow analysis for the available operation conditions of an example system is done to compute load angle, voltage and power of all buses.

Step 2: Power at all buses except the slack bus and the bus considered for voltage stability are transformed into shunt admittance by using bus voltages obtained from the harmonic load flow for fundamental and harmonic components with the following equations individually,

$$R = (V^2/P),\ X = (V^2/Q) \Rightarrow Y = (1/R) + (1/jX). \tag{5.20}$$

Step 3: These shunt admittances are added to the bus admittance matrix by taking their directions into consideration (these operations are not performed for the slack bus and the bus considered for voltage stability).

Step 4: After obtaining the new bus admittance matrix, the matrix is reordered. In this case, the elements of the bus considered for voltage stability are in the first row and first column, and the elements of the slack bus are in the second row and second column.

Step 5: The elements at the other buses are reduced to the slack bus and the considered bus by the matrix algebra method. The final reduced matrix *(2×2)* is obtained by making new orders at the bus admittance matrix as,

$$\mathbf{Y_{bus}} = \begin{bmatrix} \mathbf{K} & \mathbf{L} \\ \mathbf{L^T} & \mathbf{M} \end{bmatrix} \Rightarrow \mathbf{Y_{bus}}\ (2 \times 2) = \mathbf{K} - \mathbf{L}.\mathbf{M}^{-1}.\mathbf{L}^{\mathbf{T}}. \tag{5.21}$$

Step 6: Critical values are calculated for the final 2-bus system using the Jacobian matrix obtained from singular harmonic power flow (det[J] = 0). Thus, critical values of the bus examined for the voltage stability are calculated by considering the harmonic components when the FC-TCR is connected to the power system. We also examine how FC-TCR affects the power system voltage stability and the reactive power values.

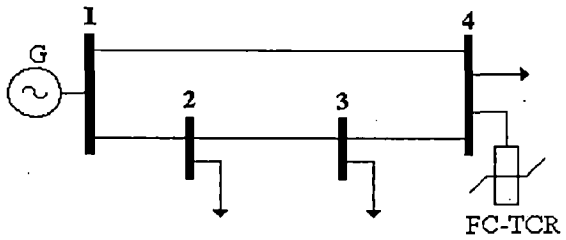


Figure5.2: Single Line Diagram of Example System Including FC-TCR.

5. 4 NUMERICAL APPLICATION

In this study, the effect of the harmonics on voltage stability has been analysed for a 4-bus power system including FC-TCR (Figure 2). Conventional and new voltage stability analyses (depending on harmonic power flow) have been used to perform the study, and the results have been compared.

The per-unit (p.u.) values of lines in the example system have been obtained for 66 kV and 10MVA base values. The characteristic values of the line and the load data of the systems are given in tables 1 and 2 respectively. All transmission lines are modelled using the same model, the lumped parameters π model, and bus-1 as the slack bus in the example system.

The static compensator with FC-TCR is connected to bus-4. There are no filters at all. The values in the application have been taken as per-unit; Hence, the reactance of TCR Xr = 0·55 p.u., capacitor reactance Xc = 2·2 p.u. and fundamental frequency f = 50 Hz. Analyses have been done and compared using the related algorithms developed based on both linear and harmonic power flows (Figures 3–8).

Results of the analyses in which harmonic components are neglected (sinusoidal condition), are denoted by a "+" symbol, while the analyses in which harmonic components are considered (non-sinusoidal condition) are denoted by the "•" in figures 4–8. When conduction angle, σ, is between $0^0$and 180^0, the ratio of harmonic current components (5, 7, 11, 13) / fundamental current component (HDI4) has been shown (as percentage) in figure 3 for TCR at

bus-4. For both conditions, the variation of reactive power for all conduction angles is shown in Figure 4.

From the point of steady-state voltage stability, the conduction angles of TCR are 70^0, $105^0$and 160^0 and the variations of critical voltage in the frequency domain at bus-4 are given in figures 5, 6 and 7 respectively.

Variations of critical power values obtained from steady-state voltage stability analysis at bus-4 and bus-3 are illustrated in Figure 8 and 9 for all conduction angles respectively.

Table 1. Four-bus system impedance and line charging data.

From bus	To bus	Z, line impedance (p.u.)	B, line charging (p.u.)
1	2	$0{\cdot}01 + j0{\cdot}01$	$j2{\cdot}1125e-4$
2	3	$0{\cdot}02 + j0{\cdot}08$	$j8{\cdot}4500e-4$
3	4	$0{\cdot}01 + j0{\cdot}02$	$j4{\cdot}2250e-4$
1	4	$0{\cdot}01 + j0{\cdot}02$	$j4{\cdot}2250e-4$

Table 2. Four-bus system load data.

Bus no.	P_{load}(p.u.)	Q_{load}(p.u.)
1	0·00	0·00
2	0·10	0·10
3	0·10	0·10
4	0·80	0·40

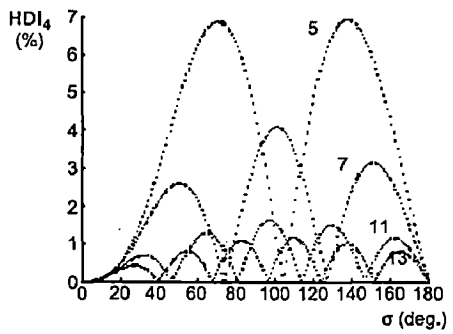


Figure5.3: Variations of Individual Harmonic Distortion as a Function of Conduction Angles.

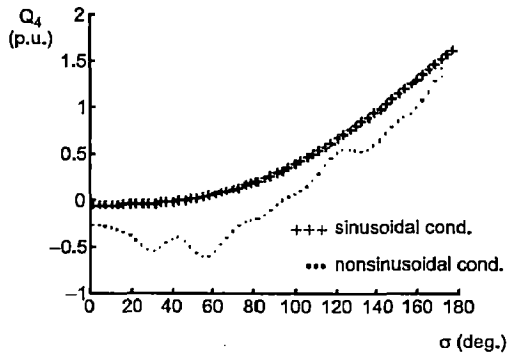


Figure 5.4: Variations of Reactive Power at bus-4 for all Conduction Angles.

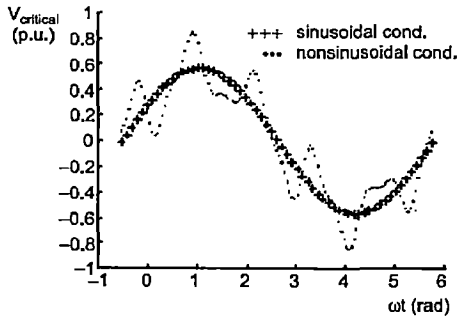


Figure 5.5: Variations of Critical Voltage at bus-4 for $\sigma = 70^0$.

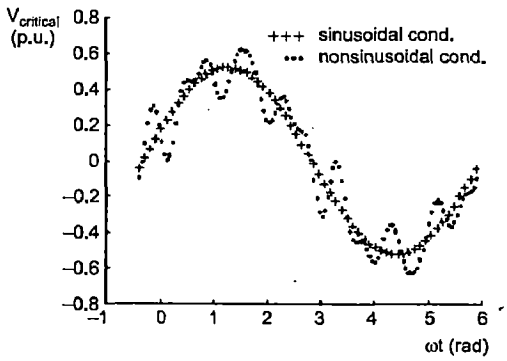


Figure5.6: Variation of Critical Voltage at bus-4 for $\sigma = 105^0$.

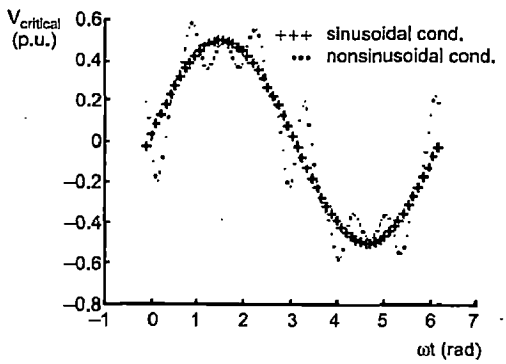


Figure 5.7: Variations of Critical Voltage at bus-4 for $\sigma = 160^0$.

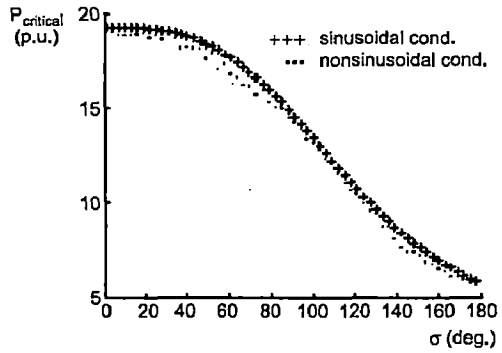


Figure 5.8: Critical Power Values Versus Conduction Angle at bus-4.

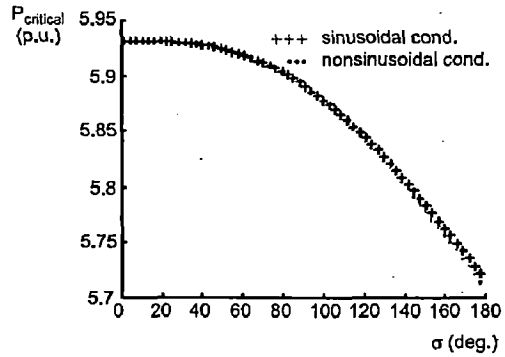


Figure 5.9: Critical Power Values Versus Conduction Angle at bus-3.

Steps to Complete Harmonic Power Flow Algorithm Analysis

Step 1: Make an initial guess for the fundamental and harmonic bus voltage magnitudes and phase angles ($V^{(1)} = 1{\cdot}0$ p.u., $\delta^{(1)} = 0$ radian, $V^{(h)} = 0{\cdot}1$ p.u. and $\delta^{(h)} = 0$).

Step 2: Compute the nonlinear device currents $g^{(h)}_{r,m}$ and $g^{(h)}_{i,m}$ for nonlinear loads.

Step 3: Evaluate [Δ**M**] (10)–(12); if it is a small enough stop.

Step 4: Evaluate ***J*** and calculate [Δ**X**], (13) using matrix inversion or forward/backward substitution.

Step 5: Update [**X**], (6), $[\mathbf{X}]^{l+1} = [\mathbf{X}]^{l} - [\Delta\mathbf{X}]$ (l is iteration number).

Step 6: Go to step 2.

RESULTS, CONCLUSION AND FUTURE WORK

Digital simulation of a 24-pulse,GTO converter and implementing an exact modeling of the STATCOM and SSSC by using a high pulse converter built a powerful base for in- depth investigation of the VSC- FACTS operation, both stand alone and within an interconnected grid. While the previous simulations have been performed by mathematical modeling or low pulse converters (6 or 12 pulse) that do not allow for an accurate simulation and investigation of the STATCOM and SSSC, this thesis provides the required modeling tools that open up new opportunities for design, control and operation of VSC- FACTS as well as power system studies. Section 3.A an extended application of such a detailed study of the STATCOM within a power system and how it leads to design a new supplementary controller for stability enhancement of the STATCOM. This presents another application of the SSSC modeling in order to study its dynamic performance and design an auxiliary regulator.

The thesis contributions can be summarized as:

1- Development of a 24-pulse, GTO converter model, with variation ac phase angle, as the basis building block of the VSC- FACTS as given in Section 3.1.1 in Chapter 3.

2- Development of the required models and exact digital simulation of the STATCOM and SSSC, using the 24-pulse converter, by Simulink /PSB software, within a power transmission system that allows for in-depth investigation of the STATCOM and SSSC operation.

3- Investigation of the STATCOM stability under various power system conditions and design a new supplementary controller to enhance the stability, presented in Section 3.A.

4- Investigation of the SSSC dynamic operation at load switching's and design an auxiliary regulator to enhance the dynamic performance of the SSSC, presented in Section 4.B.

The proposed study may be continued for further investigation of the effect of the STATCOM and SSSC on transient and steady state stability of power systems as well as operation under power system contingency such as short circuit, which may lead to design of new supplementary controllers and regulators to enhance the operation of both VSC-FACTS and the power transmission system.

In some practical application, transmission line voltage or current may be distorted or contain high levels of harmonics. Therefore some control system components of the STATCOM and SSSC, such as the PLL system, may operate inaccurately and it would result in poor operation of the compensating devices. With increasing number of nonlinear loads that generate harmonics, this may be quite usual in power transmission systems. Hence appropriate filtering of the transmission line voltage or current would be necessary. Study of such conditions and design appropriate filters to improve the STATCOM and SSSC operation may be another field to continue the proposed work.

I have investigated the effects of harmonics on voltage stability in power systems. The following conclusions are derived from the study.

(a) Reactive power compensation is very important in terms of voltage stability. Perfect compensation cannot be achieved when the effects of harmonics are not taken into consideration. The simulation results show that there are significant harmonic distortions within the compensator system. Hence, the conduction angle must be changed to obtain the desired reactive power in the system.

(b) The harmonic distortions in the system are low in properly designed static VAR compensator systems including TCR. This approach of designing for the minimization of harmonic effects helps us in the operation of the system and as a result provides steadystate operations of the system.

(c) The bus connected with nonlinear elements particularly needs to be studied in terms of stability. The analysis performed in this study indicates that the bus with nonlinear elements is the one most affected by the harmonics.

(d) When the system connected with static VAR compensator including FC-TCR is examined, it is noticed that some differences occur in critical values obtained from steady state stability analysis depending on the presence of the harmonic component. This case clearly shows that harmonic components have non-negligible importance in stability.

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