DESIGN AND DEVELOPMENT OF DUAL BAND RADIO FREQUENCY INTEGRATED CIRCUITS

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in RF and Microwave Engineering)

By

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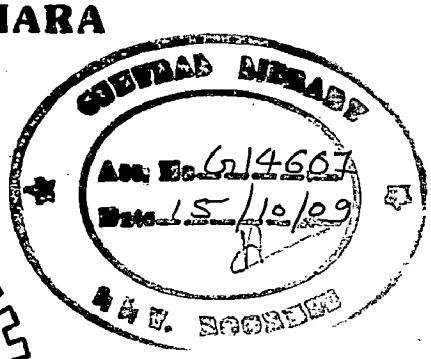

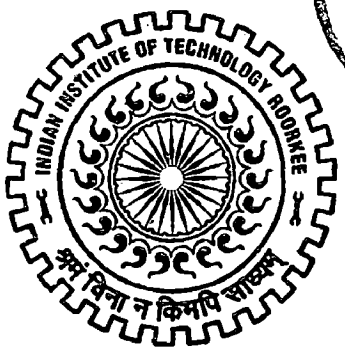

DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING
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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being presented in the dissertation entitled **"DESIGN AND DEVELOPMENT OF DUAL BAND RADIO FREQUENCY INTEGRATED CIRCUITS"** towards the partial fulfillment of the requirement for the award of the degree of **Master of Technology** in **RF and Microwave Engineering**, submitted in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work carried out under the guidance of **Dr. N.P.Pathak, Assistant Professor, Department of Electronics and Computer Engineering, IIT Roorkee**.

I have not submitted the matter embodied in this dissertation report for the award of any other degree.

Dated: 30/06/09
Place: IIT Roorkee.

(Harika Sreedhara)

CERTIFICATE

This is to certify that above statement made by the candidate is correct to the best of my knowledge and belief.

Dated: 30/06/09
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(Harika Sreedhara)

ABSTRACT

The increasing role of communication has led to a remarkable proliferation of the communication standards. Therefore, the need for systems compatible with different communication platforms has become a necessity to replace archaic systems conforming to a single communication standard. Coupled with the demand to make communication systems compact, the development of multiband circuits has revolutionized the field of communication. The development of multiband circuits in RFICs has made it possible to reduce the cost of the systems while increasing their utility making them concise.

The main objective of this dissertation is to design and develop dual band RFICs integral to a communication system. The backbone of a communication system is the seamless interaction between the linear and non-linear components within the module. To this end, this work emphasizes equally on both the linear and non-linear component designs used to implement a dual band communication system.

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CHAPTER 1

Review of Literature and Problem statement

Multiband and multi-standard architectures have revolutionized the field of communication since their arrival in the field. They became all the more important as communication technologies advanced in leaps and bounds over the years and wireless technology made its presence felt in a huge way. The advent of the wireless systems as well as their evolution over the years has acted as a catalyst to develop and then enhance multiband networks. Therefore Radio Frequency Integrated Circuits (RFICs), form a major part of the wireless communication systems [1, 2] all the more now when an increasing number of capabilities are being implemented in continuously shrinking integrated circuits. An integrated circuit containing analog circuitry operating at frequencies in and above ultrahigh frequency band is defined as a Radio Frequency Integrated Circuit (RFIC). The ICs maybe in congruence with the following technologies [3]:

a. ***Monolithic Microwave Integrated Circuits (MMICs)***: The entire IC is built on a single crystal.

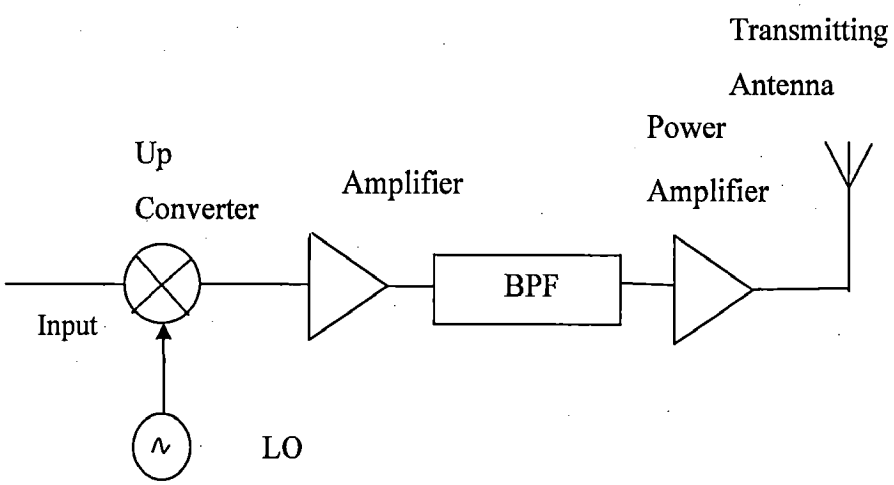
b. ***Hybrid Integrated Circuits (Hybrid ICs)***: It is a combination of two or more integrated types or one IC type together with discrete elements.

c. ***Multi-Chip Module (MCMs))***: A Multi-Chip Module (MCM) is a specialized electronic package where multiple integrated circuits (ICs), semiconductor dies or other modules are packaged in such a way as to facilitate their use as a single IC.

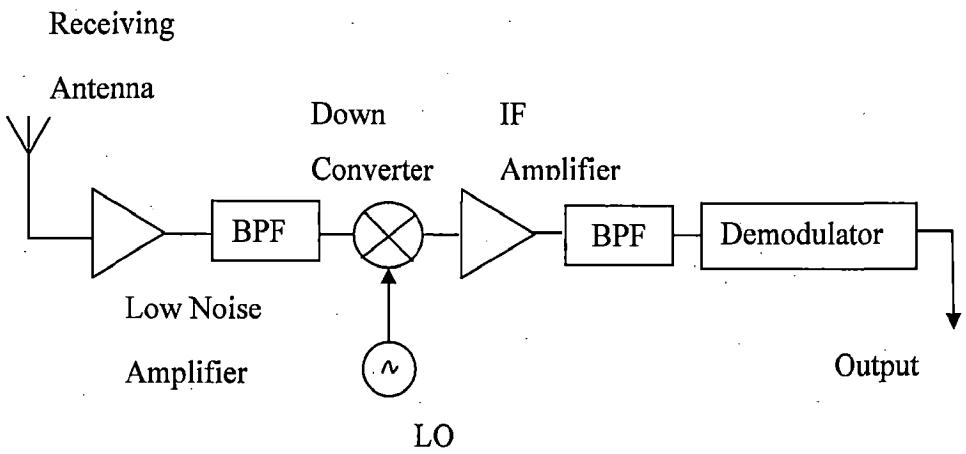
What began with multiple parallel architectures has now evolved into a communication system with wideband, concurrent capabilities. But, to begin to understand this rapid development one has to start at the roots i.e. a literature review is followed by parallel architecture design before moving on to the more challenging designs. To this end, this report has been organized in the exact same manner as will be explained in the subsequent sections.

1.1 Block Diagram of RF Transmitter & Receiver

Consider the basic block diagrams of a typical transmitter and receiver in fig.1.1



(a)



(b)

Fig.1.1: Block diagram of (a) Transmitter (b) Receiver

Thus, the basic building blocks of transmitters and receivers are filters, Low Noise Amplifiers (LNA), Mixers, Oscillators for multimode generation and some modules may include passive circuits like couplers, circulators etc. for feeding and transferring power. In dual band RFICs each these individual blocks maybe implemented to given a dual

band performance or it is also possible to have a part of the circuit performing dual band operation and the remaining components may be optimized to work on an individual frequency thereby achieving a balance between space constraints and optimization. Usually, the linear components like amplifiers are designed for multiband operation whereas the non-linear components like mixers are preferably designed for a single frequency operation if it can be afforded as designing a non-linear circuit to operate at multiple frequencies can be quite complex and challenging.

1.1.1 Brief description of RFIC front end components

1. **Filters:** They are passive components that are made up of inductors and capacitors that inherently have a narrowband operation. The challenge is to change the network in such a way so that the filter operation is obtained at multiple frequencies. They are responsible for frequency selection at the first stage of the input. The corner frequencies are usually varied by capacitance tuning for multiband operation [3].

   Passive Components [10] are responsible for feeding power to the active components or dividing power frequency selection and matching purposes. They can be responsible for transferring or splitting power between different sections of the entire module. Hence, their importance cannot be undermined in anyway [6, 9, 21].

   The above components are the building blocks of any typical RFIC and since it is not possible to understand the scope and design of every component in the time allotted, a selection has been made from the active and passive domains: Power divider from the passive and a mixer from the active.

2. **LNA:** The low noise amplifier is an integral component as the RF signal is amplified at this stage preceding the mixer. Many concurrent and switched networks have been developed for obtain multiband LNA performance [3, 7]. The switched networks usually rely on a switched inductive or capacitive networks often modified by the incoming RF signal [5, 16, 19, 20].

3. **Mixers:** Responsible for downconverting the RF signal to baseband can be implemented using FETs in configurations like Dual Gate FET, Gilbert cell etc.. For dual band operation, the Gilbert cell is preferred and designs have achieved excellent performance using this as a mixer configuration [3, 5, 25].

4. **Oscillators:** Since the frequency synthesizer for a multi standard and multi band receiver ahs to provide all the requisite LO frequencies with no overlapping, its design is subject to the most stringent criteria. In fully integrated synthesizers, the VCO includes a switched capacitor for coarse tuning and a varactor for fine tuning purposes [3]. A set of parallel VCOs can also be used for same purpose notwithstanding the concerns about the area they will occupy. A multiband VCO can also be implemented using a frequency divider to generate the actual LO frequency when the VCO oscillates at a multiple of the desired frequency. A fractional LO w.r.t. the VCO frequency can be generated using an SSB mixer or plain mixer with image SB filtering [3, 5, 13].

1.2 Literature Review

A literature review is the first step to any design. A comprehensive literature review reveals different possible ways in which dual band operation can be achieved in a circuit. Dual band operation has been achieved in passive as well as active devices. In active devices, dual band performance has been achieved in linear as well as the non-linear mode of operation [3-4], [8, 11, 13, 24]. Entire receiver and even transceiver chips have been designed to operate in dual band. The following types of architectures have been used to design dual band circuits:

1. **Parallel Architecture** In this conventional approach, the receiver has different paths for each individual frequency. Therefore, each frequency band has its own matching circuit and transistor for an LNA, mixer etc. This kind of architecture occupies a lot of die area since it is equivalent to combining the components of different receivers on a single chip [3, 5]. This architecture has the advantage of low interference and each stage can be optimized separately. However, owing to the large die area it occupies, the layout and PCB designing becomes difficult.

   Switched Network Architecture A variation to the parallel architecture can be having a switched network which chooses the path corresponding to the incoming RF frequency. The switch at the input of the circuit performs selection between the parallel paths for the incoming frequencies. Also, switched inductor networks have been used in practice which do away with the parallel paths but use the transistor model to change the equivalent value of the lumped components in the matching

network such that, the same matching network can serve for both the incoming frequencies. For example, a FET maybe a part of the matching network so that the transistor gets switched on for only one of the incoming frequencies. The capacitance of the FET model i.e. C_{ds} and C_{gs} can change the equivalent capacitance in the matching network. However, this method is effective for the operation of dual band networks but not for tri band etc [4, 7].

2. **Concurrent Architecture** In this architecture, the same receiver architecture is designed in a way to receive more than one frequency simultaneously. This architecture can result in a very compact die area. For example, a concurrent LNA can simultaneously amplify two or more incoming bands. However, the design of such architecture is extremely challenging and an optimum gain cannot be achieved for all the bands. In other words, a compromise has to be made in the amount of gain achieved [16, 17, 21].

3. **Wideband Architecture** This is strictly not dual band architecture. In this architecture, the matching networks are designed to function over an entire frequency range. The matching network is first designed at the centre frequency and then optimized to operate over the entire frequency range. The challenge is to optimize the wideband network in such a way that acceptable if not optimum performance can be achieved over the entire range of frequencies [3].

Each of the architectures has its own advantages and disadvantages. However, concurrent and wideband architectures have been used extremely efficiently in circuits where the space constraints are at a maximum. However, some tradeoff in terms of the gain has to be made as it is virtually impossible to obtain optimal performance at both the frequencies. The design aim to achieve acceptable performance at both the desired frequencies of operation. This has been achieved in passive networks like couplers, power dividers etc.. As for the circuits using active devices tremendous success has been achieved in designing LNA especially in all the different kinds of architectures. Mixers and other non-linear devices on the other hand, are difficult to design with dual band characteristics and often implemented with parallel paths even in dual band transceiver modules.

1.3 Problem Statement

The main objectives of the dissertation are:

I. **To design and develop a microstrip based dual passive combining/splitting network simultaneously working at 2.4 GHz and 5.25 GHz.**

II. **Design and Development of active integrated circuit mixer for use at 2.4 GHz and 5.25 GHz and broadband**

1.4 Organization of the dissertation

Chapter 1 of this dissertation describes the review of literature along with statement of the problem.

Chapter 2 of this dissertation describes the details of design and development ofpower combining/dividing microwave networks in microstrip for dual band operation.

Chapter 3 describes the basic theory and characteristics of a mixer.

Chapter 4 describes the design and implementation of active mixers and finally,

Chapter 5 discusses the conclusion and future scope of the work reported in this dissertation.

CHAPTER 2

Passive Radio Frequency Integrated Circuits

2.1 Introduction

Passive RFIC networks are mainly comprised by couplers, filters, circulators etc. They can be 2 port, 3 port or even 4 port networks [22]. In this dissertation, 3 port passive networks are focused upon as the objective was to design a mixer. A 3 port passive network can be used to feed RF and LO power to a mixer. Therefore, the design and development of dual band Wilkinson Power Divider is presented in this chapter.

2.2 Conventional Wilkinson power divider

The Wilkinson power divider is a lossy three-port network that has all the ports matched and has isolation between its output ports. It has the useful property of being lossless when the output ports are matched i.e. only reflected power is dissipated. The Wilkinson power divider can be made to give arbitrary power division but here, only the equal-split (3dB) case is being considered. A conventional Wilkinson power divider is as shown below [22]:

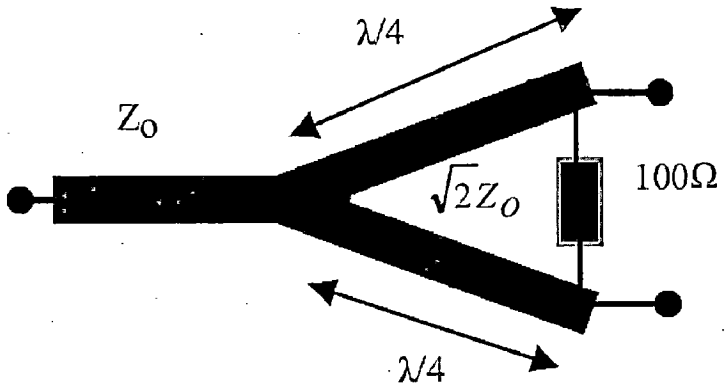


Fig.2.1: A conventional Wilkinson power divider

As can be seen from fig.2.1, the Wilkinson power divider consists of two-quarter wave impedance transformers whose characteristic impedance is $\sqrt{2}\ Z_o$, where Z_o is the characteristic impedance of the three ports. A resistor of value $2Z_o$ has been placed between the two output ports to improve the isolation between the two output ports. The

values of the resistor and the characteristic impedance of the impedance transformers have been obtained mathematically in [22] using an even and odd mode analysis. This divider is often implemented in micro strip or strip line.

2.3 Design of the π-section Dual Band Wilkinson Power Divider

This power divider consists of replacing each (λ/4) transmission line in the conventional Wilkinson power divider with a corresponding π-section. This π-section has been designed such that the power divider operates at two arbitrary frequencies. The objective is to obtain the characteristic impedances of each transmission line section of the equivalent π-section as a function of their electrical lengths at one of the desired operation frequencies [9-10], [12, 23].

2.3.1 Analysis of the equivalent π – section

The equivalent π-section [12] consists of two identical open stubs connected by a series transmission line as shown in fig.2.2 [12].

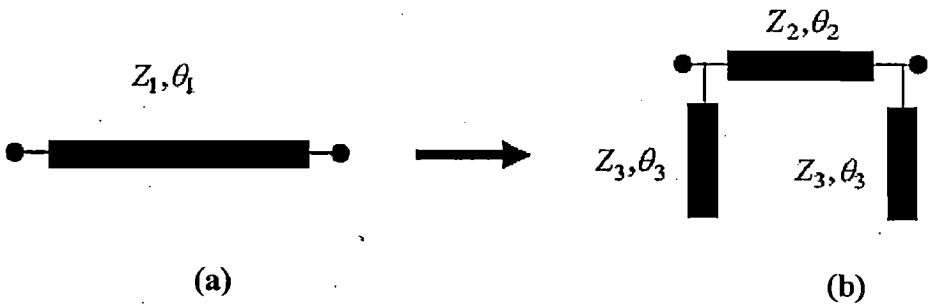


Fig.2.2: (a) Transmission line (b) Equivalent π-section

The equivalence between the two sections can be seen by using the ABCD matrices of both the sections. The analysis is as explained below:

The ABCD matrix of fig. 2.2 (a) with (λ/4) length transmission line is:

$$M_1 = \begin{bmatrix} 0 & jZ_1 \\ jY_1 & 0 \end{bmatrix} \tag{2.1}$$

Where $Z_1 = \sqrt{2}\, Z_o$ as in the conventional Wilkinson power divider.

The ABCD matrix of the π-section of fig. 2.2 (b) is:

$$M_2 = \begin{bmatrix} \cos\theta_2 & jZ_2 \sin\theta_2 \\ jY_2 \sin\theta_2 & \cos\theta_2 \end{bmatrix} \quad (2.2)$$

$$M_3 = \begin{bmatrix} 1 & 0 \\ jY_3 \tan\theta_3 & 1 \end{bmatrix} \quad (2.3)$$

Where,

M_2 is the ABCD matrix of the series transmission line of fig. 2.2(b) and M_3 is the ABCD matrix of the shunt stubs of fig, 2.2 (b).

θ_2 and θ_3 are the electrical lengths of the transmission lines with characteristic impedances Z_2 and Z_3 as shown in fig. 2.2 (b) respectively.

The equivalent ABCD matrix of the π-section is then given by:

$$M_T = M_3 M_2 M_3 \quad (2.4)$$

Equating element A from matrices,

$$\cos\theta_2 - Y_3 Z_2 \sin\theta_2 \tan\theta_3 = 0$$

This gives,

$$\tan\theta_3 = \left(\frac{Z_3}{Z_2}\right)\cot\theta_2 \quad (2.5)$$

Equating element B from matrices,

$$jZ_2 \sin\theta_2 = jZ_1$$

$$Z_1 = Z_2 \sin\theta_2 \quad (2.6)$$

For dual band operation (2.6) must be modified as:

$$Z_2 \sin\theta_{2f1} = \pm Z_1 \quad (2.7a)$$

$$Z_2 \sin\theta_{2f2} = \pm Z_1 \quad (2.7b)$$

where f_1 and f_2 are the two operating frequencies and θ_{2f1}, θ_{2f2} are the electrical lengths of the transmission line of characteristic impedance Z_2 at frequencies f_1 and f_2 ($f_2 > f_1$) respectively.

From (2.7a) and (2.7b),

$$\theta_{2f1} = n\pi - \theta_{2f1}, n = 1,2,3,.... \tag{2.8}$$

Since a compact size is always preferred, n = 1 is chosen so that the relation between the electrical lengths and dual operation frequencies f_1 and f_2 is obtained as:

$$\frac{\theta_{2f2}}{\theta_{2f1}} = \frac{f_2}{f_1} = R \tag{2.9}$$

Using (2.8) in (2.9), we get the above equation in a modified form,

$$\theta_{2f1} = \frac{n\pi}{R+1} \tag{2.10}$$

$$\theta_{2f2} = \frac{Rn\pi}{R+1} \tag{2.11}$$

Similarly,

$$\theta_{3f1} = \frac{m\pi}{R+1} \tag{2.12}$$

$$\theta_{3f2} = \frac{Rm\pi}{R+1} \tag{2.13}$$

For compact design m=1 is chosen.

The above analysis is sufficient to design the dual band Wilkinson power divider as will be explained in the next section.

2.3.2 Design of Dual Band WPD

The following steps are followed to design the dual band Wilkinson power divider:

i. Select the two frequencies for which the operation is desired.

ii. Find the value of R using (2.9).

iii. Calculate the values of $\theta_{2f1} and \theta_{3f1}$ using (2.10) and (2.12) or calculate the values of $\theta_{2f2} and \theta_{3f2}$ using (2.11) and (2.13) with m = n = 1.

iv. If (2.10) and (2.12) have been used, calculate the values of impedances Z_2 and Z_3 as shown below:

$$Z_2 = \frac{Z_1}{\sin \theta_{2f1}} \tag{2.14}$$

$$Z_3 = Z_2 \tan \theta_{2f1} \tan \theta_{3f1} \tag{2.15}$$

v. If (2.11) and (2.12) have been used, follow a similar procedure and replace θ_{2f1} and θ_{3f1} by θ_{2f2} and θ_{3f2}.

2.3.3 Numerical Analysis and Momentum Simulation

Design software used: ADS (Advanced Design System) (Momentum)

Implementation and practical realization using: Microstrip

Operation frequencies selected: $f_1 = 1.8$ GHz and $f_2 = 4.775$ GHz

Substrate parameters: $\varepsilon_r = 3.38$, substrate thickness, h = 1.542 mm, tan $\delta = 0.0025$, conductor thickness = (1/4) Oz. Cu

i. From (2.9) , $R = (f_2 / f_1) = (4.775 / 1.8) = 2.6527$

ii. Using (2.11) and (2.13) with m = n = 1 and the value of R from (2.9) ,

$$\theta_{2f1} = \theta_{3f1} = \frac{\pi}{R+1} = 0.860 \text{ Radians}$$

iii. From (2.14) and (2.15) ,

$$Z_2 = \frac{Z_1}{\sin \theta_{2f1}} = \frac{Z_1}{\sin 0.860}$$

Here, $Z_o = 50\ \Omega$

Therefore, $Z_1 = \sqrt{2}\, Z_o = \sqrt{2} * 50 = 70.711\ \Omega$

$Z_2 = 93.31\ \Omega$

and $Z_3 = Z_2 \tan(\theta_{2\,f1}) \tan(\theta_{3\,f1}) = 93.31 * \tan^2(0.860) = 125.89\ \Omega$

iv. Calculate the dimensions of the microstrip lines to implement the power divider

Table 2.1: Dimensions of the π-section dual band Wilkinson Power divider

Dimensions(mm)	Characteristic Impedance of Input & Output Port Lines	Characteristic Impedances of the π-section	
	$Z_0 = 50\ \Omega$	Z_2= 93.31Ω	Z_3= 125.89Ω
Width, W	3.513340	1.054230	0.457713
Length, L	5 (arbitrary)	14.496800	14.751200

v. Once the dimensions are known the power divider is designed using microstrip.

vi. **The layout** was then drawn and simulated from 0.1 GHz to 6 GHz.

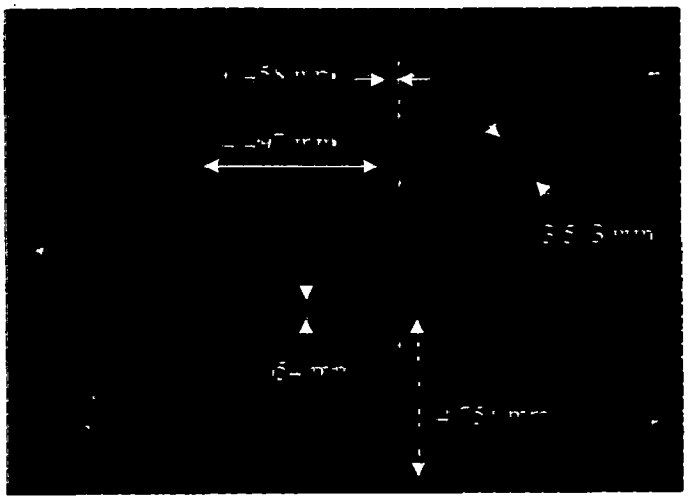


Fig.2.3: Layout of the π-section WPD (layout not to scale)

vii. The momentum simulation results are shown in fig.2.4.

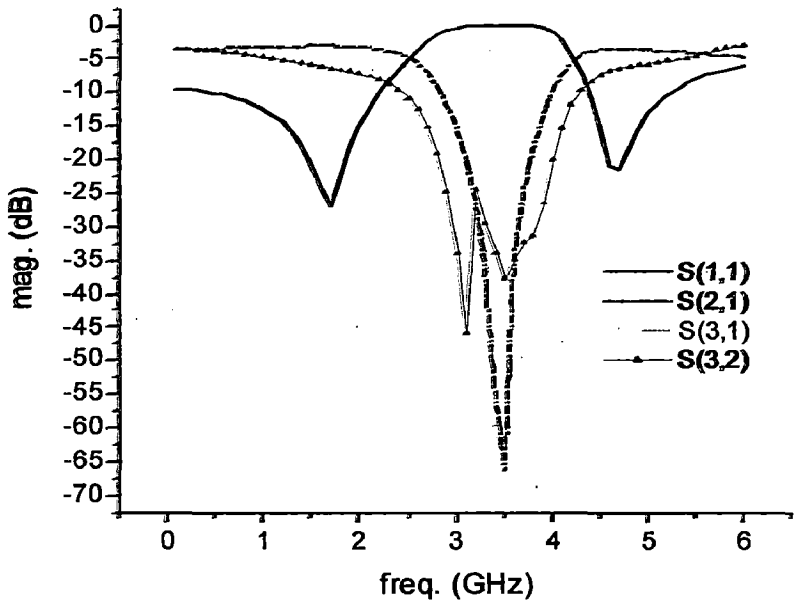


Fig.2.4: S_{11}, S_{21}, S_{31}, S_{32} obtained by simulating the power divider using momentum

viii. **The fabricated** π-section WPD is as shown in fig.2.5.

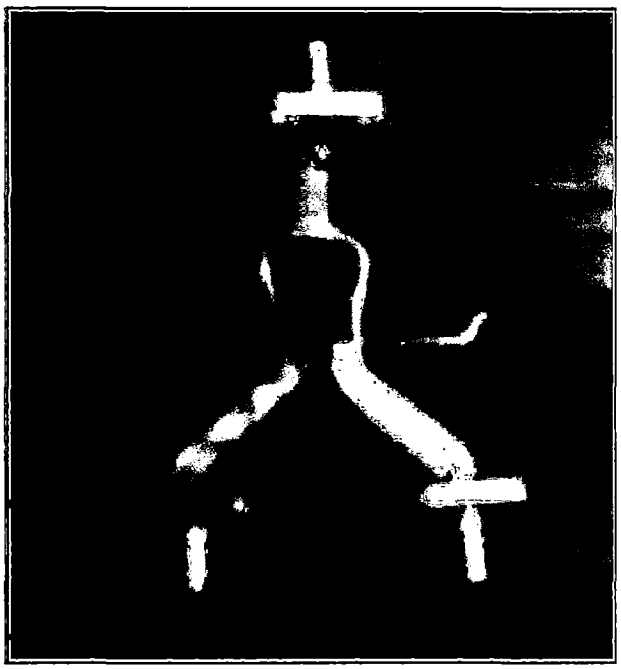
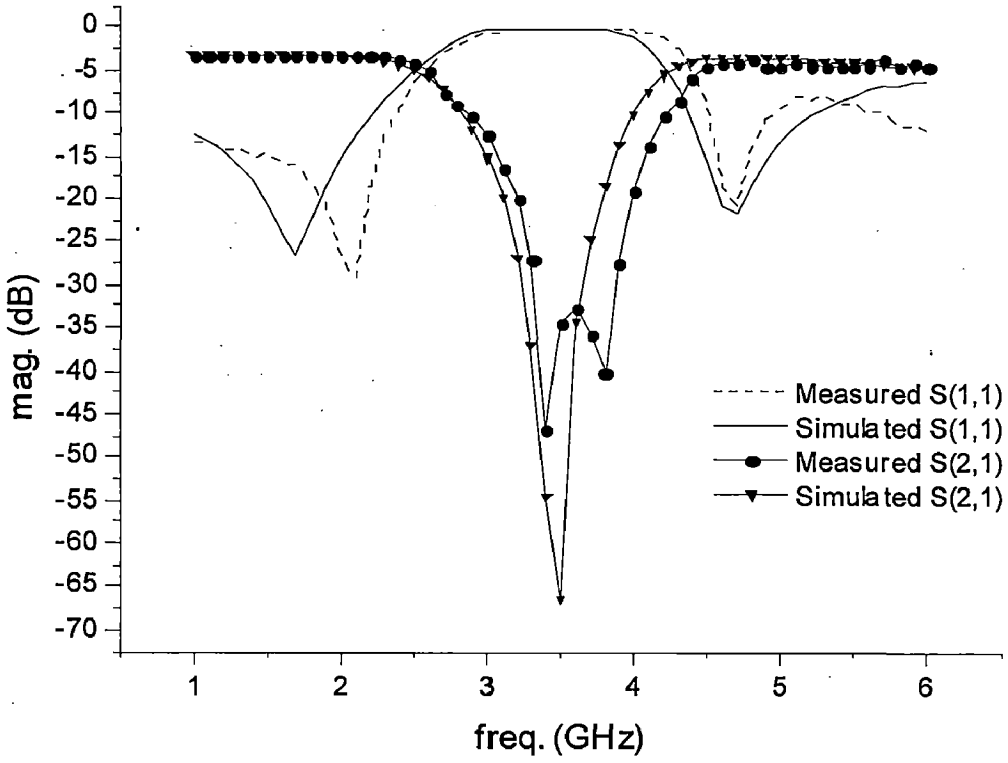
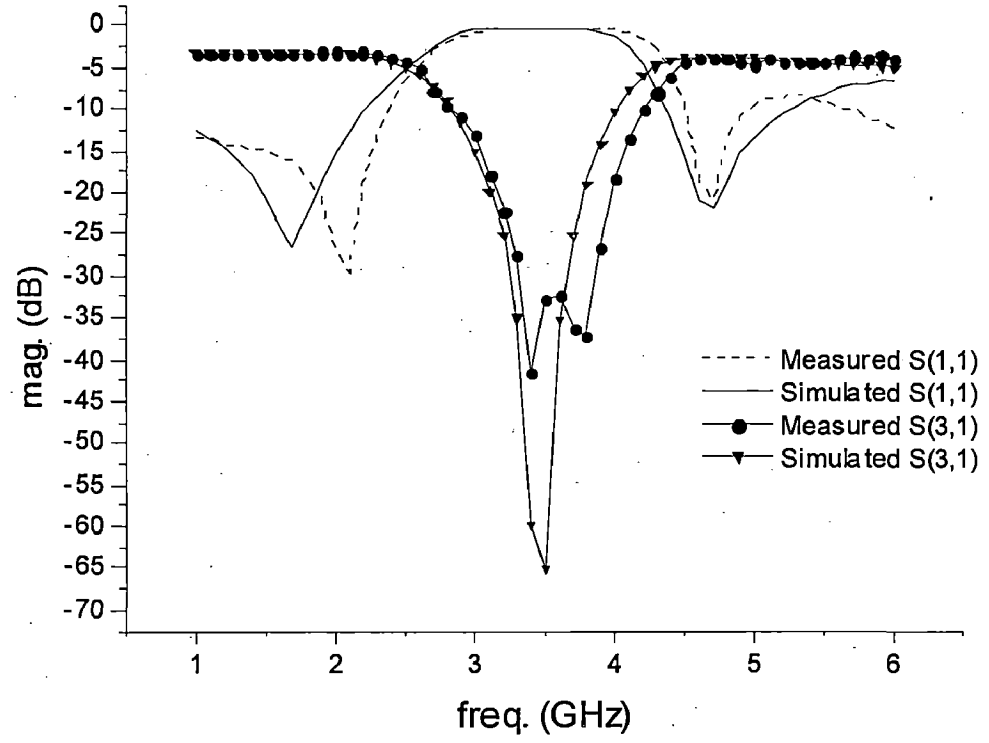


Fig.2.5: Fabricated π-section WPD

ix. The fabricated WPD was tested on the VNA and the results obtained are shown in fig.2.6.


0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
-55
-60
-65
-70
mag. (dB)
1
2
3
4
5
6
freq. (GHz)
Measured S(1,1)
Simulated S(1,1)
Measured S(2,1)
Simulated S(2,1)

(a)


0
-5
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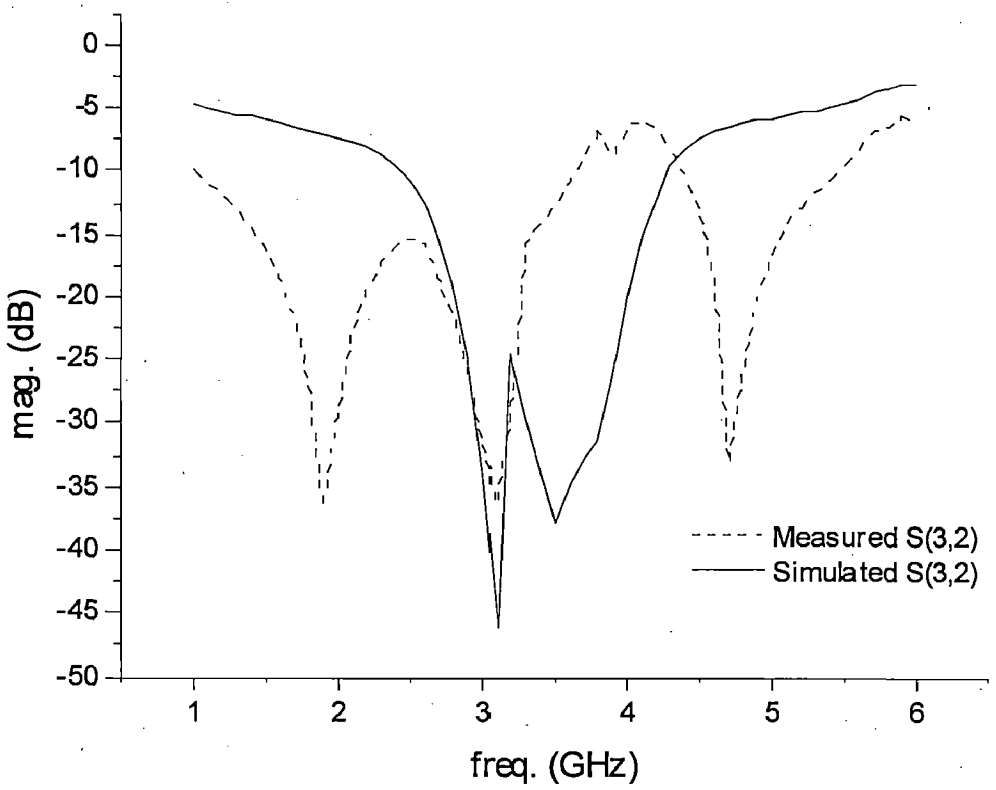
-40
-45
-50
-55
-60
-65
-70
mag. (dB)
1
2
3
4
5
6
freq. (GHz)
Measured S(1,1)
Simulated S(1,1)
Measured S(3,1)
Simulated S(3,1)

(b)



(c)

Fig.2.6: Comparison of measured and simulated (a) S_{11}, S_{21} (b) S_{11}, S_{31} (c) S_{32}

The results differ to some extent in the actual fabrication circuit. The losses may be attributed to fabrication errors. The return loss at the input port i.e. port 1 is -18 dB at 1.8 GHz and -13 dB at 4.775 GHz. The results still exhibit the dual band behavior of the circuit at the design frequencies i.e. -3.2 dB power split at 1.8 GHz and -3.5 dB at 4.775 GHz. Isolation between the two output ports is less than -25 dB at both the frequencies. Thus, the π-section WPD has been designed and implemented successfully and the desied results are obtained.

2.4 Dual Band WPD using cascaded section and a short/open stub

The π-section WPD described in the previous section is one of the ways a dual band operation is obtained from a WPD. No dual band design method is valid for every frequency ratio of the two desired frequencies of operation i.e. it is bound within a restricted frequency ratio range only within which the design equations and methodology hold. For example, the π-section dual band WPD is not suitable for fabrication if the frequency ratio is about 2.5. Therefore, another dual band WPD design shown in fig.2.7

[24] is provided here so that between these designs a considerable frequency ratio range is covered.

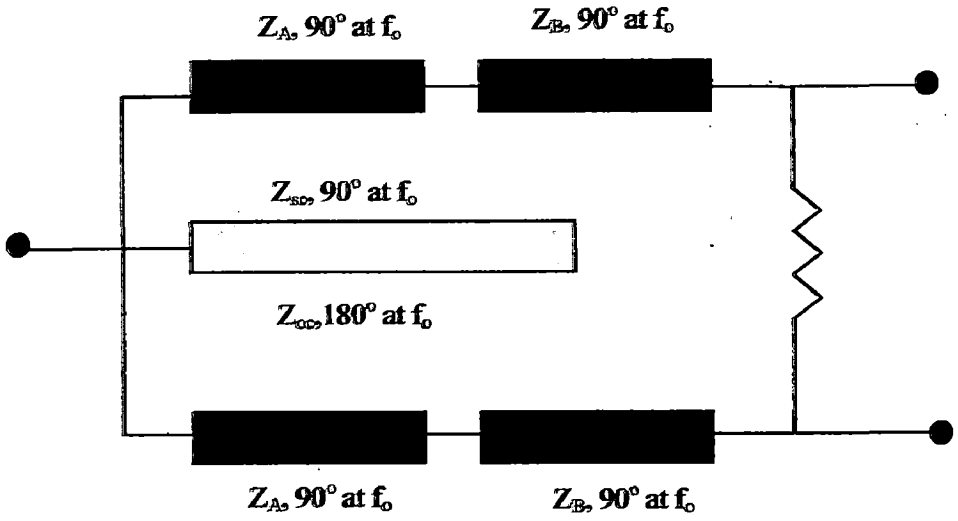


Fig.2.7: Proposed dual band divider circuit

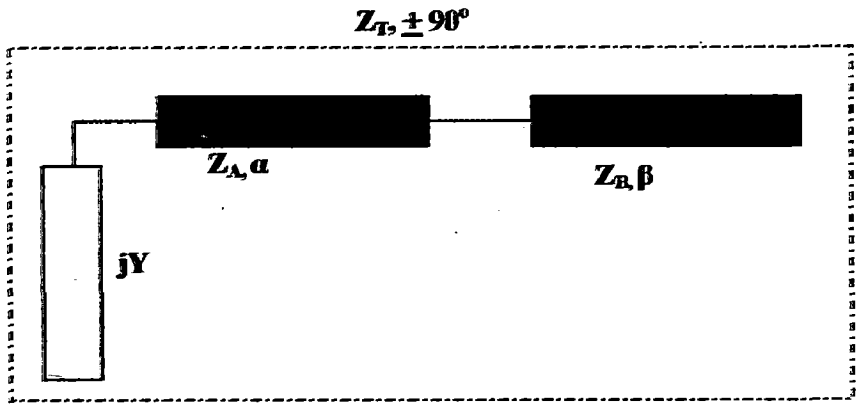


Fig.2.8: Transformer for dual band operation

The equations for this equivalent can be obtained by equating the ABCD matrices of the transformers i.e. the 90° electrical length transformer in a conventional WPD and the equivalent substituted in its place shown in fig.2.10. The entire equivalent ABCD matrix would be the product of the ABCD matrices of the individual elements. Thus, it would be the product of the ABCD matrices of the shunt element (Y) and the two series lines each of characteristic impedance 'Z_A' and 'Z_B' **and electrical lengths 'α' and 'β'** respectively. The mathematical analysis is carried out to find out the values of 'Z_A', 'Z_B', 'α', 'β' and 'Y'. The final design equations are listed here for convenience [24]:

$$Z_A = \sqrt{2} Z_o \tan\frac{\pi}{2}\varepsilon \tag{2.16}$$

$$Z_B = \sqrt{2} Z_0 \cot\frac{\pi}{2}\varepsilon \tag{2.17}$$

$$Z_{sc} = \frac{Z_o}{2}\frac{\tan\pi\varepsilon}{\sqrt{2}}\tan^2\frac{\pi}{2}\varepsilon \tag{2.18}$$

$$Z_{oc} = \frac{Z_o}{2}\tan^2\frac{\pi\varepsilon}{\sqrt{2}}\tan\frac{\pi}{2}\varepsilon \tag{2.19}$$

$$\text{Here, } \varepsilon = \frac{\frac{f_2}{f_1} - 1}{\frac{f_2}{f_1} + 1} \tag{2.20}$$

Where,

f_2 and f_1 are the upper and lower frequencies of operation respectively.

Z_o is the characteristic impedance of 50 Ω

Z_A and Z_B are the characteristic impedances of the sections of the two section branch line

α and β are the electrical lengths of the transmission lines of impedances Z_A and Z_B resp.

Z_{oc} and Z_{sc} are the characteristic impedances of the shunt elements.

2.4.1 Design and Analysis

This power divider is designed as per the following:

Operation frequencies selected: WLAN frequencies: f_1 = 2.4 GHz and f_2 = 5.25 GHz

Substrate parameters: ε_r = 2.2, substrate thickness, h = 0.254 mm,

conductor thickness = 18 μm.

The dual WPD designed here is designed with an open stub in order to prevent any holes to the ground in the substrate. Therefore, the calculated impedances and their dimensions in microstrip are calculated using (2.16), (2.17), (2.19), (2.20) and listed in table 2.2.

$f_1 = 2.4$ GHz

$f_2 = 5.25$ GHz

$\varepsilon = 0.3725$

Knowing these values table 2.2 can now be fully constructed.

Table 2.2: Transmission line values for dual band WPD with cascaded section and open stub

Transmission Line	Electrical Length (Degrees)	Characteristic Impedance (Ohms)	Width, W (mm)	Length, L (mm)
Z_o	0	50	0.784	5
Z_A	122.987	45.8183	0.866835	14.2174
Z_B	122.966	109.135	0.162866	14.9167
Z_{oc}	245.963	57.127	0.615046	28.7532

The simulation is now setup into the by drawing the layout and simulating it within the operational frequency range. The layout is shown below in fig.2.9. It occupies an entire area of 614 mm^2.

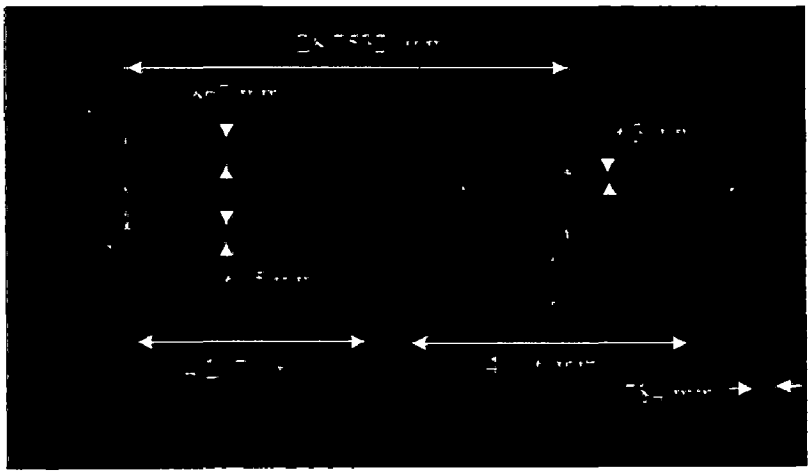


Fig.2.9: Layout of the cascaded section and open stub WPD (not to scale)

The simulation results are shown in fig.2.10.

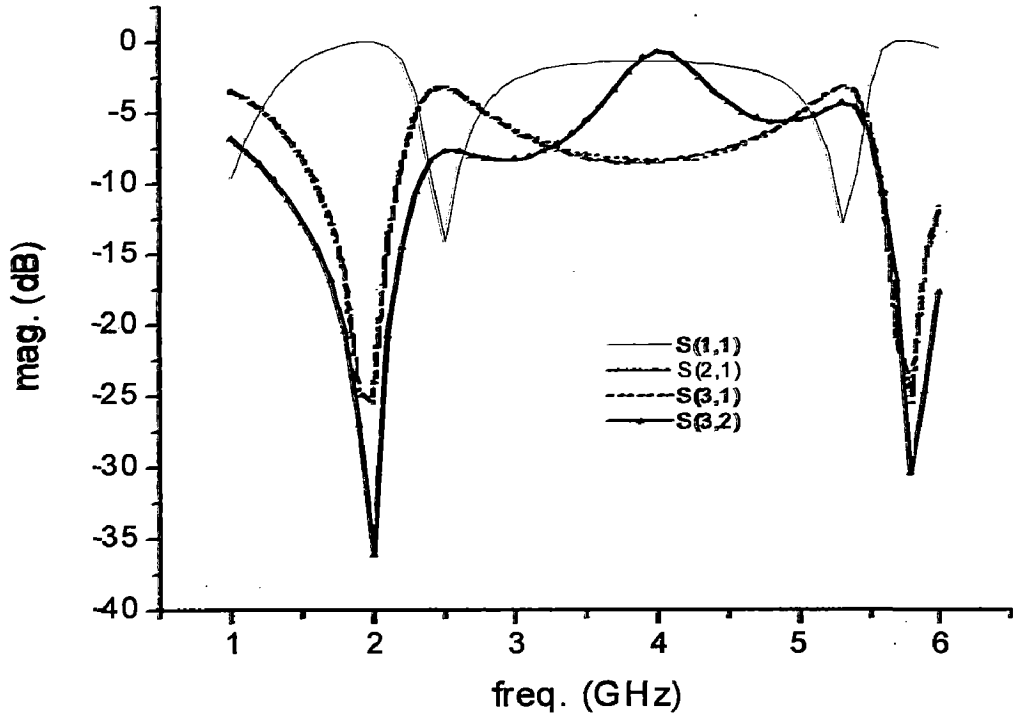


Fig.2.10: $S_{11}, S_{21}, S_{31}, S_{32}$ of the cascaded section and open stub WPD simulated in momentum

The fabricated circuit in microstrip is shown below in fig.2.11. The circuit was tested using a VNA and the required S-parameters at the operating frequencies have been measured. The measurement results have been shown in fig.2.12.

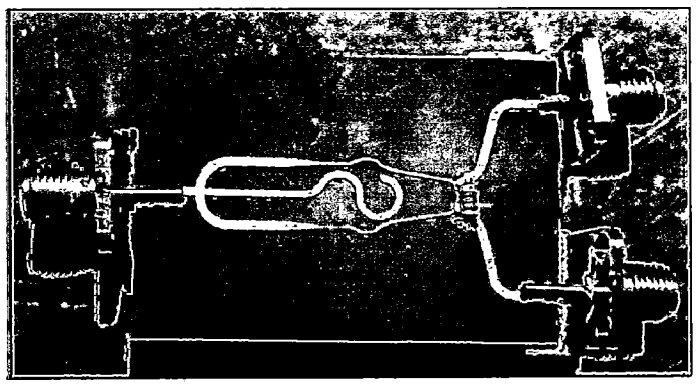
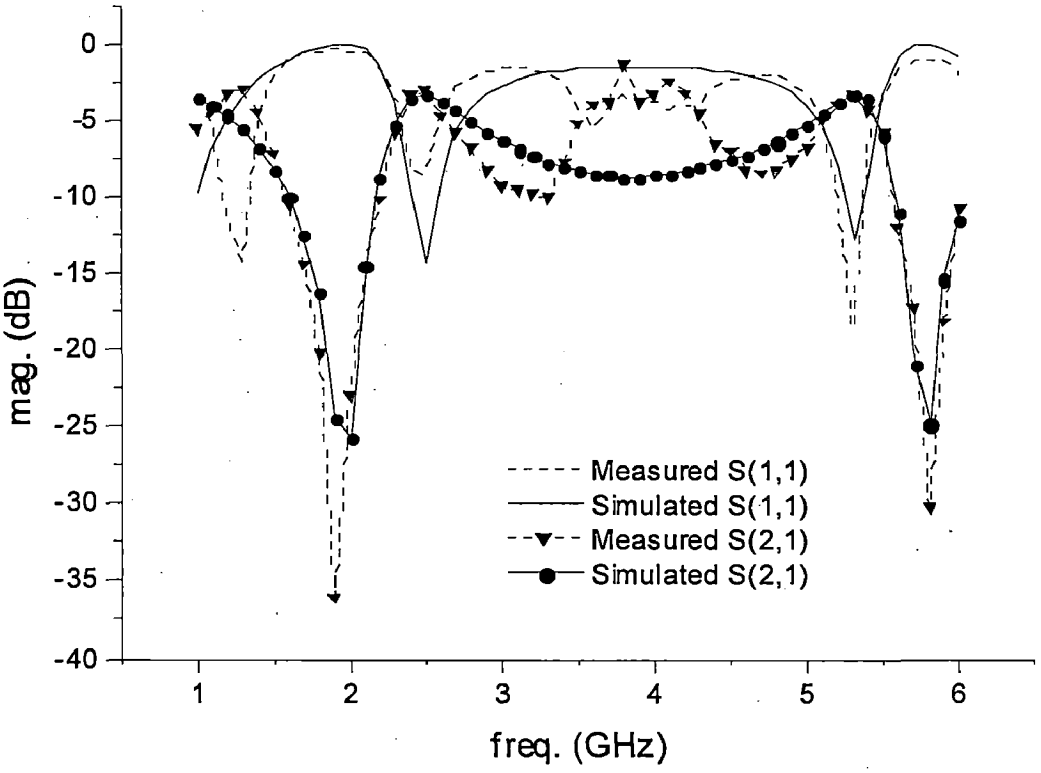
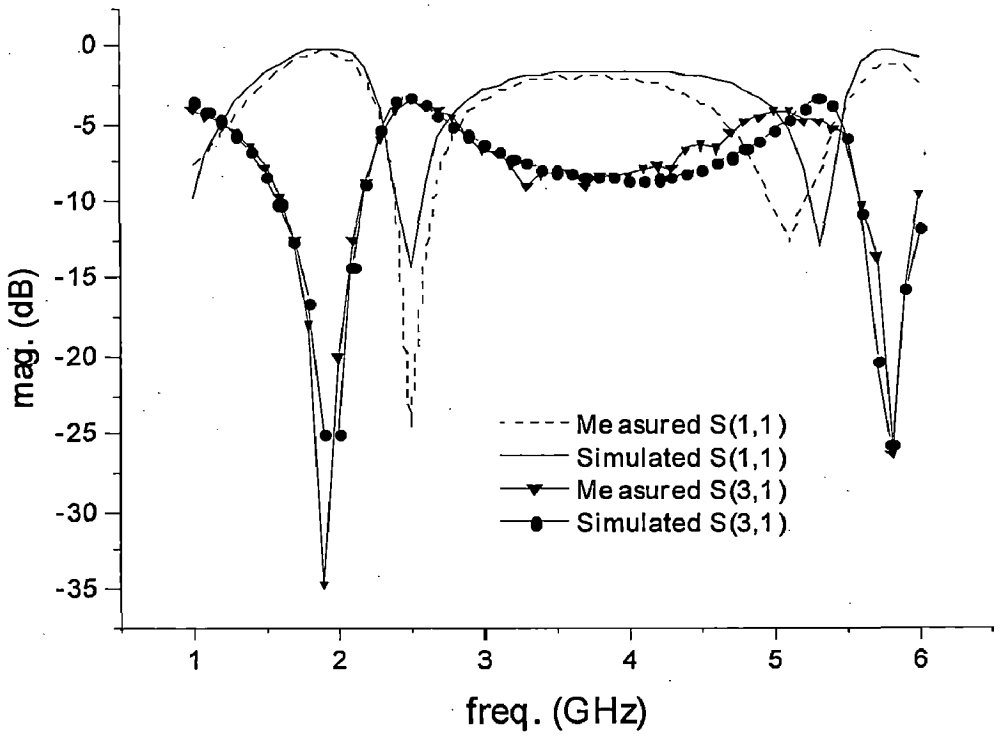


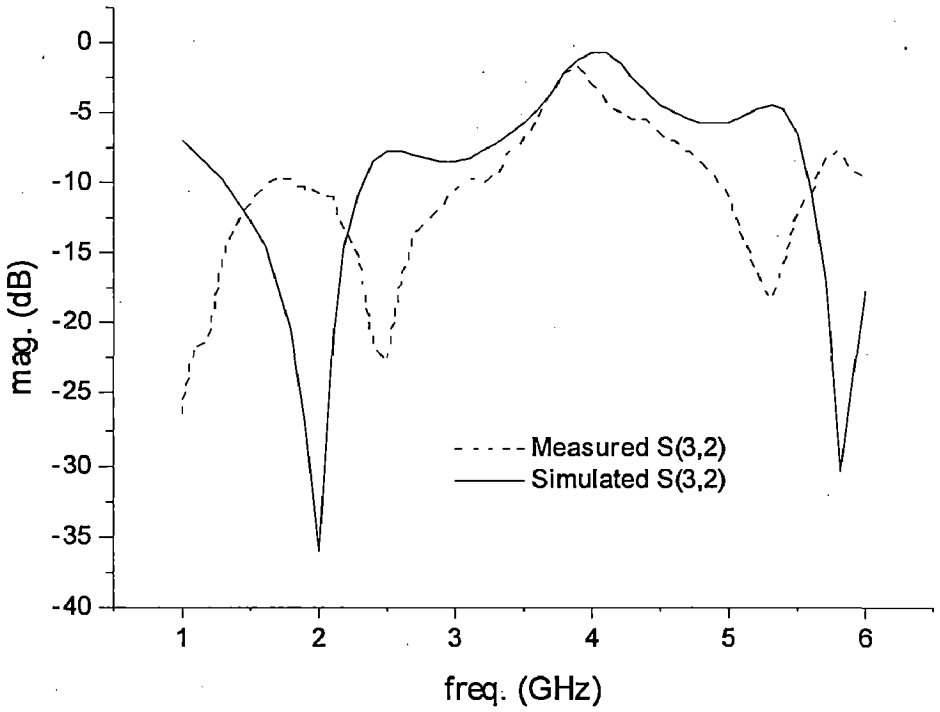
Fig.2.11: Fabricated Dual Band WPD using cascaded section and an open stub


0
-5
-10
-15
-20
-25
-30
-35
-40
mag. (dB)
1
2
3
4
5
6
freq. (GHz)
Measured S(1,1)
Simulated S(1,1)
Measured S(2,1)
Simulated S(2,1)

(a)


0
-5
-10
-15
-20
-25
-30
-35
mag. (dB)
1
2
3
4
5
6
freq. (GHz)
Measured S(1,1)
Simulated S(1,1)
Measured S(3,1)
Simulated S(3,1)

(b)



(c)

Fig.2.12: Comparison of measured and simulated (a) S_{11}, S_{21} (b) S_{11}, S_{31} (c) S_{32} of the fabricated WPD with an open stub

The designed power divider gives acceptable performance in terms of reflection, power division achieved and the isolation. The return loss is about -10 dB at the input port for 2.4 GHz as well as 5.25 GHz. Power split achieved is -3.2 dB at 2.4 GHz and -3.8 dB at 5.25 GHz. The designed WPD shows an isolation of less than -15 dB at both the operating frequencies. This completes the passive RFICs discussion and the remaining report will be dedicated to RFICs using an active device represented here by a mixer.

2.5 Conclusion

Two different designs have been presented to implement a dual band WPD and the measured results have been found to be in agreement with the desired results.

CHAPTER 3

RFIC Mixer using Active Element

The most important part of a communication system is the mixer as this is the part that translates frequency for transmission as well as translates frequency at the receiver to obtain the original baseband signal. A mixer is a three port device that accepts two input signals and at the output produces a signal at a frequency that is the sum of the two input frequencies, a signal at a frequency that is the difference of the two input frequencies, the original input frequencies and their harmonics. These frequencies are however, filtered out using an IF filter.

The basic block diagram of a mixer is as shown below:

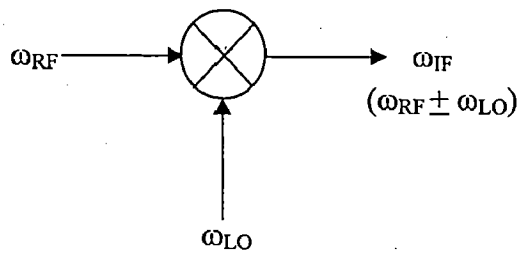


Fig.3.1: Mixer block Diagram

Whether the signal at the sum has to be retained or the one at the difference depends upon the mixer application i.e. whether it is an up converter at the transmitter or a down converter at the receiver.

Mixer operation can be represented mathematically quite simply as:

For up conversion One of the mixer inputs is a low frequency baseband signal (IF) and the other is a relatively high frequency signal (LO) represented as [23]:

$$v_{LO}(t) = \cos 2\pi f_{LO} t \tag{3.1}$$

$$v_{IF}(t) = \cos 2\pi f_{IF} t \tag{3.2}$$

The output of an idealized mixer is given by the product of the LO and IF signals:

$$v_{RF}(t) = K\, v_{LO}(t)\, v_{IF}(t) = K \cos 2\pi f_{LO} t \cos 2\pi f_{IF} t \quad (3.3)$$

$$= (K/2)\,[\cos 2\pi (f_{LO}-f_{IF})\, t + \cos 2\pi (f_{LO}+f_{IF})\, t] \quad (3.4)$$

Therefore, $f_{RF} = f_{LO} \pm f_{IF}$

where 'K' is the voltage loss or gain introduced by the mixer.

The sum and difference frequencies are called the sidebands of the carrier frequency f_{LO} with the sum term being the Upper Sideband (USB) and the difference term being the Lower Side Band (LSB).

A Double Sideband (DSB) mixer contains both USB and LSB while a (Single Sideband) SSB signal can be produced by filtering.

Similarly, ***for down conversion,*** one of the inputs is the up converted baseband signal (RF) and the other is a high frequency signal (LO) similar to the one used for up conversion.

$$v_{RF}(t) = \cos 2\pi f_{RF} t \quad (3.5)$$

The output of the mixer after multiplication with LO will be:

$$v_{IF}(t) = (K/2)\,[\cos 2\pi (f_{RF}-f_{LO})\, t + \cos 2\pi (f_{RF}+f_{LO})\, t] \quad (3.6)$$

The desired output at the mixer is the difference term in equation (5.6) and the sum term can be filtered out.

The above equations represent the operation of an ideal mixer whereas in practical mixers many more terms other than the sum and difference are produced. These products will be generated due to the more involved non-linearity of the non-linear device used. These products are known as harmonics and are removed by filtering at the output.

3.1 Mixer operation and Non-Linearity: If two signals are applied to a linear device then the output will contain signals at the same frequency as the input signals. To get output signals at the sum and difference of the input frequency as required by a mixer, it is essential to use a non-linear device to mix the two input signals. Non-linear devices used for mixing purposes are mainly diodes and transistors.

In general, the non-linearity operation of a diode comes from the fact that the V-I characteristics of a diode are non-linear. Usually, a large signal model of the diode is used for analysis because the large LO pump which has to be applied makes the small signal analysis insufficient. However, a mixer designed with a diode providing the desired non-linearity will give a conversion loss. Mixers using diodes are known as *passive mixers*.

In this report, an active mixer is the focus and so, this will be discussed in more detail.

Active mixers are basically transistor based mixers. Both BJTs and FETs can be used to design an active mixer. However FETs are preferred as compared to BJTS as they provide better noise characteristics. The main difference between an active and passive mixer is that an active mixer provides conversion gain as opposed to the conversion loss provided by a passive mixer. Diode mixers on the other hand, have a better noise figure. There are several FET parameters that offer non-linearity that can be used for mixing but transconductance is the strongest non-linearity.

The drain current $i_d(t)$ can be expressed as:

$$i_d(t) = g(t)\, v_g(t) \tag{3.7}$$

,where g (t) is the transconductance waveform and $v_g(t)$ is the gate voltage.

Since the LO pump is quite large, a large signal analysis has to be carried out. Thus, the LO pumped FET transconductance can be expressed as a Fourier series in terms of the harmonics of the LO signal:

$$g(t) = g_0 + 2\sum g_n \cos n\omega_{LO}t \quad , n = 1, 2, \ldots\ldots\infty \tag{3.8}$$

If the RF signal applied at the gate is $v_g(t) = V_{RF} \cos \omega_{RF}t$, (3.7) becomes:

$$i_d(t) = g_0 V_{RF} \cos n\omega_{LO}t + g_1 V_{RF}[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t]$$

$$+ g_2 V_{RF}[\cos(\omega_{RF} - 2\omega_{LO})t + \cos(\omega_{RF} + 2\omega_{LO})t] + \ldots\ldots \tag{3.9}$$

As can be seen from (3.9) the desired down-conversion term is due to the n=1 term of the Fourier series. Therefore, the only significant co-efficient is g_1.

Since there is no explicit formula to calculate the transconductance the required Fourier co-efficient cannot be calculated directly but measurements must made to obtain these values.

Measurements typically give a value of g_1 in the range of 10mS. Thus, it can be seen that the non-linear parameters of a device can result in the formation of the sum and difference mixing products as explained above.

3.2 Mixer Terminology

- **Conversion gain** It is defined as the ratio of the output power delivered to the load at IF frequency to the input available power at the RF frequency. Mathematically, it can be represented as:

$$Conversion\ \ Gain = \frac{P_{load}}{P_{RF}} \tag{3.10}$$

$$CG\ (dB) = 10\ log_{10}\ (CG) \tag{3.11}$$

A down conversion active mixer must provide sufficient gain to compensate for the IF filter loss, any noise contribution at the input and output stages. This gain must not become large enough to saturate the mixer output.

- **Noise figure** It is a measure of the signal degradation caused by the circuit. It is defined as a ratio of SNR at the output to the SNR at the input.

$$Noise\ Figure = \frac{SNR_{output}}{SNR_{input}} \tag{3.12}$$

where SNR is the signal to noise ratio

In a mixer, the NF can be SSB NF or DSB NF. Analysis shows that $(NF)_{SSB}$ is twice the $(NF)_{DSB}$.

- **Inter-modulation distortion** Inter-modulation products are signals formed at the output of a mixer at frequencies that are not harmonics of either of the input frequencies. They are basically linear combinations of the fundamental frequencies. Higher the amplitude of the input signals, more pronounced is the inter-modulation distortion. The third order inter-modulation products are closest to the fundamental frequencies and have the highest amplitude. Therefore, a measure of the third order inter-modulation product (TOIP) is a measure of the linearity of the device i.e. how well a device performs in the presence of large signals.

- **Gain compression** A large input signal can saturate the mixer and a 1 dB compression point at the input gives a measure of the input power level that causes the mixer to deviate from its linear magnitude by 1 dB.
- **Isolation** This quantity measures the coupling between the RF-LO signals as well as the coupling between the applied input signals and the IF signal at the output. This is an important quantity as the FCC sets stringent limits on the power radiated by receivers.

3.3 Topologies of Dual Band Active mixers

An active mixer uses BJTs and FETs to perform mixing action. FETs are preferred due to their low noise performance. For dual band operation, FETs can be arranged in the topologies shown in fig.3.2.

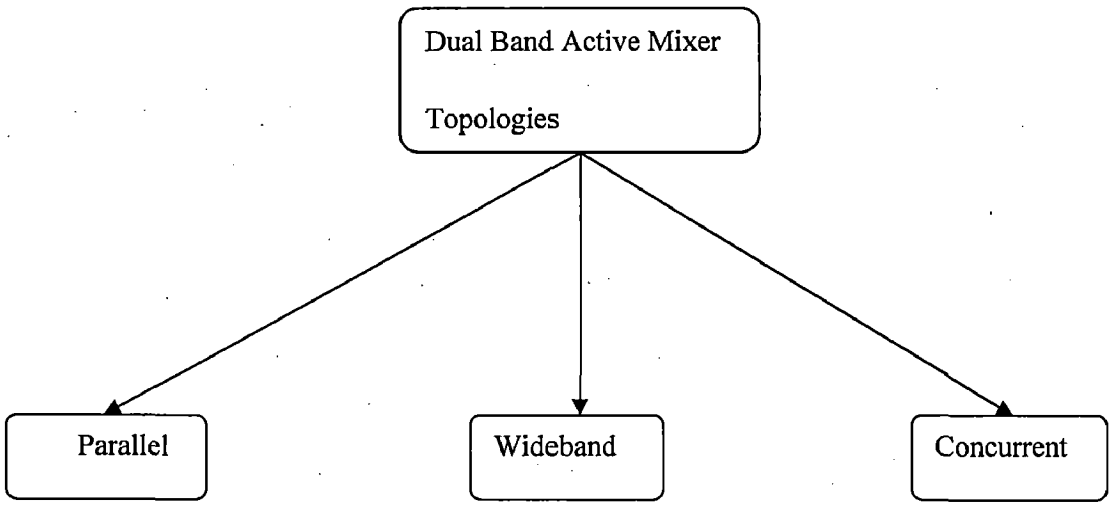


Fig.3.2: Topologies of Dual Band Active Mixer

Of these three topologies, Parallel and Wideband architecture active mixer design will be presented. The subsequent sections of this chapter will describe in brief the methodology followed to design a mixer. This methodology will be followed to design parallel and wideband mixers in the subsequent chapters. Single gate FETs will be used to design both.

3.4 Methodology for Designing Mixers

3.4.1 DC Analysis

The first and foremost step is to choose the operating point for the single gate FET mixer operation. There are primarily three mixing modes for single gate FET mixers. They are: Transconductance mixer, Drain mixer, Resistive mixer [14].

The bias point selection for a single gate FET depends upon the mixing mode chosen for operation. The typical bias point chosen for each of the mixing modes is as shown below [14]:

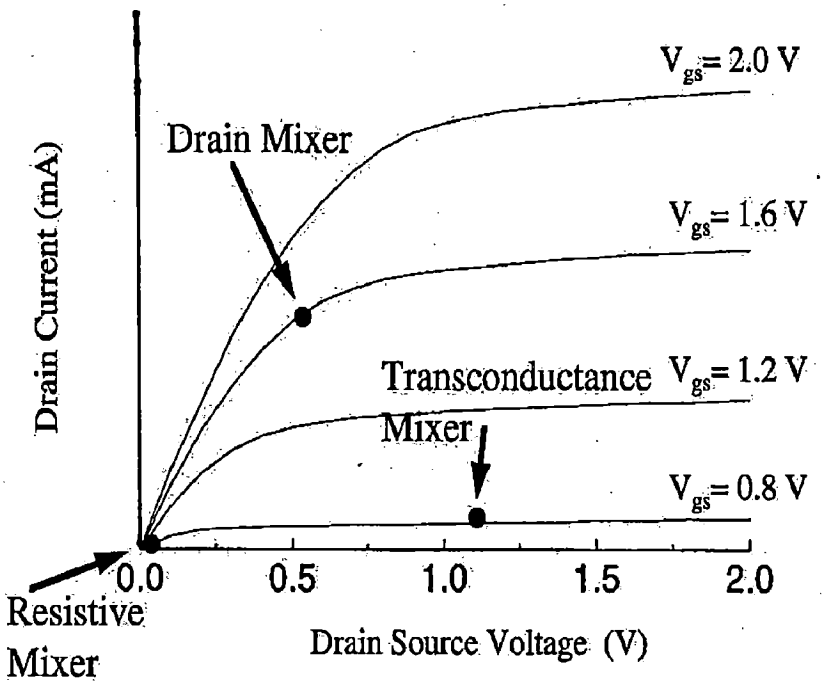


Fig.3.3: Bias points of a transconductance, drain and resistive mixer

- A ***FET transconductance mixer*** operates by changing the gate source voltage, which swings the FET from saturation to cut-off region. It is usually biased at the threshold with a 50% duty cycle which maximizes the gain. It must be ensured that the FET never enters the linear region of operation. To meet this criterion the drain source voltage should be large and kept constant.

- A ***FET drain mixer*** operates by a drain fed LO modulating the drain-source voltage of the device. This voltage is responsible for swinging the FET from the linear region to the saturation region. However tempting this might seem to

obtain the necessary RF-LO isolation, their performance is not good enough as compared to a transconductance mixer.

- A ***FET resistive mixer*** operates by modulating the channel resistance between the drain and the source with a large LO signal while keeping the FET in the linear region of operation. The FET channel is switched between fully depleted and fully inverted regions of operation. The channel resistance varies between infinite and a very low value. A drain source bias is not required to keep the FET in the linear region. Therefore, the FET resistive mixer is also known as a passive mixer. The LO is applied to the gate along with the gate DC bias. The main characteristic of this mixer is the low inter-modulation products which result from the fact that the FET channel resistance is very linear in this region of operation ($V_{DS} = 0$). This type of mixer however, suffers from two major disadvantages:

    - It requires a large LO power as compared to the two active mixers described above.

    - Despite using a transistor, it provides a conversion loss instead of a conversion gain.

  Thus, the appropriate operating point is chosen depending on the kind of mixer mode chosen from the three mentioned above.

3.4.2 Bias Network Design

There are many ways of biasing a transistor to obtain the necessary operating point. They are mentioned briefly below:

- **Using an adjustable resistor divider network** The most obvious method of biasing FET is to supply separate DC voltages to the gate and drain terminals such that the gate supply can be varied i.e. it is adjustable. In practice, the gate supply is usually a fixed DC voltage source varied by employing an appropriate resistor divider network to supply the required gate voltage. The source is grounded in this case. The maximum gain is obtained from a FET when the source is grounded and hence, this is preferred if a high efficiency is required.

- **Using a self-bias network** In this, a resistor of appropriate value is chosen to be placed between the source and the ground terminals. A source bypass capacitor is placed in parallel with the resistor to prevent the RF signal from loading the transistor i.e. the RF signal at the operating frequency sees a short to the ground via the bypass capacitor. The major advantage of this biasing is that only a single positive supply is needed to power up the transistor. This configuration also provides better stability to the transistor. The advantages are however diminished by the reduction in the efficiency due to the voltage drop across the source resistor. Moreover, the bypass capacitor cannot provide RF ground to all frequencies as compared to the RF grounding provided with via holes. It is for this reason that self-bias networks are used in designing LNAs but not in power amplifiers, mixers etc. where harmonics of fundamental frequencies are also involved.

- **Using an active bias network** This circuit uses another FET to maintain the main FET at the desired operating point. This analog circuit prevents any change in the FET Q-point by adjusting itself to provide the required gate bias. Any changes in the Q-point cause the network to determine the gate voltage to be supplied to bring the Q-point back to its original intended position.

- **Using a bias Tee** Bias Tees are used to supply DC voltages and currents to RF devices such as FETs etc. Bias Tees are basically diplexers which choose their path depending on the incoming frequency. The basic schematic of a bias tee is shown in fig.3.4 to understand its operation better.

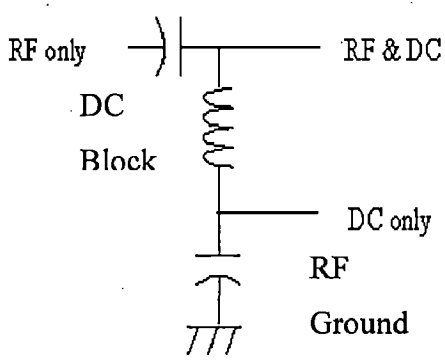


Fig 3.4: Schematic of a simple Bias Tee

The applied RF signal shown in the figure passes through the DC block capacitor and goes on to the RF and DC terminal shown above. The DC block capacitor prevents any stray DC voltages or currents from entering the circuit which might

cause the operating point of the transistor to shift. The ideal case would be that the RF sees an open circuit at the bias network. In case any RF signal passes through the inductor (RF choke) it sees a short to the ground via RF ground capacitor shown above. On the other hand, the applied DC sees an open circuit to the ground and pass through the inductor which acts as a DC feed. Usually, the DC source is preceded by a high value resistor to completely eliminate any probability of the RF signal loading the DC source as an AC signal sees an ideal DC source as a short circuit. In microstrip implementation, the inductor can be replaced by a high impedance line and the capacitor can be implemented as an open stub. The length of the high impedance line representing the inductance is kept ($\lambda/4$) so that the RF signal sees the open stub as a capacitor shorted to ground. This makes the grounding through via hole unnecessary and prevents introducing losses into the circuit. The only disadvantage of this bias network is that is occupies a relatively large area. Therefore, in a microstrip implementation this bias network may look like this:

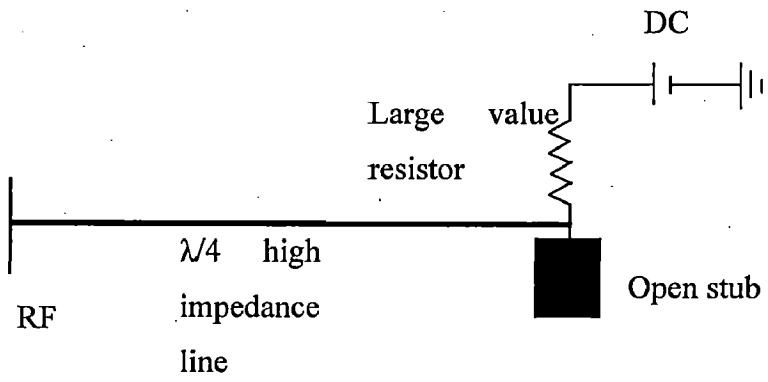


Fig.3.5: Bias network in microstrip

This is a commonly used bias circuit and its performance parameters are RF bandwidth, insertion loss and mismatch at the two RF ports and the maximum DC current depending on the device being used as specified on the manufacturer's datasheet.

- **Using gate or drain resistors** This is the most common method for biasing a transistor. This method has the additional advantage of providing stability to the transistor operation apart from being able to bias the transistor. There are four

possible configurations for this method. They are using a series gate resistor, shunt gate resistor, drain gate feedback resistor, shunt drain resistor

The bias network must be chosen carefully as all bias networks may not provide stability to the transistor. Moreover, for the resistor based bias networks, the simplest possible bias networks must be chosen to obtain a stable operation of the transistor in the desired region because as the number of resistors increase the loss in the circuit increases and the noise performance is also compromised.

3.4.3 Transistor stability

The next step is to ensure that the chosen bias network is providing stability to the transistor. To check the transistor stability, the transistor is biased at the chosen operating point using the selected biasing network. The S-parameters of the transistor are then measured at this operating point. The conditions for transistor stability are:

$$K > 1 \tag{3.13}$$

$$\text{and, } |\Delta| < 1 \tag{3.14}$$

where,

$K = 1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2$ and

$\Delta = S_{11} S_{22} - S_{12} S_{21}$

The transistor has to be stable in the entire desired frequency range of operation.

3.4.4 Impedance Measurement and Matching Networks design

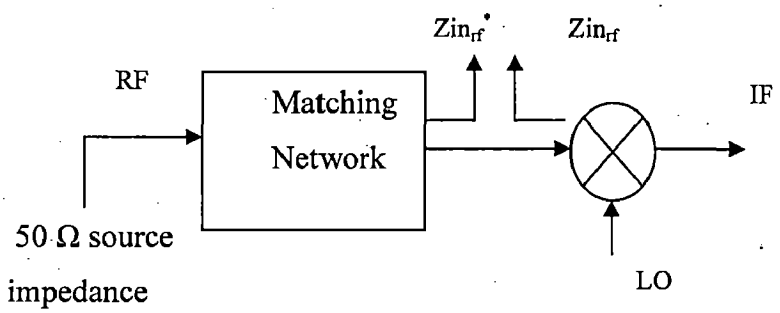
Once the transistor has been stabilized in the desired frequency range at the fixed operating point, the next step is to measure the input impedance at RF and output impedance at IF at the input and output terminals of the transistor respectively. Since the device is not unilateral, the presence of a short circuit on one side of the device will affect the impedance seen on the other side of the device.

- To design the input matching network, the input impedance has to be measured at RF while short circuiting the IF. The LO signal is very close to the RF signal and hence, to measure the input impedance LO signal cannot be shorted at the input terminal. Instead, the IF is shorted at the input and optimization is carried out to match the input

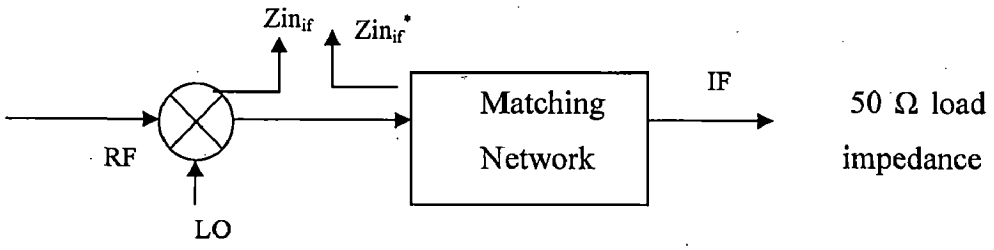
impedance measured at RF to 50 Ω of the input line impedance. Thus, the impedance seen at each frequency is different for each terminal.

- To design the output matching network, the output impedance has to be measured at IF while short circuiting all RF and LO signals. The output matching network has to match the impedance measured at IF to the output 50 Ω output line impedance.

The purpose of impedance matching is to transform maximum power from one impedance to another. According to maximum power theorem, this can be achieved when the impedances are conjugate matched. Since the impedances seen at RF and IF ports must be conjugate matched so that they can be transformed to 50 Ω, for RF and IF ports the impedance matching should be as shown in fig. 3.7.



(a)



(b)

Fig.3.6: Conjugate matching at (a) RF port and (b) for IF port for maximum power transfer

This will transfer power from the input of the transistor to the output seamlessly without any losses. All the matching networks are designed conforming to this condition. An ideal matching network transfers power without any losses but practically losses may be

introduced due to errors in fabrication, parasitic losses, minor changes in the matching network component values. They are usually filters like resonant structures have a single resonant frequency at which they match the source and the load for maximum power transfer. They typically exhibit narrowband behavior and any slightest change in the incoming frequency can lead to a mismatch leading to degradation in the signal level. However, multiband and wideband circuits have been designed despite these limitations using various techniques.

3.4.5 HB Analysis and Matching Optimization

The final step in mixer design is carrying out HB analysis and optimizing the input and output matching networks if required, for bringing the matching elements values and hence, their implementation into realms of practical realization. Parallel and wideband architecture mixers are designed and analyzed using the methodology described above.

3.4.6 Conclusion

The steps to be followed sequentially to design and analyze a mixer can be summarized as shown below in fig.3.7.

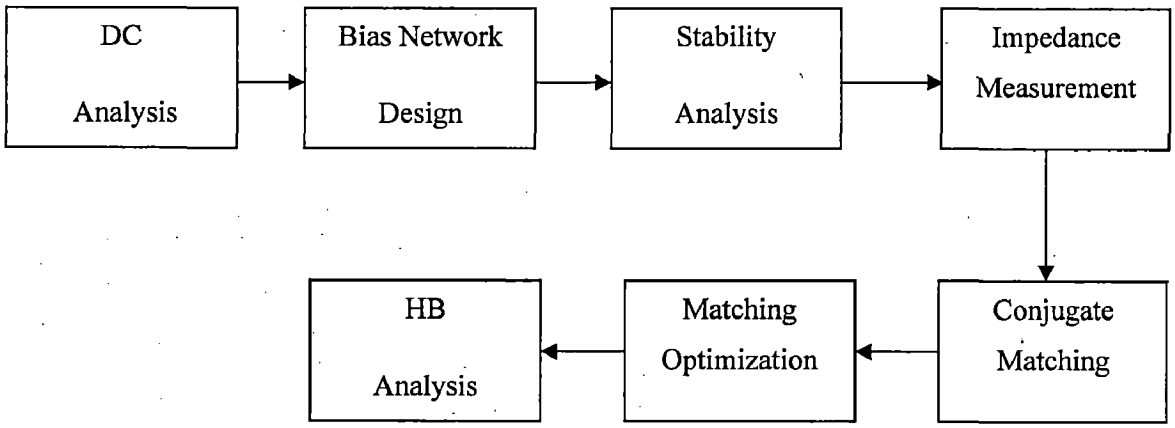


Fig.3.7: Mixer design and analysis steps summary

This chapter provided an insight into the mixer operation and emphasized on the importance of a mixer in communication system. It also provides a design methodology to be followed for successful design of a mixer.

CHAPTER 4

Design and Analysis of Dual Band Active Mixer

This chapter presents the actual design and analysis of a dual band active mixer using:

- Wideband Architecture
- Parallel Architecture

The chapter will end with a comparison of both the architectures and their results.

Operating Frequencies: $f_1 = 2.4$ GHz and $f_2 = 5.25$ GHz

IF: for Wideband Architecture = (i) 300 MHz

(ii) 140 MHz

for Parallel Architecture = 300 MHz

Transistor used: NE4210S01 (operating range: 2-18 GHz)

Substrate parameters: $\varepsilon_r = 2.2$, h = 10 mil = 0.254 mm

Design Specifications: 1. Conversion Gain > 0 dB

2. Noise Figure > 5

4.1 Wideband Architecture

The design of a mixer using parallel architecture follows the sequence of steps explained in the previous chapter. The matching network design to make the mixer operational in the frequency range 2GHz to 6 GHz.

4.1.1 DC Analysis

The mixer is designed to operate as a transconductance mixer and hence, the operating point is chosen as in fig.4.1 for mixer performance.

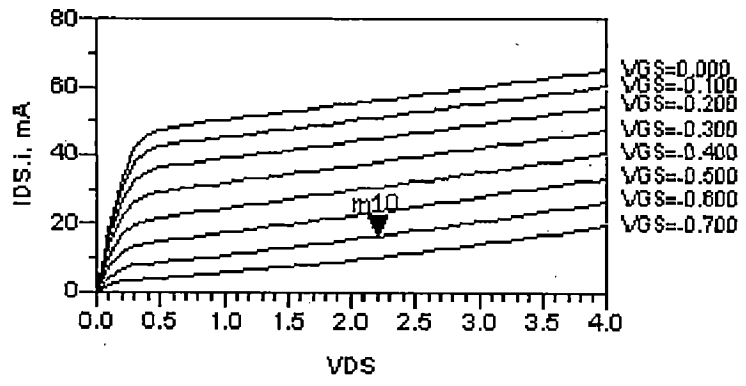


Fig.4.1: Operating Point Selection for transconductance mixer

Selected operating point: $V_{DS} = 2$ V, $I_{DS} = 10$ mA ($V_{GS} = -0.6$ V)

4.1.2 Bias Network

The broadband bias network was first designed in microstrip as shown in fig.4.2.

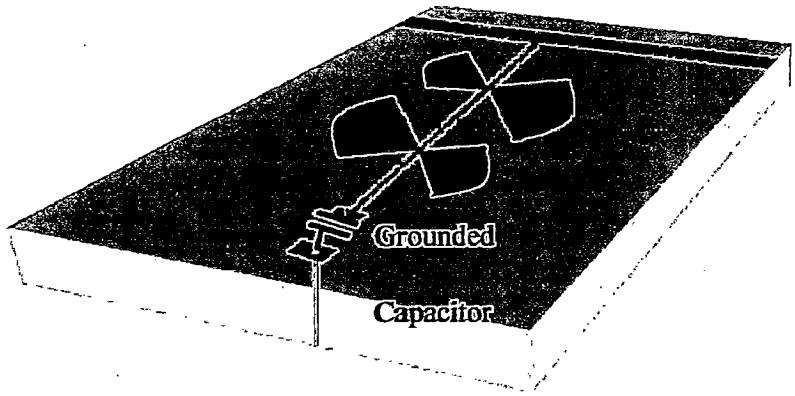


Fig.4.2: Broadband Bias network

Instead of using a single radial stub as in fig.3.5, multiple radial stubs are chosen for the design of the bias network. As shown in fig.4.2, it resembles a butterfly structure. The dimensions of the network are shown in table 4.1.

Table 4.1 (a) : Dimensions of broadband bias network in microstrip
For 3.825 GHz

Z_0 (Ohms)	W (mm)	L (mm)
50	0.759	Arbitrary(taken 5)
100	0.204	14.9086

Radial stub dimensions are [27]:

Table 4.1 (b) : Dimensions of radial stub in broadband bias network in microstrip

α (degrees)	r_1 (mm)	r_2 (mm)
66	0.3	10.0824

The S-parameters are measured to check the broadband performance of the circuit shown in fig.4.4.

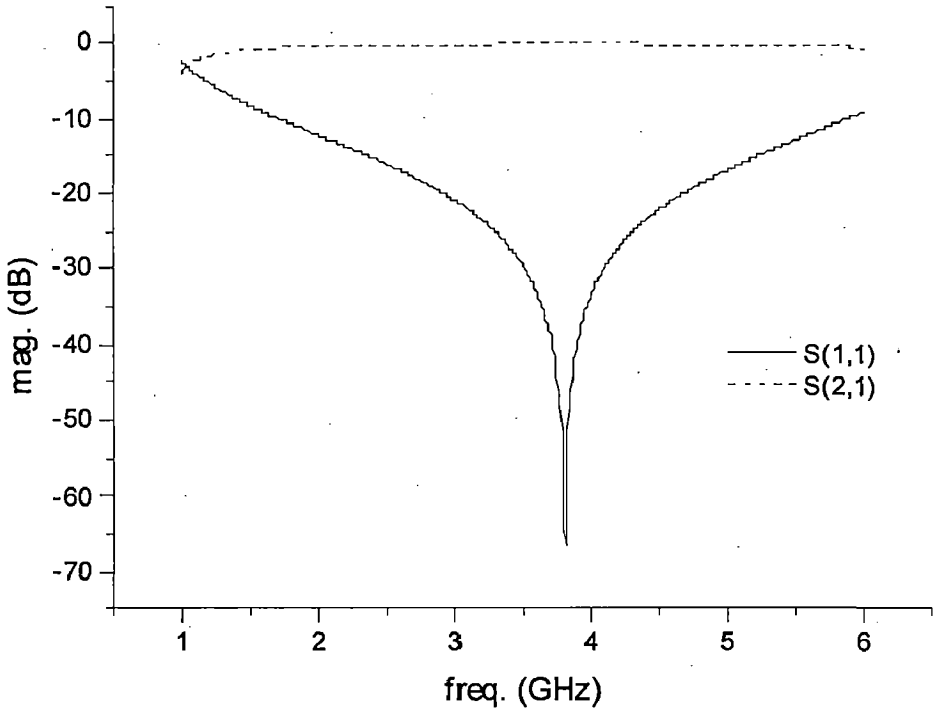


Fig.4.3: S_{11} and S_{22} of the broadband bias network

However, this does not provide stability to the transistor as shown in fig.4.4:

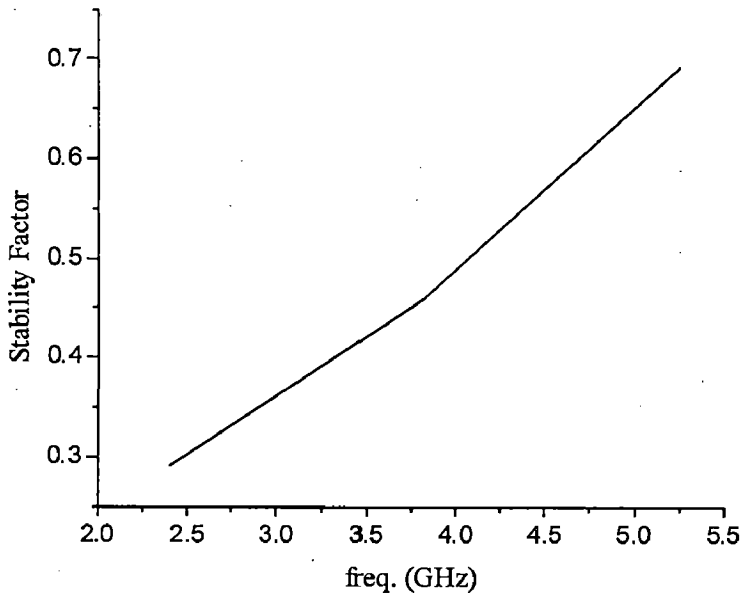


Fig.4.4: Plot showing K<1 using broadband biasing network

Therefore, it is necessary to change the bias network to provide stability to the transistor. The alternative bias network is chosen as a ***shunt gate resistor*** of value 100 Ω. This technique high impedance to the RF and also stabilizes the transistor. A shunt gate resistance prevents oscillations by effectively cancelling out the negative resistance of the active device. The reason for choosing **100 Ω** is the availability of a chip resistor of the value so that there is no need to solder more resistors in series and parallel thereby increasing the losses. Also, a 100 Ω resistor has served its purpose of stabilizing the transistor and the value is large enough to prevent any RF leakage into the bias resistor.

The method of using the shunt gate resistor has some disadvantages:

- The shunt gate resistance increases the loss of any series impedance terminating the gate terminal.
- The shunt gate resistance degrades the noise figure slightly.

Both these factors however, do not undermine the ease of using the shunt gate resistor for bias. Moreover, the noise figure degradation is not by a large amount i.e. about 1 dB. The stability factor 'K' plotted w.r.t. frequency now represents a stable transistor with K>1 as shown in fig.4.5.

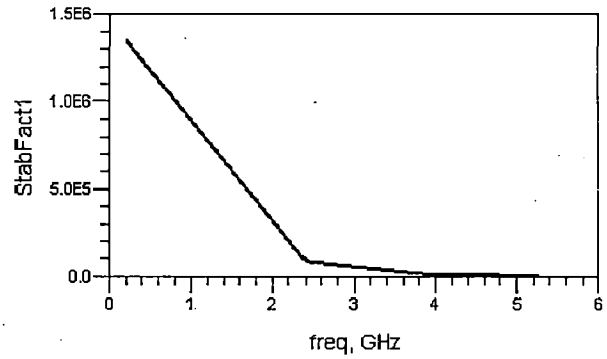


Fig.4.5: Plot showing K>1 after shunt gate resistor is added

4.1.3 Impedance measurement

The next step is to design the matching networks at the input and output. To measure the input and output impedances for matching, short circuit the IF at the RF input side and

the RF/LO at the output side as explained in the previous chapter. The values found are listed in table 4.2 :

Table 4.2: Input and output impedances at RF and IF

Freq. (GHz)	Impedance at RF port (Ohms)	Impedance at IF port (Ohms)
0.14	0.99 – j 2.457e-4	934.097-j147.323
0.3	0.990 – j 3.561e-4	859.830 – j 285.918
2.4	83.250 – j 21.251	1.0 – j 0.003
4	72.717 – j 30.371	0.999 – j 0.005
5.25	63.811 - j 33.985	0.999 - j 0.006

4.1.4 Design of Wideband Matching Network

The concept used in designing the matching network for a wideband operation is that the quality factor, 'Q' of a circuit is inversely proportional to the bandwidth provided by the circuit. Therefore, if a matching network is designed with a low Q then the matching circuit can provide wideband operation. The components of the matching network themselves have a low Q. The value of Q for 3 dB bandwidth is given by [15]:

$$Q = \frac{\sqrt{f_1 f_2}}{f_2 - f_1} \tag{4.1}$$

Where, f_2 = Upper frequency

f_1 = Lower frequency

The idea of impedance matching is to transform the input and output impedance to 50Ω for maximum power transfer i.e. the target is to reach the centre of the Smith Chart. The methodology for broadband matching can be summarized as:

- Plot the Q circle.
- Plot the impedance to be transformed.

- Traverse the path between the plotted impedance and the centre of the Smith Chart within the bounds of the real axis and the Q circle.
- Each hop between the real axis and the Q circle represents an L-C section.
- The number of L-C sections required is determined by the number of hops required between the real axis and the Q-circle to reach the Smith Chart centre.
- The values of the elements so obtained will have a low Q sufficient to provide broad band matching.

The above is now applied to the current problem to design a wideband matching circuit at 4 GHz so that impedance matching at 2.4 GHz and 5.25 GHz can be obtained simultaneously.

In this case, $f_1 = 2$ GHz and $f_2 = 6$ GHz with a centre frequency of 4 GHz. Substituting in (4.1),

$$Q = 0.866 \tag{4.2}$$

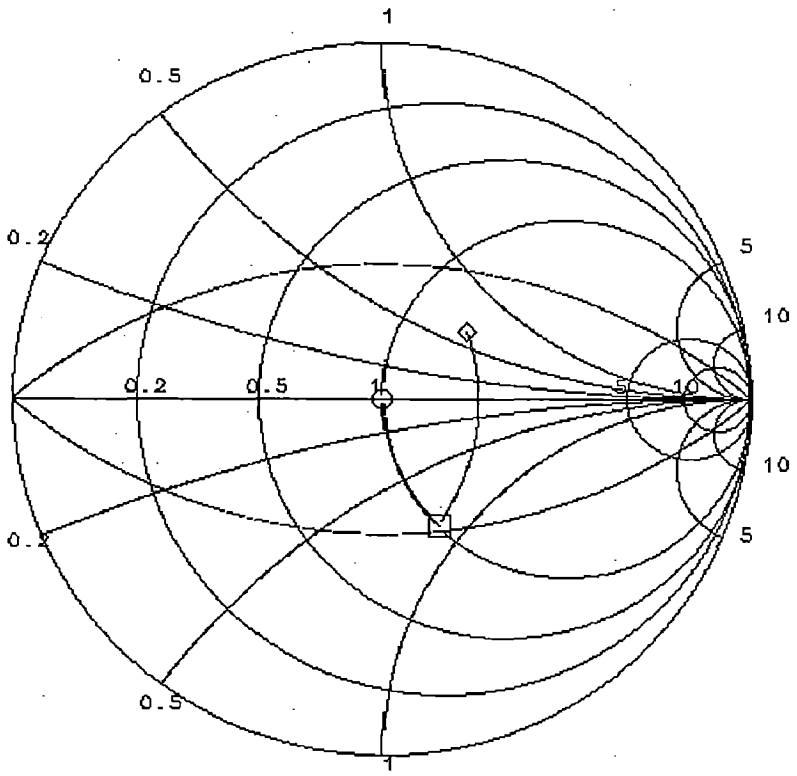


Fig.4.6: Smith Chart traversal within Q-circle

The component values of the impedance matching network obtained at the input at 4 GHz is :

Table 4.3(a) : Component values of wideband impedance matching network at 4 GHz

Component	Value
Shunt C	0.583 pF
Series L	1.67095 nH

The output matching network is designed by direct conjugate matching using a Smith chart and the values obtained are:

Table 4.3(b) : Component values of output impedance matching network at 300 MHz

Component	Value
Shunt C	2.55 pF
Series L	112.85 nH

4.1.5 IF matching circuit Optimization

The output IF is chosen to be 300 MHz so the output network can be designed simply by using a Smith Chart as described above. What has not been considered up till now is that the output network contains a 112.85 nH inductor that is practically not feasible to realize. Thus, the output IF network must now be optimized to bring the circuit into the realms of practicality. Also, it would be advisable to have a DC block at the output to prevent the applied drain DC voltage to appear at the output. Thus, considering all the constraints another possible matching network is chosen. The network is:

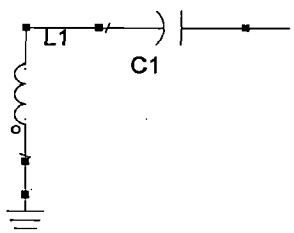


Fig.4.7: Changed IF output matching network

Table 4.4: Component values of the changed IF network

Component	Value
Shunt L	129.17 nH
Series C	2.49 pF

The obvious advantages of the architecture are that the shunt inductor though of a large value can be replaced with a parallel L-C circuit thereby reducing the value of the inductor and simultaneously providing a large enough capacitance to act as an RF/LO short at the output. The inductor can also be used as an RF choke at the drain thus increasing the functionality of the circuit.

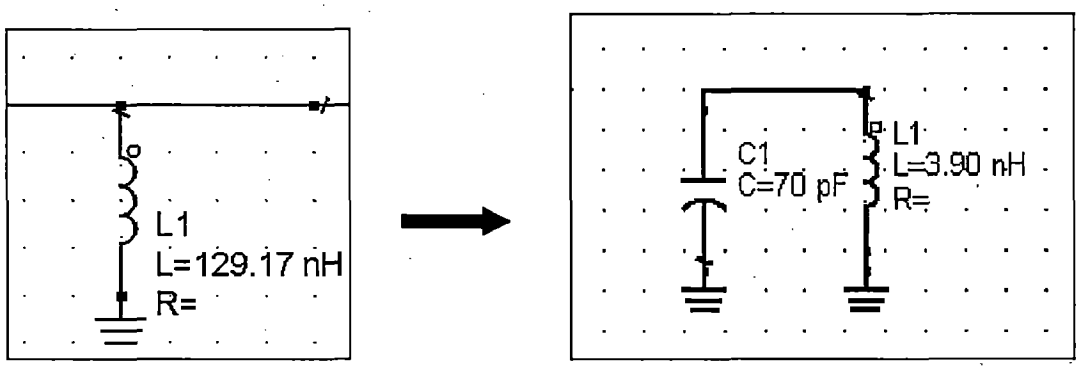


Fig.4.8: Modification of shunt inductor into parallel LC in IF output matching network

The second modification necessary is to replace the series capacitor in fig.4.7 with a series L-C circuit to provide enough impedance to the RF signal at the output. The values obtained are:

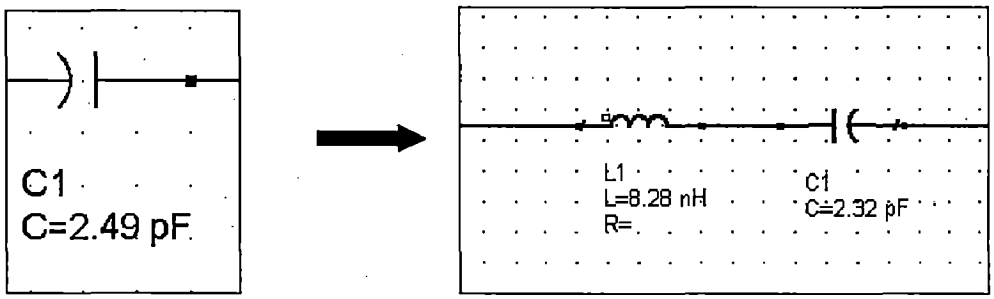


Fig.4.9: Modified equivalent of the series capacitor in output IF matching network

Table 4.5: Component values of optimized output IF =300 MHz matching circuit

Component	Value
Shunt L	3.90 nH
Shunt C	70 pF
Series C	2.32 pF
Series L	8.28 nH

The final circuit for IF becomes:

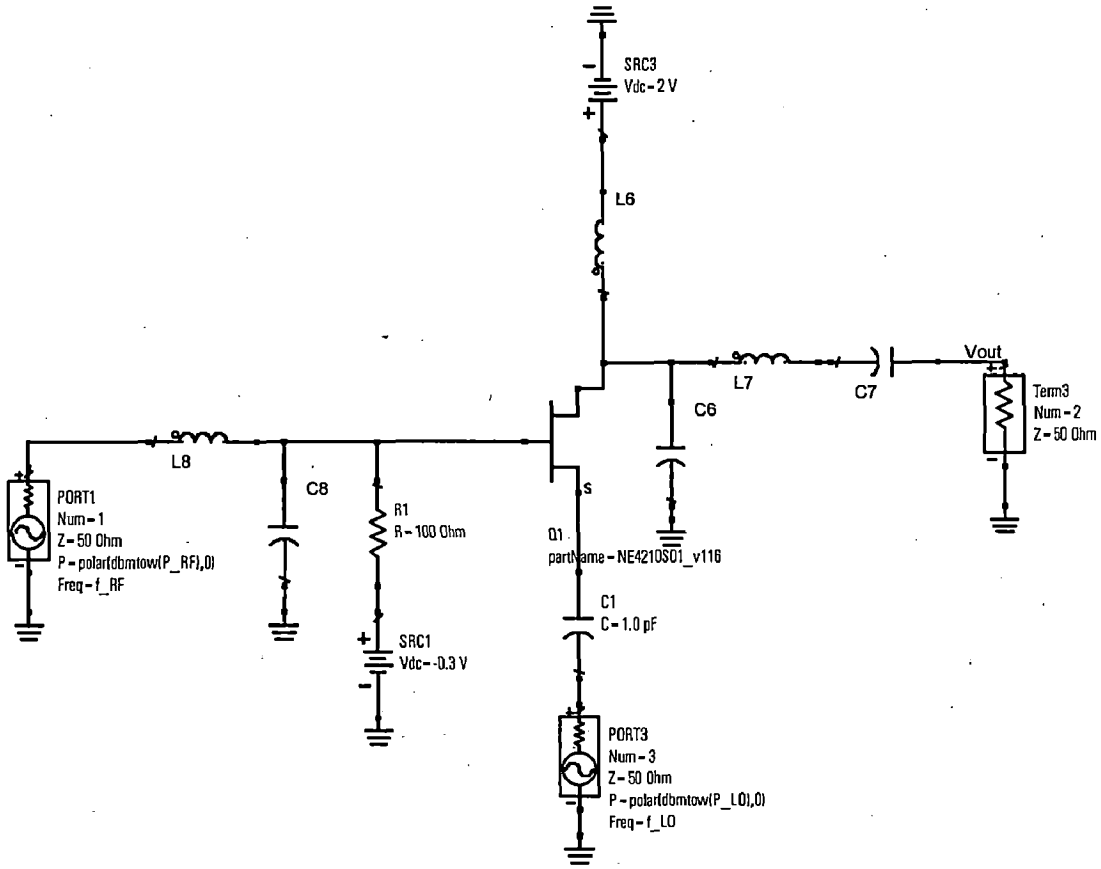


Fig.4.10: Wideband architecture with optimized IF (300 MHz) network

A similar approach is followed for 140 MHz IF and the output IF circuit is optimized for maximum functionality. Table 4.6 shows the component values.

Table 4.6: Component values of optimized output IF =140 MHz matching circuit

Component	Value
Shunt L	10 nH
Shunt C	124.37 pF
Series C	5 pF
Series L	16.5 nH

The optimized circuit for 140 MHz IF is shown in fig.4.11:

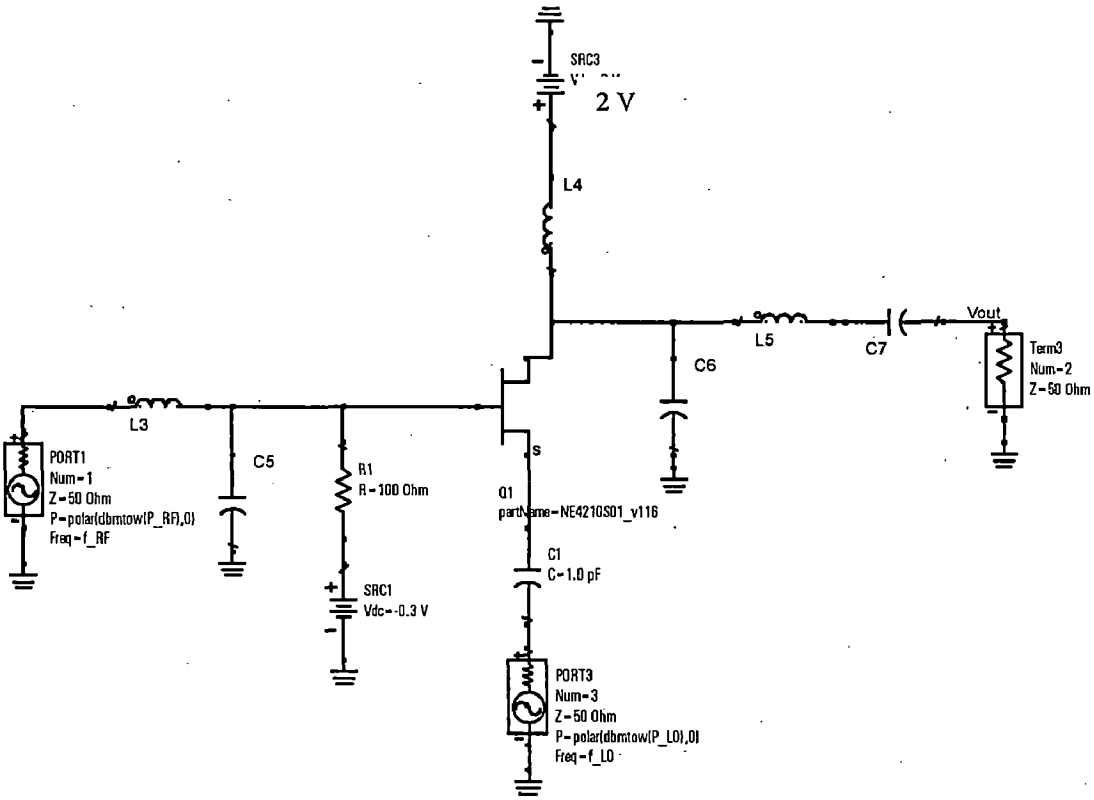
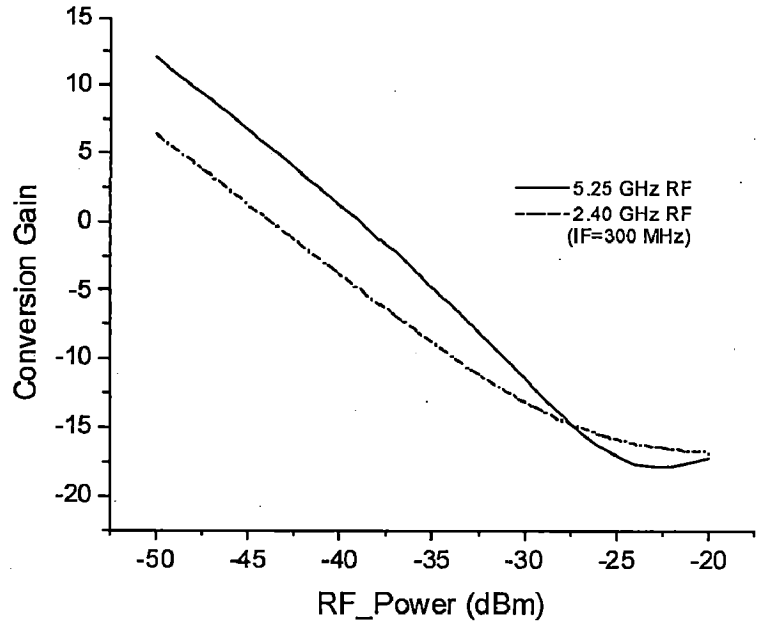


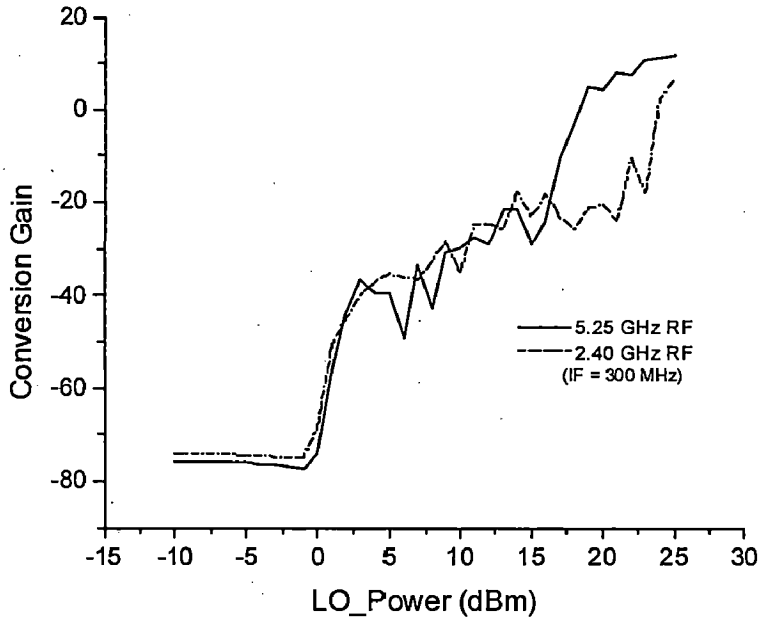
Fig.4.11: Architecture with optimized IF (140 MHz) network

4.1.6 HB Analysis of wideband Architecture

For IF = 300 MHz



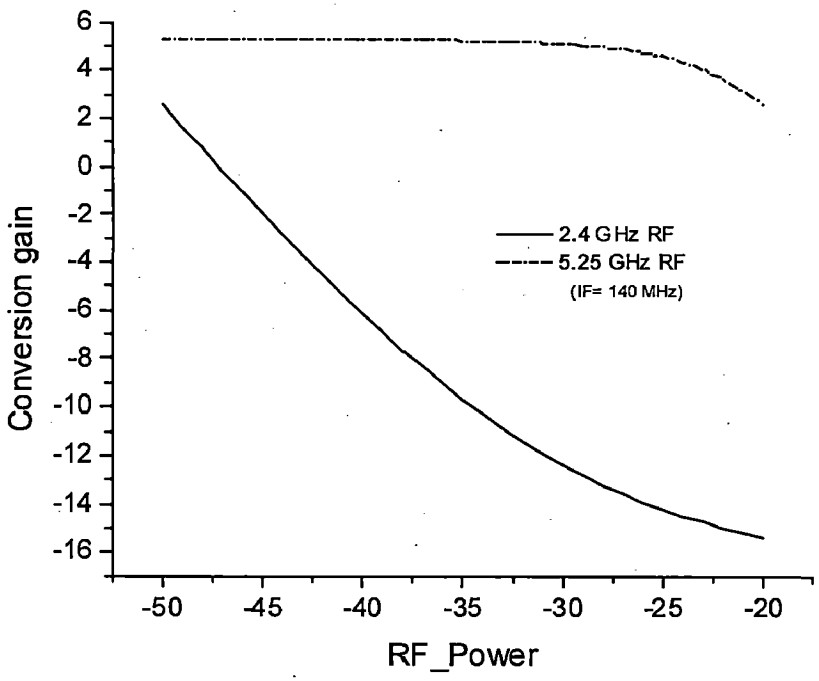
(a)



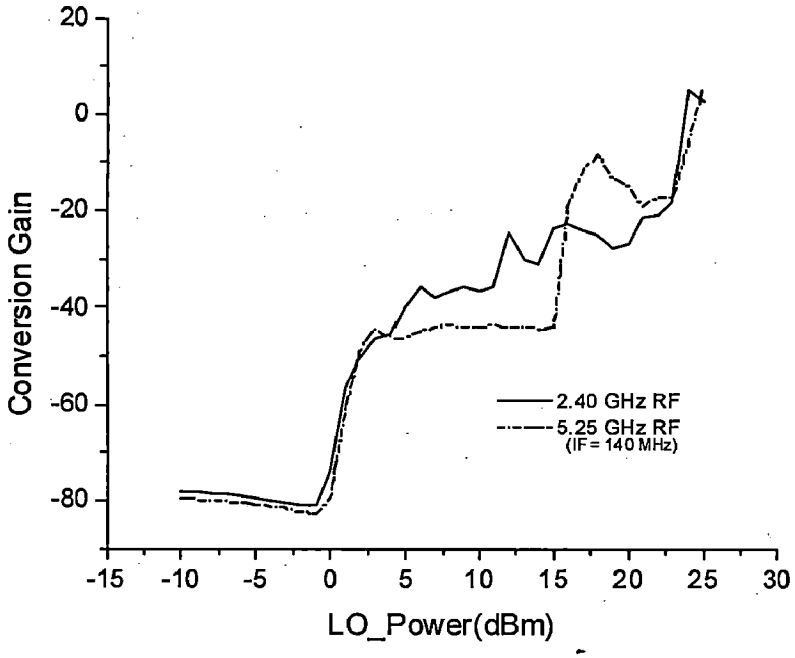
(b)

Fig.4.12: (a) CG vs RF power (b) CG vs LO power obtained after HB simulation of the wideband mixer (IF=300 MHz)

For IF=140 MHz,



(a)



(b)

Fig.4.13: (a) CG vs LO power (b) CG vs RF power obtained after HB simulation of the wideband mixer (IF = 140 MHz)

The wideband architecture has been designed and HB analysis is carried out for 300 MHz IF and 140 MHz IF. The results show that the wideband architecture circuit can be optimized for any of the above IF. The only problem however, of the 140 MHz design is that the dimensions of the transmission line equivalents of the lumped elements are large and it becomes slightly difficult to draw a layout in such a way so as to prevent coupling between lines in microstrip. However, it is possible to optimize the circuit for a 140 MHz IF as well.

Table 4.7: Comparison between circuit simulation of wideband architecture for IF=300 MHz and IF=140 MHz

Parameters	IF= 300 MHz		IF = 140 MHz	
	2.4 GHz RF	5.25 GHz RF	2.4 GHz RF	5.25 GHz RF
CG	6.372	12.059	2.533	5.729
NF	7.544	11.930	8.706	13.968

Table 4.8: Comparative results of optimized and un-optimized Wideband architecture (IF=300 MHz)

Parameter	Un-optimized IF matching wideband Architecture		Optimized IF matching wideband architecture	
	2.4 GHz RF	5.25 GHz RF	2.4 GHz RF	5.25 GHz RF
CG (dB)	3.597	4.305	6.372	12.059
NF (dB)	10.124	9.104	7.544	11.930

Thus, results show that the optimized IF matching network gives a much better CG and NF.

4.1.7 Non-Linear Analysis of Active mixer

A full wave analysis is the most accurate form of analysis of a design. It is set to include all the parasitic and stray losses that might occur in the circuit. This simulation is carried out after drawing the layout. The method for full wave analysis is:

- Draw the complete layout of the circuit.
- Define the ports at each part of the layout.
- The input and output ports are defined as single ports.
- The remaining ports are placed wherever any active device or lumped components are placed and wherever any external connection has to be made for instance, sources, ground etc. These ports are defined as internal ports.
- The entire layout is then turned into a component to be used in the schematic window. The lower and upper frequencies of the circuit operation are defined and a component is created to be used in the schematic window.
- The active devices or their S-parameter files and the sources, ground, lumped elements are connected at their respective ports.
- Simulation is setup normally as in a schematic window. Momentum simulation is carried out first which is followed by a circuit simulation.

This is represented in the fig.4.14.

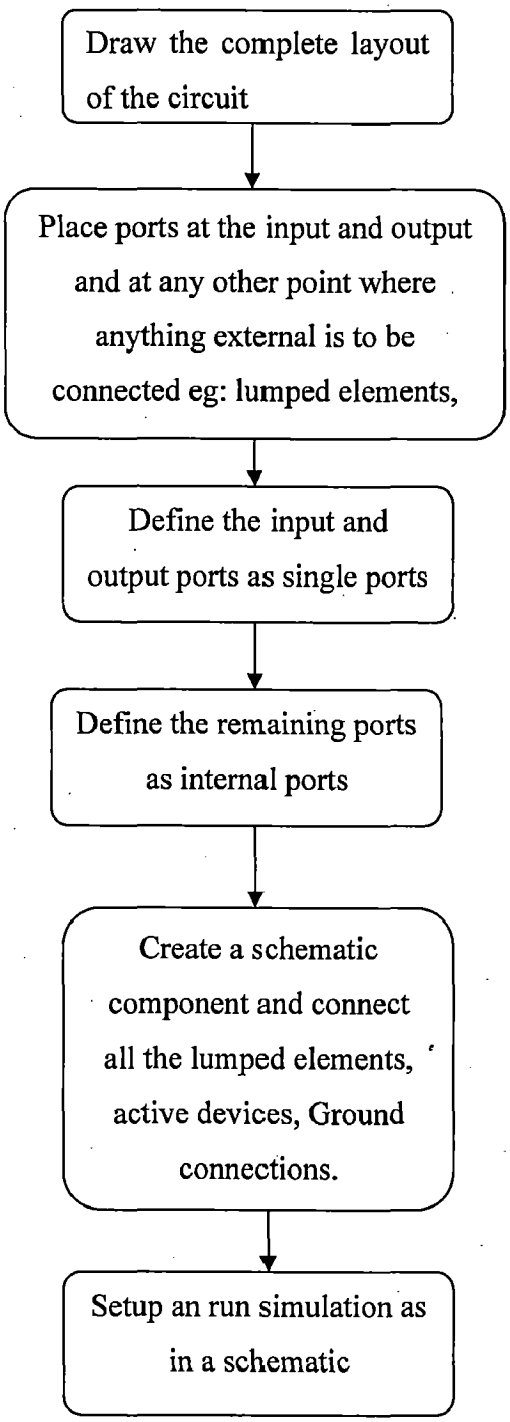
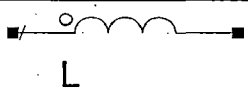
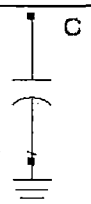


Fig.4.14: Co-simulation steps

The layout of the circuit shown in fig.4.15 is created by using the transmission line equivalents of the lumped elements wherever possible.

On the input side, at 4 GHz,

Table 4.9 (a) : Transmission line equivalents of the lumped elements on the input side of wideband architecture

Lumped Element	Value	Transmission Line equivalent	Width, W (mm)	Length, L (mm)
	1.67095 nH		0.204040	3.933
	0.583 pF		1.55817	3.533

On the output side, at 300 MHz

Table 4.9(b): Transmission line equivalents of the lumped elements used on the input side of wideband architecture

Lumped Element	Value	Transmission Line equivalent	Width, W (mm)	Length, L (mm)
	8.28 nH		0.2641	19.48
	3.90 nH		0.261	9.8337

The complete layout is shown in fig.4.15.

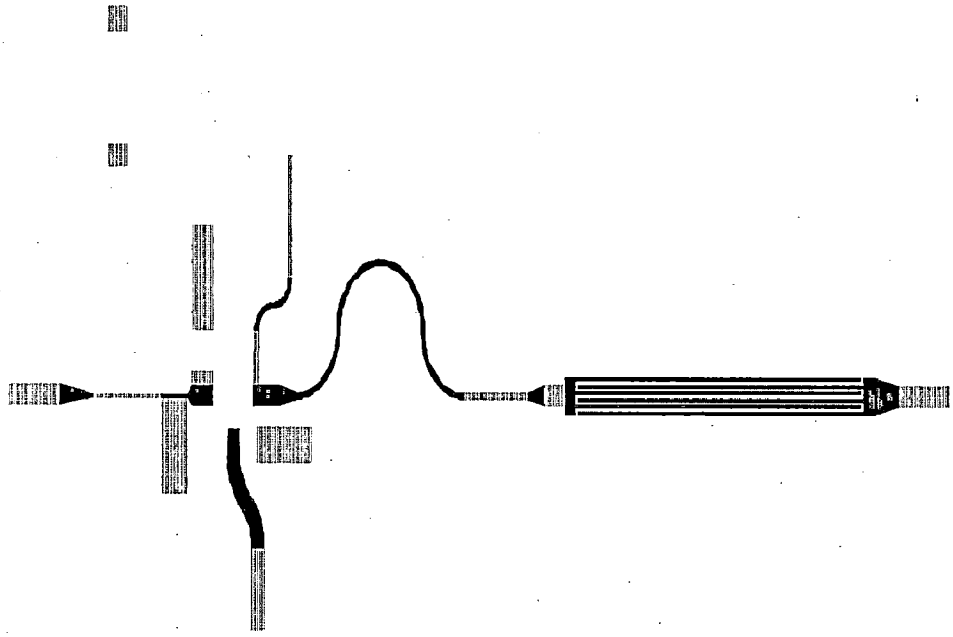


Fig.4.15: Complete layout of the wideband mixer (layout not to scale)

The dimensions of the layout are 5 cm x 2.1 cm. In comparison to the parallel architecture this is a huge advantage.

This layout is used to create a component to be used in the schematic.

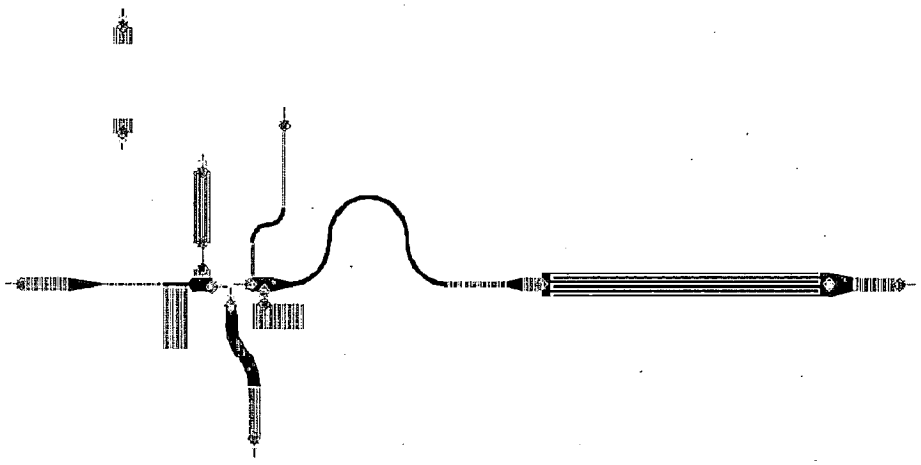
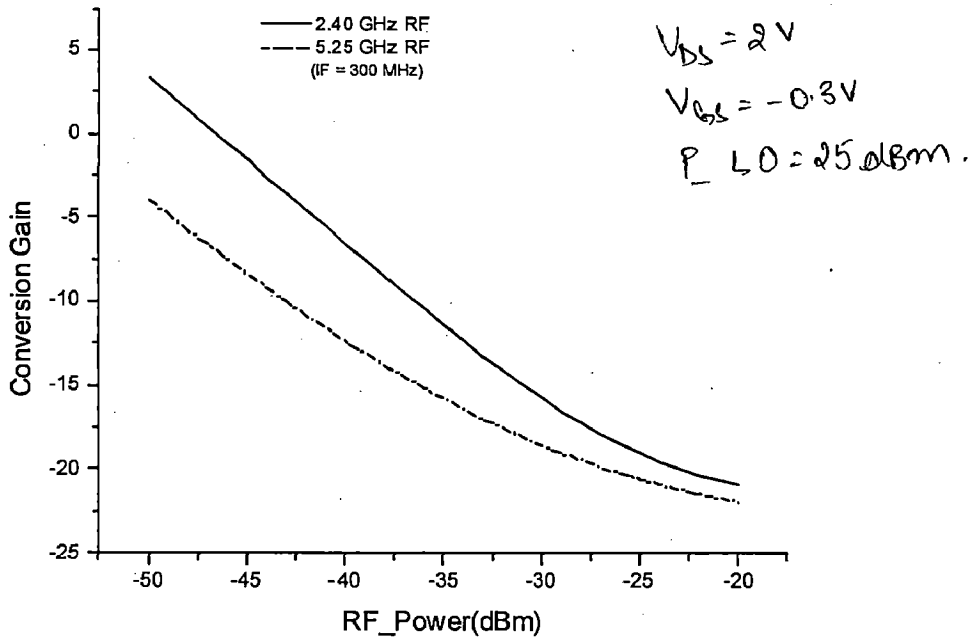


Fig.4.16: Layout with internal and single ports defined (Layout not to scale)

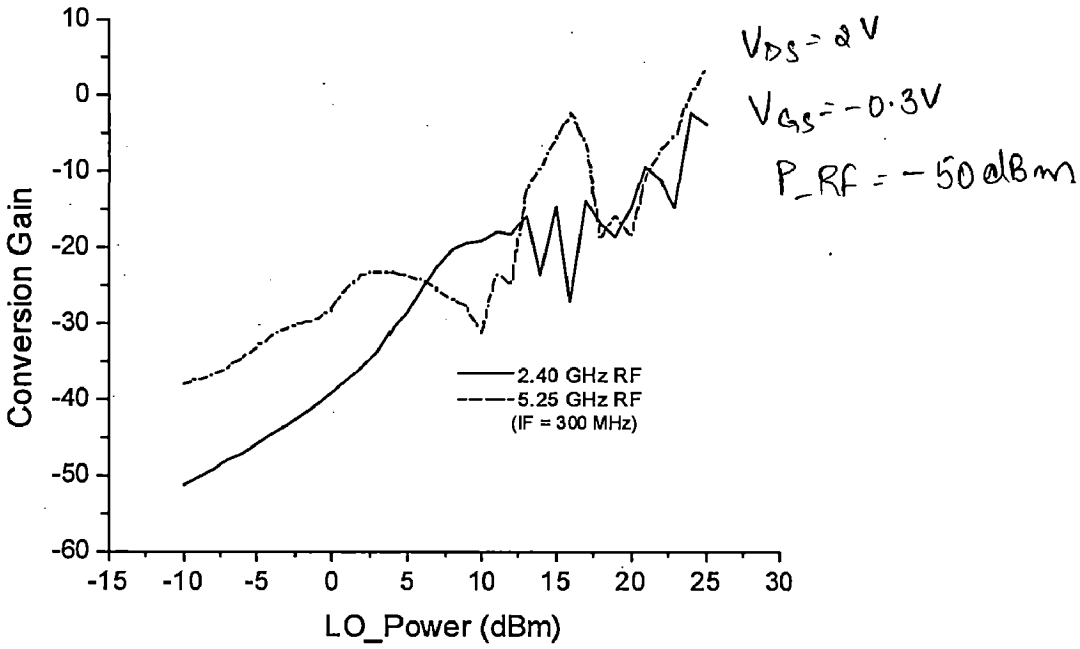
The defined component is available in the component library for use in schematic after this step. In the schematic window, the component is set up for HB analysis.

The lumped components i.e. 100 Ω bias resistor, 70 pF capacitor at the output IF side have been paced at their respective positions as they would be in the fabricated circuit.

The active device i.e. the FET and the bias voltage supplies have also been connected along with the ground connections. The circuit is simulated twice for 2.4 GHz and 5.25 GHz. The results obtained are shown in fig.4.17.



(a)



(b)

Fig.4.17: (a) CG vs RF power (b) CG vs LO power obtained after co-simulation of the wideband mixer

4.1.8 Fabrication and Measurement

The wideband architecture mixer for IF=300 MHz has been fabricated and tested using the spectrum analyzer. The bias network is changed to a self-bias circuit for obtaining the designed current. For,

$V_{DS} = 2V$, $I_D = 10$ mA , R_G (Gate Resistor) = 2.2 kΩ, $V_{DD} = 5V$

$$V_{GS} = -I_G R_S \tag{4.3}$$

$$V_{DD} - I_D R_S - V_{DS} - I_D R_S = 0 \tag{4.4}$$

Using (4.3) and (4.4), $R_S = 45\Omega$ and $R_D = 225\ \Omega$.

The design was implemented in microstrip and the fabricated circuit is shown below:

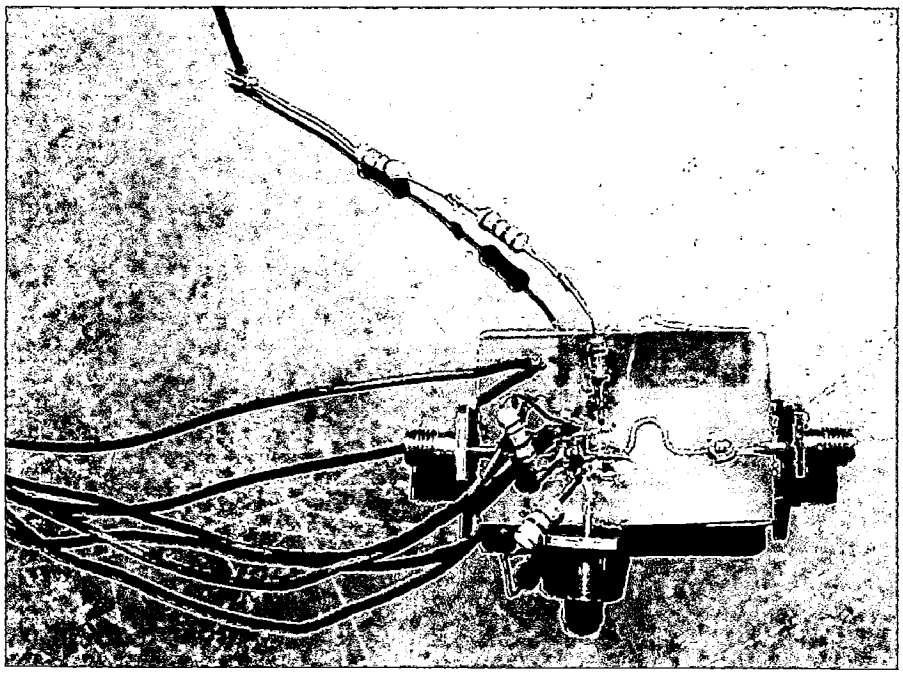


Fig. 4.18: Fabricated Wideband architecture for IF=300 MHz

The mixer has been tested using a spectrum analyzer and the setup is shown in fig.4.19. The spectrum is similar in the entire operating frequency range i.e. 2-6 GHz.

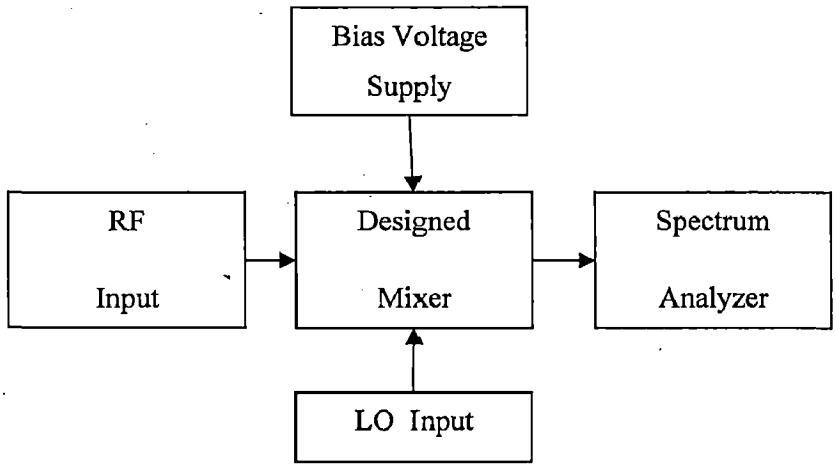


Fig.4.19: Test setup for wideband mixer

The circuit also caters for a minor shift in the incoming RF frequency as the IF is still detected at 295 MHz and 305 MHz as well. Though an IF is detectable in the spectrum, the power obtained at the output shows a conversion loss instead of a conversion gain. The reason for this is the fabrication error introduced. An error in the following dimensions of the circuit has been detected in the actual fabricated mixer.

Table 4.10: Fabrication errors of wideband mixer

Characteristic Impedance of Line (Ohms)	Desired Dimensions		Actual Dimensions	
	Width, W (mm)	Length, L (mm)	Width, W_o (mm)	Length, L_o (mm)
50	0.784	5	1.2	5
100 (L = 1.67 nH)	0.204	3.983	0.5	3.5
30 (C = 0.583 pF)	1.558	3.533	2	4
90 (L = 8.28 nH)	0.264	19.480	0.5	18
90 (L = 3.90 nH)	0.264	9.833	0.5	9

Also, a few changes have been made in the matching network at the output side (at 300 MHz) due to the unavailability of the components' values used and the fabrication limitations.

- The interdigital capacitor of value 2.32 pF used during design and simulation on the output side has been replaced with a parallel combination of two chip capacitors each of value 1 pF. Therefore, an equivalent of 2 pF has been used instead of the desired 2.32 pF.

- The 70 pF shunt capacitor has been replaced by an equivalent of 69 pF using chip capacitors.

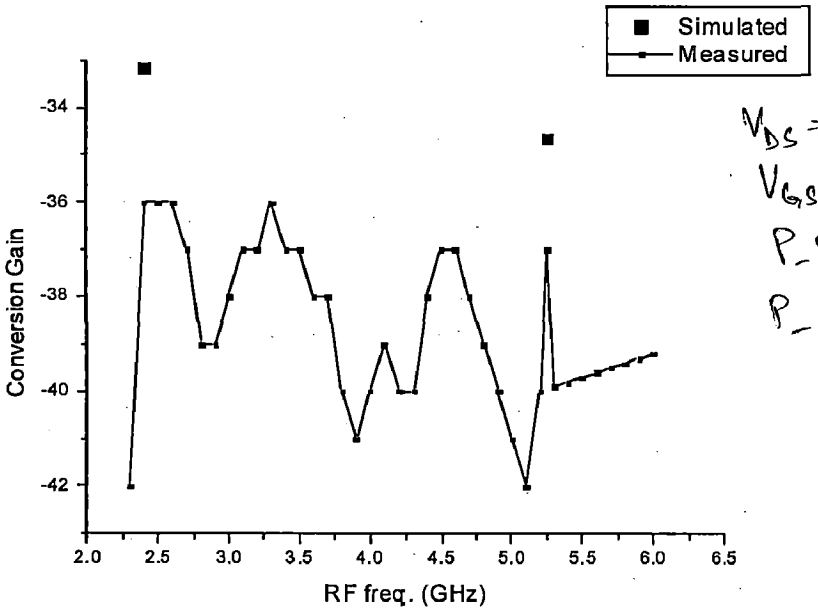
Apart from this, changes in the widths of lines at various interconnect lines and tapered lines have been observed. Table 4.11 though shows a marked decrease in the CG of when non-linear analysis is completed, it still exhibits the required dual band behavior. The performance deterioration is explained by the fact that ideal components have been replaced by practical ones and also, conductor losses had not been taken into account during circuit simulation.

Table 4.11(a): Comparison of Non-linear full wave analysis and circuit simulation of wideband architecture (IF=300 MHz)

Parameters	Non-linear analysis		Circuit Simulation	
	2.4 GHz RF	5.25 GHz RF	2.4 GHz RF	5.25 GHz RF
CG	-3.971	3.419	6.372	12.059
NF	9.779	11.733	7.544	11.930

Table 4.11(b): Comparison of measurement and simulation (errors included) results

Parameters	Non-linear analysis		Measurement	
	2.4 GHz RF	5.25 GHz RF	2.4 GHz RF	5.25 GHz RF
CG	-33.157	-34.633	-41	-42



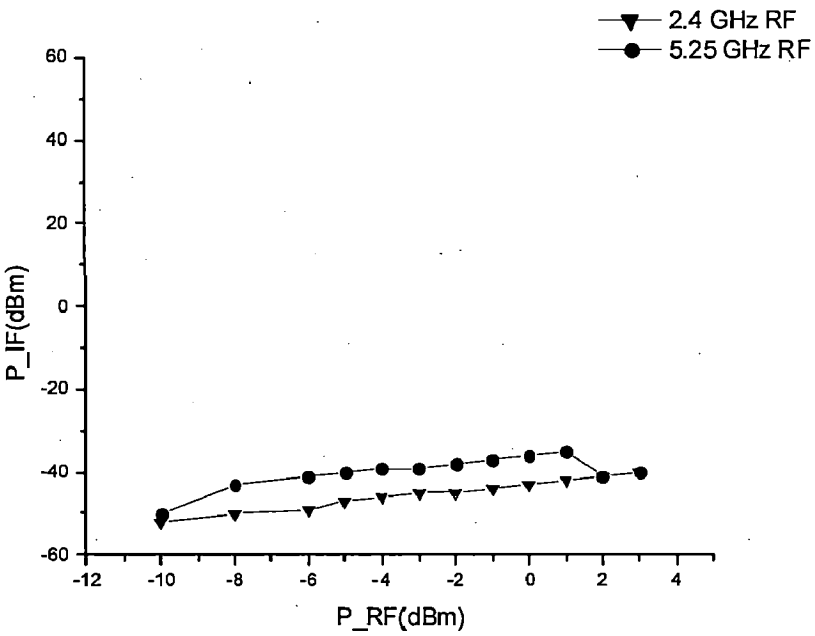
$V_{DS} = 2\ V$

$V_{GS} = -0.3V$

$P\_RF = -5\ dBm$

$P\_LO = 5\ dBm.$

(a)

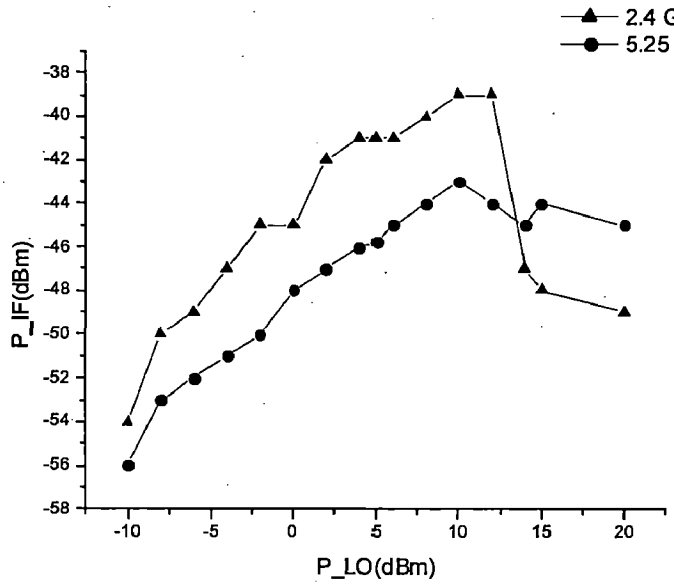


$V_{DS} = 2V$

$V_{GS} = -0.3V$

$P\_LO = 5\ dBm$

(b)



$V_{DS} = 2V$

$V_{GS} = -0.3V$

$P_{RF} = -5dBm$

(c)

Fig.4.20: (a) Simulated (with errors) and measured results (b) Output power vs RF power (c) Output Power vs LO power

It can be seen from the graph that the output power decreases beyond a certain limit of applied LO power. This is due to the mixer getting saturated due to which the gain decreases. The measured results show good agreement with the simulated results when the errors are included. Thus, the desired performance may be obtained if the fabrication errors are minimized.

4.2 Parallel Architecture

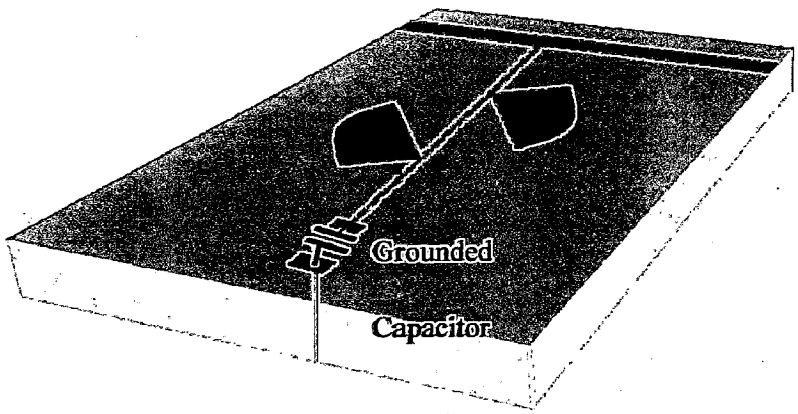
In this architecture, each individual matching network is designed and optimized separately for optimal performance. Each matching network is narrowband and operates only at one incoming RF frequencies. There is a separate parallel path for 2.4 GHz and 5.25 GHz. Each path has a separate transistor to perform mixing operation. The advantage of this architecture is optimal performance at each individual frequency. The matching can be done using the conventional method using the Smith Chart to obtain transmission line matching or lumped element matching networks. Lumped element networks are preferred as they occupy lesser area as compared to transmission line networks.

4.2.1 DC Analysis

DC analysis is similar as in the previous section and the operating point chosen is also the same as in the wideband case.

4.2.2 Bias Network Design

The bias network design was begun with the microstrip implemented bias circuit similar to the one shown in fig.3.5. The bias networks designed for 2.4 GHz and 5.25 GHz bias networks, their dimensions and their simulation results are shown in fig.4.21 and 4.22 respectively.



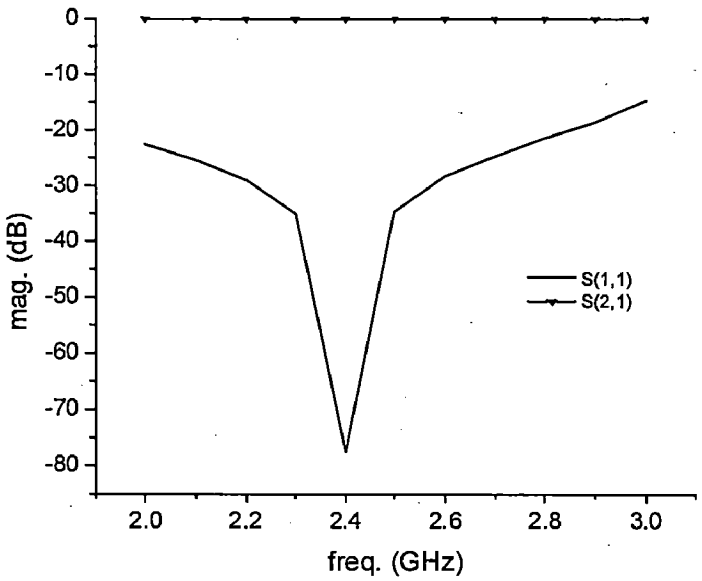
(a)

Table 4.12 (a): Line dimensions of 2.4 GHz Bias network

Z_0 (Ohms)	W (mm)	L (mm)
50	0.759	2.5(arbitrary)
100	0.204023	23.7634

Table 4.12 (b): Radial stub dimensions in 2.4 GHz bias network (post tuning)

α (degrees)	r_1 (mm)	r_2 (mm)
66	0.8	13.9272



(b)

Fig.4.21: 2.4 GHz (a) Bias network (b) S_{11} and S_{21} of the bias network

Similarly, the bias network for 5.25 GHz is designed. The dimensions of the bias network and measured S-parameters are shown in table 4.13.

The bias network designed is similar to the one shown in fig.4.21 except for the dimensions.

Table 4.13 (a) : Line dimensions of 5.25 GHz bias network

Z_0 (Ohms)	W (mm)	L (mm)
50	0.759	2.5(arbitrary)
100	0.204018	10.8604

Table 4.13 (b): Radial stub dimensions in 5.25 GHz bias network (post tuning)

α (degrees)	r_1 (mm)	r_2 (mm)
66	0.3	6.92716

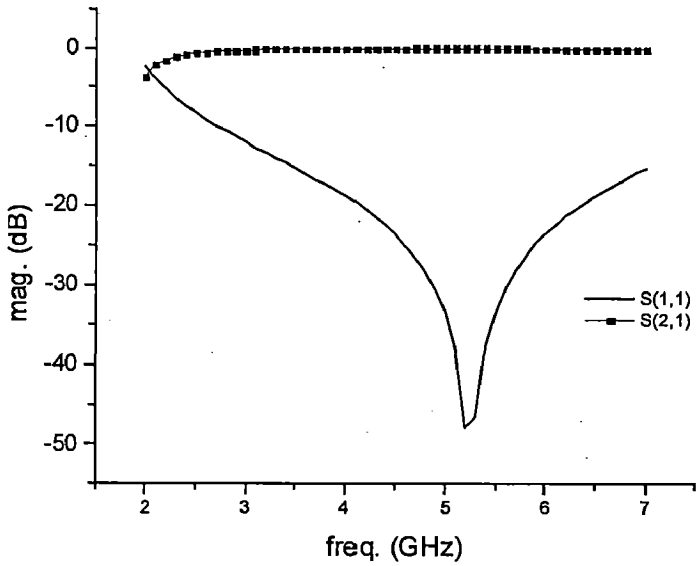


Fig.4.22: 5.25 GHz bias network simulation plots of S_{11} and S_{21}

4.2.3 Stability Analysis

This network did not provide stability to the transistor. Therefore, a similar approach as described in the previous section was adopted to stabilize the transistor at the chosen operating point i.e. a shunt resistor was added to make the circuit stable.

4.2.4 Impedance measurement and Matching Networks Design

The next step is to design the matching networks at the input and output. To measure the input and output impedances for matching, short circuit the IF at the RF input side and the RF/LO at the output side as explained in the previous chapter. Impedance measured is shown in table 4.14.

Table 4.14: Impedance measurement values at RF and IF

Freq. (GHz)	Impedance at RF port (Ohms)	Impedance at IF port (Ohms)
0.3	0.990 – j 3.561e-4	859.830 – j 285.918
2.4	83.250 – j 21.251	1.0 – j 0.003
5.25	63.811 - j 33.985	0.999 - j 0.006

Matching network at the input and output is designed to match the RF impedance and the IF impedance shown in table 4.14 to the 50 Ω input and output lines.

The mixer for 2.4 GHz with input and output matching networks is:

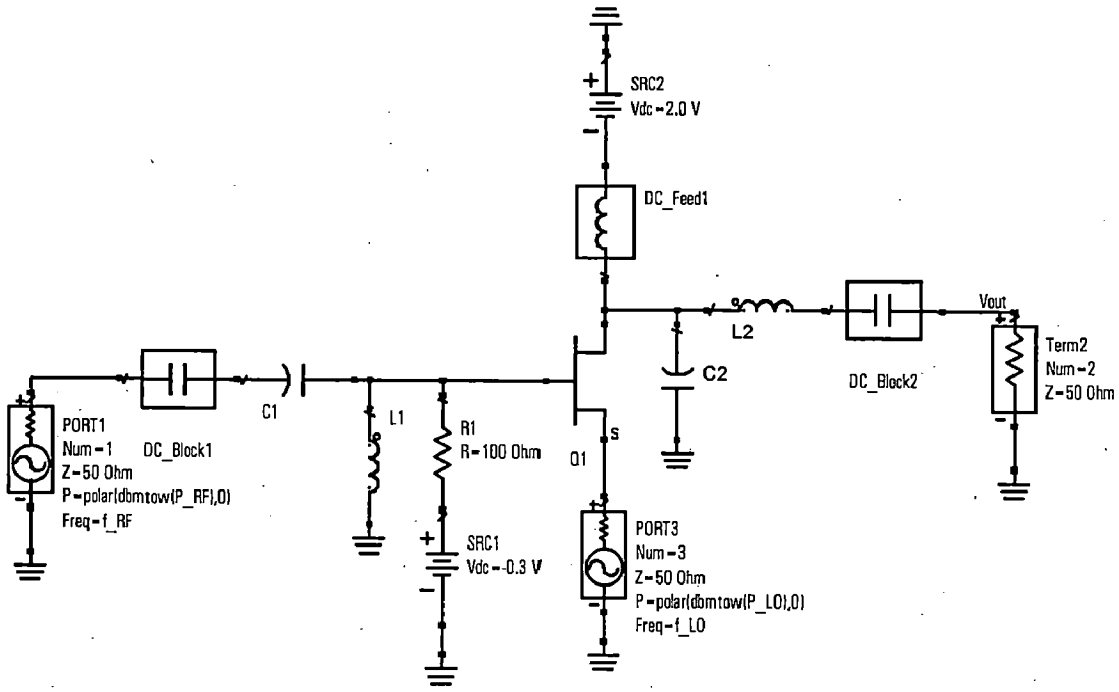


Fig.4.23: 2.4 GHz mixer with input and output matching networks

The values of the L-C matching network at the input and output are given below in table 4.15.On the input side:

Table 4.15 (a): Input Impedance matching network component values of the 2.4 GHz mixer

Component	Component name	Value
Series C	C1	1.51 pF
Shunt L	L1	5.18 nH

On the output side:

Table 4.15 (b) : Output Impedance matching network component values of the 2.4 GHz mixer

Component	Component name	Value
Shunt C	C2	2.55 pF
Series L	L2	112.85 nH

The HB analysis results are shown in fig.4.25.

The 5.25 GHz mixer is designed in a similar manner. The 5.25 GHz mixer with the input and output impedance matching networks is as shown in fig.4.24

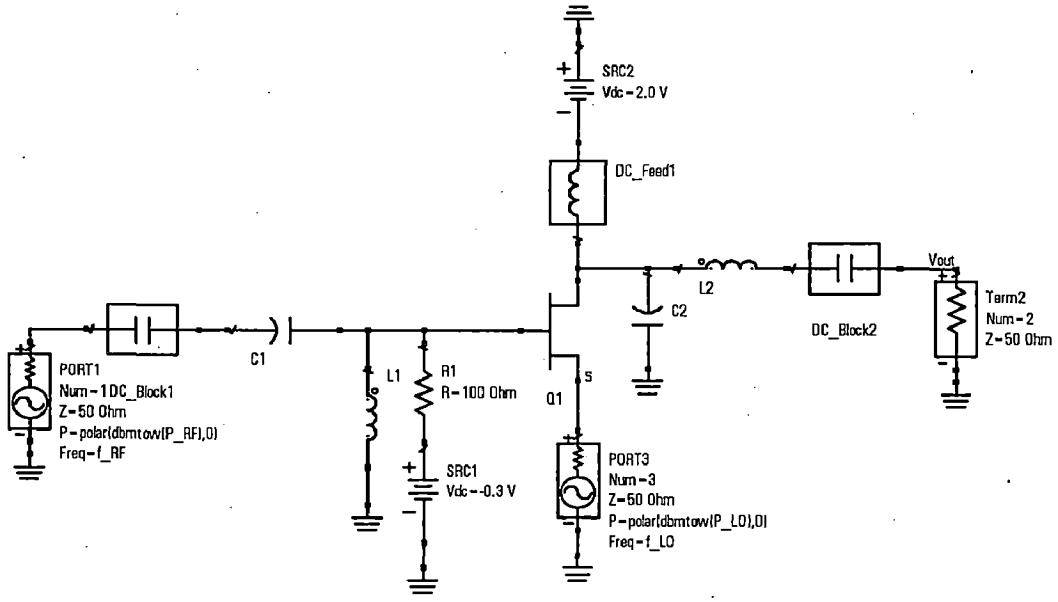


Fig.4.24 : 5.25 GHz mixer with input and output matching networks

Table 4.16 (a): Input Impedance matching network component values of the 5.25 GHz mixer

Component	Value
Series C	0.759 pF
Shunt L	1.86 nH

Since the IF is the same 300 MHz, the output matching network is the same as for 2.4 GHz mixer and is repeated here for convenience.

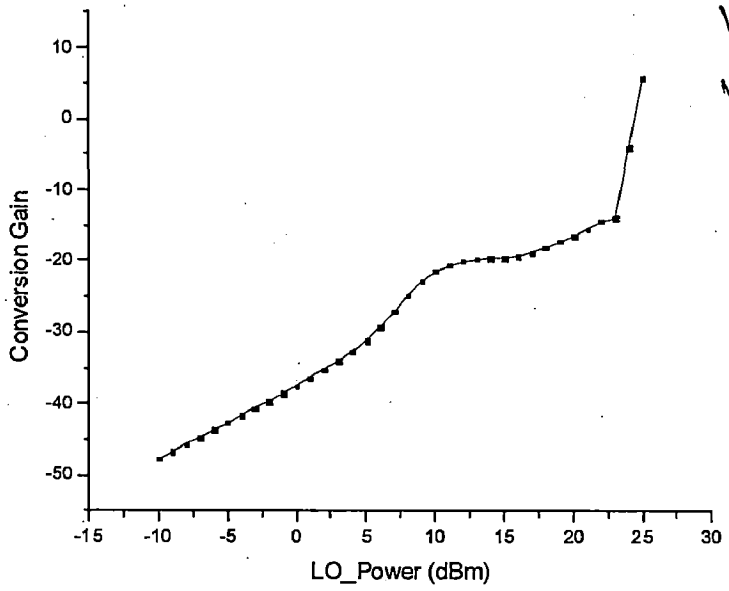
Table 4.16 (b) : Output Impedance matching network component values of the 5.25 GHz mixer

Component	Value
Shunt C	2.55 pF
Series L	112.85 nH

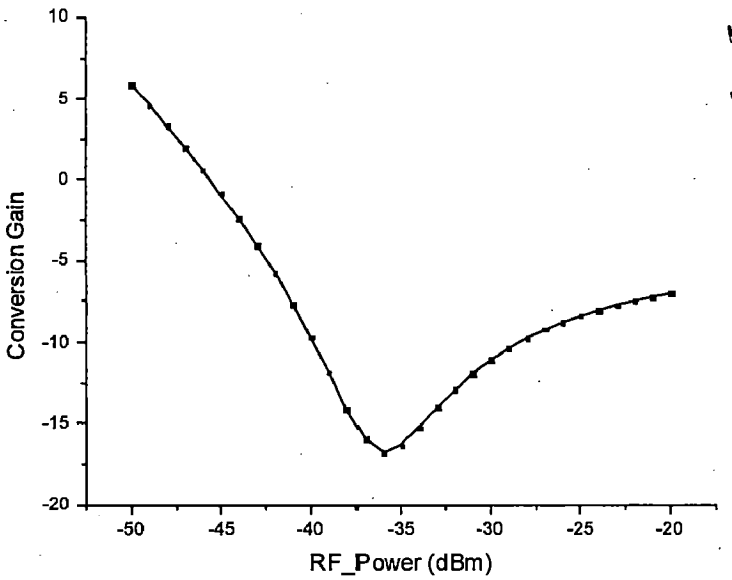
The HB analysis results are shown in fig.4.26.

4.2.5 HB analysis of 2.4 GHz and 5.25 GHz mixers

The HB analysis results of the 2.4 GHz mixer are shown in fig.4.25.



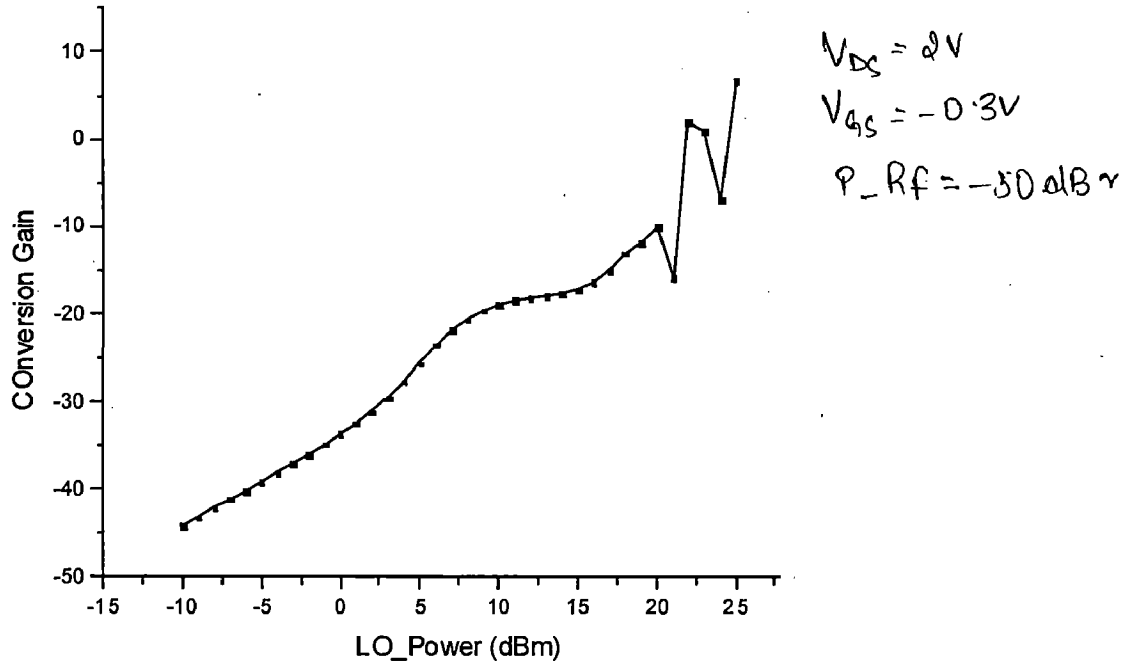
(a)



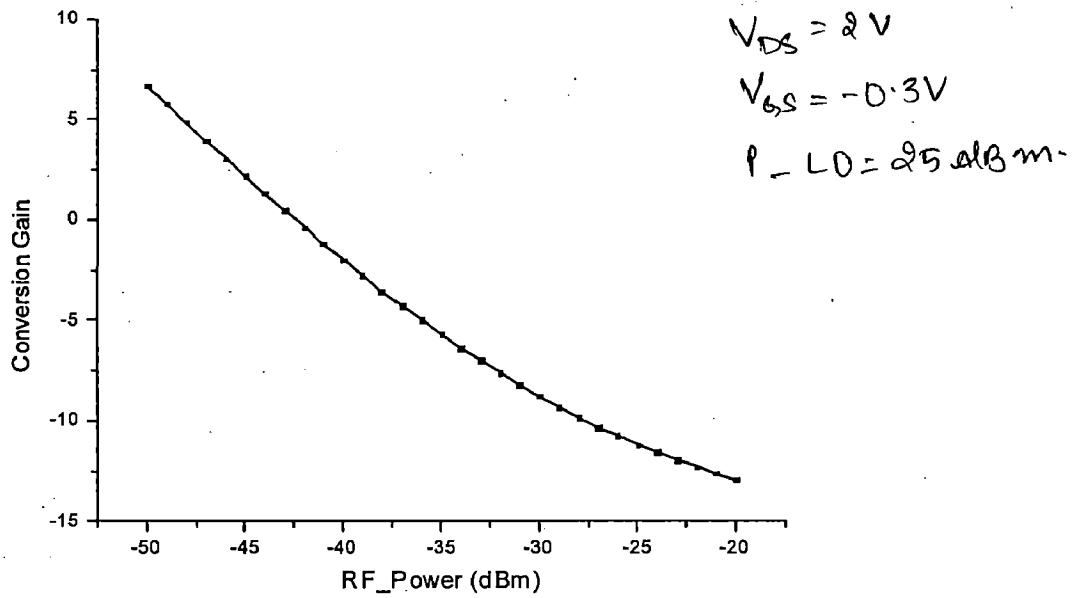
(b)

Fig.4.25: (a) Conversion gain vs LO power (b) Conversion gain vs RF power from HB simulation of 2.4 GHz mixer

The HB analysis results of the 5.25 GHz mixer are shown in fig.4.26.



(a)



(b)

Fig.4.26: (a) Conversion gain vs LO power (b) Conversion gain vs RF power from HB simulation of 5.25 GHz mixer

4.2.6 Combining 2.4 GHz and 5.2 GHz mixer output

The final step is to combine the output IF paths using a Power combiner at the output. This will complete the parallel architecture design. The output path is combines using a WPD with a centre frequency of 300 MHz. The schematic of the parallel architecture mixer is shown in fig.4.27.

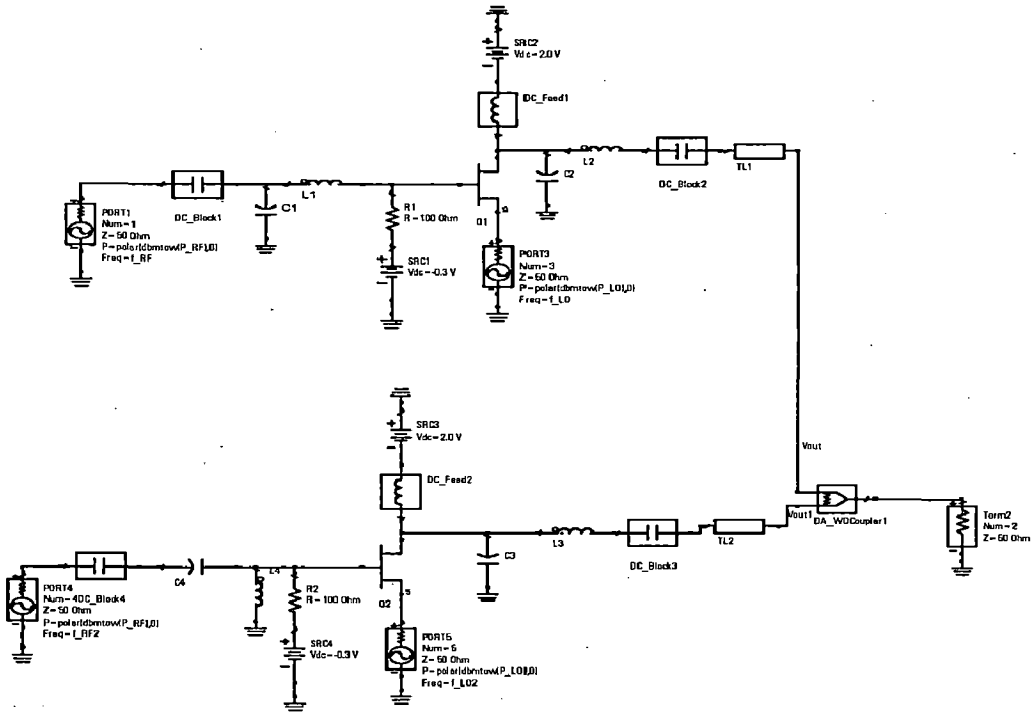


Fig.4.27: Parallel architecture mixer containing 2.4 GHz and 5.25 GHz mixer with a combiner

4.2.7 HB Analysis of Parallel Architecture

The HB analysis results for the complete parallel architecture are shown in table 4.6.

The comparisons of HB analysis reveal a similarity between the results of simulation of an individual mixer and that of a parallel architecture when the output paths at the IF are combined. The results are tabulated in table4.17:

Table 4.17: Comparison of the performance of the individual mixers and the combined parallel architecture

Parameter	Individual Mixers		Combined Parallel Architecture	
	2.4 GHz RF	5.25 GHz RF	2.4 GHz RF	5.25 GHz RF
CG	5.860	6.595	5.826	5.8
NF	8.035	8.25	6.681	10.354

Table 4.17 shows only a slight degradation of the NF at 2.4 GHz RF input and a slight decrease in the output at 5.25 GHz RF input in the parallel architecture. The NF at 5.25 GHz RF input is however, better than in the case of an individual mixer designed at 5.25 GHz. Therefore, a parallel architecture can be used to design a dual band mixer theoretically, but a large WPD required at the output prevents its practical realizability. The WPD designed at 300 MHz has approximately 1500 mm^2 of area and hence, this architecture is rarely used.

4.3 Conclusion

A wideband mixer has been designed and implemented in microstrip for 300 MHz IF. The same mixer has been designed for 140 MHz but not implemented due to practical constraints. A parallel architecture has also been discussed and simulated but not designed due to area constraints.

Chapter 5

Conclusion and future scope

Dual band performance has been obtained from RFICs. The performance has been found to be within the acceptable levels. All the desired results have been plotted and the plots have been presented throughout the report, which represent the operation of the circuits designed. References used have been added at the end to clarify the report further.

The future scope of development of the dissertation may include the design and development of more passive dual band components like filters and couplers. The design domain may be expanded further by using a dual gate FET or a differential transistor pair like a Gilbert Cell for the development of the dual band mixers.

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