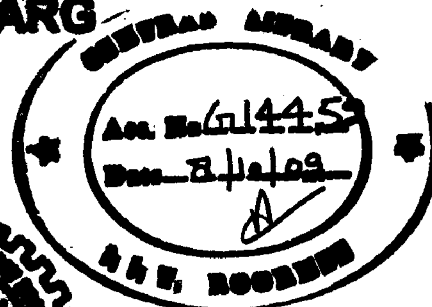
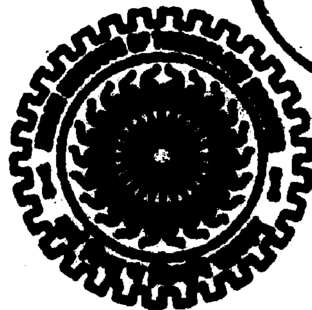
ANALYTICAL MODELING OF DGMOSFET USING GREEN's FUNCTION TECHNIQUE

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree
of
MASTER OF TECHNOLOGY
in
ELECTRONICS AND COMMUNICATION ENGINEERING
(With Specialization in Semiconductor Devices & VLSI Technology)

By
ANOOP GARG





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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation report, entitled **"Analytical Modeling of DOUBLE GATE MOSFET Using GREEN's Function Technique"**, is being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Semiconductor Devices and VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work, carried out from June 2008 to June 2009, under guidance and supervision of **Dr. S.N.Sinha**, Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not submitted for the award of any other Degree or Diploma.

Date:

Place: Roorkee

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CERTIFICATE

This is to certify that the statement made by the candidate is correct to best of my knowledge and belief.

Dr. S.N. Sinha

Professor

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I wish to express my sincere gratitude to my supervisor Dr. S.N.Sinha for his invaluable guidance and advice during every stage of this endeavor. I am greatly indebted to him for his continuing encouragement and support without which, it would not have been possible for me to complete this undertaking successfully. His insightful comments and suggestions have continually helped me to improve my understanding.

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Anoop garg

M.Tech.(S.D.V.T.)

ABSTRACT

Silicon-on-insulator (SOI) technology has been receiving a lot of attention owing to its advantages in reduced second-order effects for VLSI applications. It has been the forerunner of the CMOS technology in the last decade offering superior CMOS devices with higher speed, higher density and excellent radiation hardness. Many novel device structures have been reported in literature to address the challenge of short-channel effects (SCE) and higher performance for deep submicron VLSI integration.

Double Gate (DG) MOSFETs using lightly doped ultra thin layers seem to be another very promising option for ultimate scaling of CMOS technology. Excellent short-channel effect immunity, high transconductance and ideal subthreshold factor have been reported by many theoretical and experimental studies on this device.

We have proposed a two dimensional analytical model for the modeling of DG-MOSFET's using Green's functions. An analytical model using Poisson's equation also has been presented for the potential distribution and threshold voltage model for the DG-MOSFET. The results are compared with existing model results.

In this thesis, an analytical solution for the potential distribution of the two dimensional Poisson's equation with the dirichlet boundary condition has been obtained for the DGMOSFET device by Green's function technique. Based on the calculated potential distribution, the minimum surface potential of the DGMOSFET is determined. From the calculated minimum surface potential, the threshold voltage of the DGMOSFET is determined. It has been verified that the dependence of the calculated threshold voltage, surface potential and potential distribution on device channel length, gate oxide thickness, channel doping concentration, drain and gate biases with previous model results. This general solution of electrostatic potential distribution is uniquely determined by the given dirichlet boundary condition along the rectangular region. It can deal with any arbitrary doping profile.

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LIST OF PARAMETERS

C_{ox}	oxide capacitance per unit area
C_{si}	capacitance of silicon film
ε_{ox}	permittivity of oxide
ε_{si}	permittivity of silicon
t_{ox}	thickness of oxide
t_{si}	thickness of silicon body
f(y)	doping profile in channel region
N_A	acceptor concentration in the body
V_{gs}	Gate voltage
V_{ds}	Drain voltage
V_{gb}	applied voltage between gate and body
V_{sb}	applied voltage between source and body
V_{bi}	Built in Potential
V_{th}	threshold voltage
V_{fb}	flat band voltage
Φ_f	Fermi potential
Ψ_s, Φ_s	surface potential
E	electric field
L	Channel Length
q	electron charge
n_i	intrinsic concentration of Si
μ	Mobility of carrier

CHAPTER 1

INTRODUCTION

1.1 Background

In this background, we will be first presenting an overview of the Double Gate MOSFET structure which gives a basic understanding of the unconventional device. Later, we will present an overview of the general analytical modeling procedure.

1.1.1 Overview of Double Gate-MOSFET

In conventional single Gate bulk-Si microcircuits, the active elements are located in a thin surface layer (less than 0.5 μm of thickness) and are isolated from the silicon body with a depletion layer of a P-N junction. The leakage current of this P-N junction exponentially increases with temperature and is responsible for several serious reliability problems. Excessive leakage currents and high power dissipation limits operation of the microcircuits at high temperatures. Double –Gate MOSFETs technology employs Two Gate and a thin layer of silicon (tens of nanometers) isolated from a silicon substrate by a relatively thick (nanometers) layer of silicon oxide. DG MOSFET was proposed in the early 1980s. Double-Gate MOSFETs have been regarded as the most promising candidate for ultimate MOSFET scaling due to their excellent Short Channel MOSFET (SCE) immunity [1]. It can be scaled to the shortest channel length possible for a given gate oxide thickness.

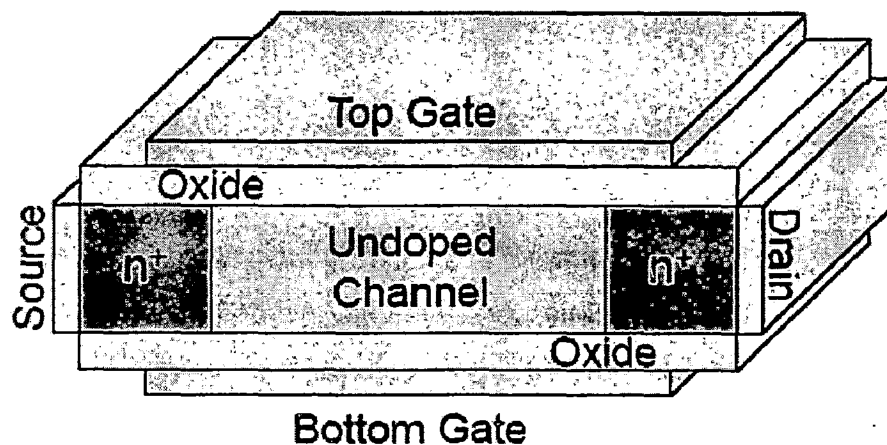


Figure1.1: Double gate MOSFET

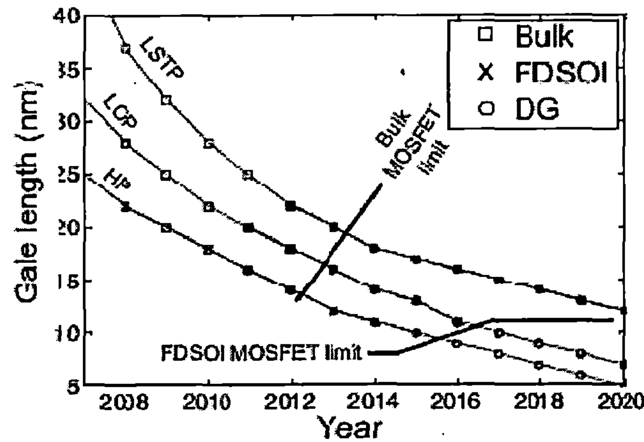


Figure.1.2: Evolution of gate length predicted by the 2005 ITRS For high-performance (HP), low operating power (LOP), and low standby power (LSTP) digital circuits [2].

Depending on the doping of the silicon layer, DG-MOSFETs will operate doped or undoped (lightly doped). The advantage advocated for DGMOSFETs include: ideal 60mv/decade subthreshold slope; volume inversion (for symmetric DGMOSFETs)[3];setting of threshold voltage by the gate work function thus avoiding dopant and associated Number fluctuation effects etc. However, with the reduction of channel length, control of Short-channel effects is one of the biggest challenges in further down-scaling of the Technology. The predominating short-channel effects are a lack of pinch-off and a shift in Threshold voltage with decreasing channel length as well as drain induced barrier lowering (DIBL) and hot-carrier effect at increasing drain voltage. However, the thin-film thickness has to reduce to the order of 10 nm to significantly improve the device performance, which becomes prohibitively difficult to manufacture and causes large device external resistance due to shallow source/drain extension (SDE) depths.

In a symmetric DGMOSFETs both gate material, oxide thickness, work function and applied Gate voltages are same and in asymmetric DGMOSFETs all things are different.

Figure.1.3: Symmetric Double Gate MOSFET

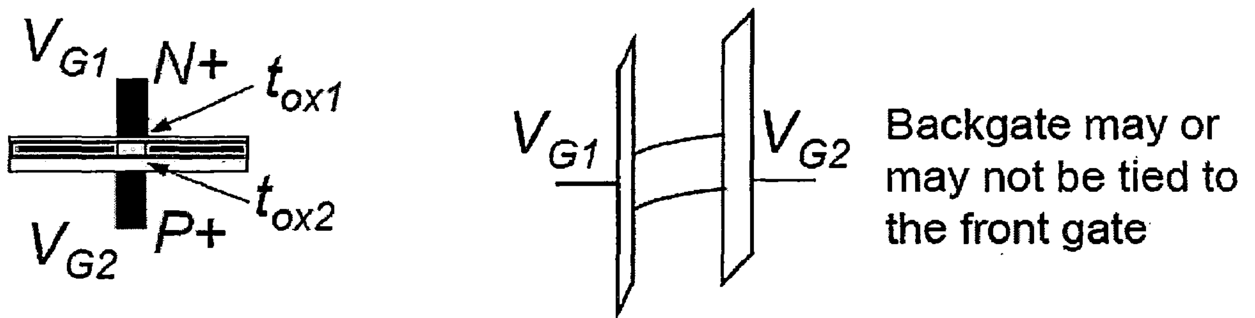


Figure.1.4: Asymmetric Double Gate MOSFET

The aim of this work is, therefore, to study the potential benefits offered by the DGMOSFETs in suppressing the short-channel effects in undoped DGMOSFETs using two-dimensional modeling and numerical simulation. The effects of varying device parameters can easily be investigated using the simple models presented in this work. There are three types of DGMOSFET structures which are commonly used: these are briefly described in the following sections.

Planar type:

The structure of planer type DGMOSFET is shown in fig.1.5. In this structure fabrication is more difficult in comparison with two other structures. This device is also known Self Align Double Gate MOSFET. A DG configuration with the two gates electrically separated is necessary for some applications such as dynamic threshold voltage control. For this, a relatively simple self aligned electrically separable double gate MOS transistor technology is best.

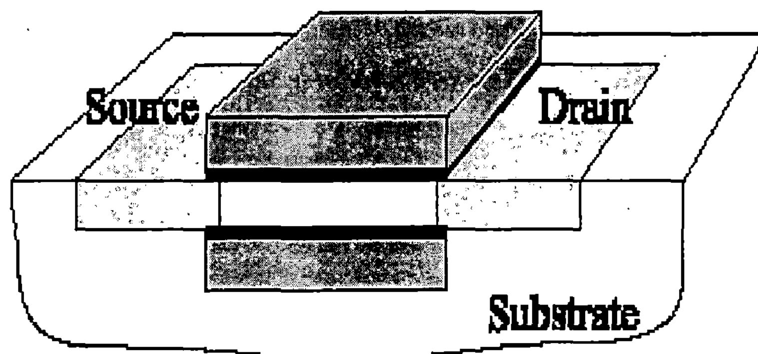


Figure.1.5: Planar Double-Gate MOSFET [4].

Advantages of planar type are:

1. Better uniformity of silicon channel thickness.
2. Can take advantages of existing fabrication processes.

Disadvantages of planar type are:

1. Fabrication of back gate and gate dielectric underneath the silicon channel is difficult.
2. Accessing bottom gate for device wiring is not easy.

Fin type:

In Fin type double-gate MOSFET is one of the most attractive alternative to classical MOSFET structure for gate length down to 20nm. The main advantage of the FinFET is its ability to drastically reduce the short channel effect. Inspite of its double-gate structure, the FinFET is closed to its root, the conventional MOSFET, in layout and fabrication, the basic principles and to uncover several important aspects: evaluation of the length, width and quantum effects.

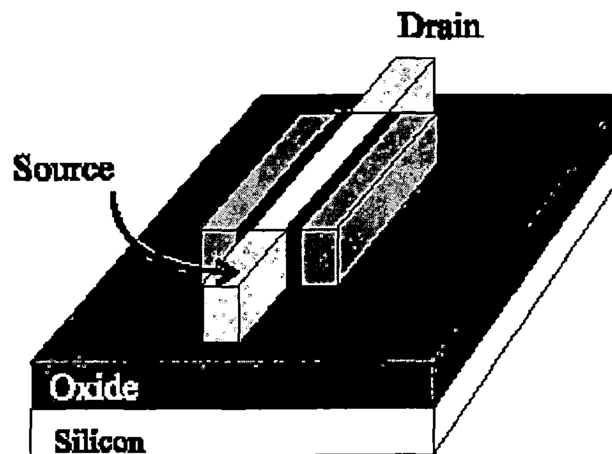


Figure.1.6: Fin type Double gate MOSFET [4].

Advantages of the Fin type structure are:

1. A transistor is formed in a vertical ultra –thin Si fin and is controlled by double-gate,which considerably reduces short channel effects.
2. The two gates are self aligned and are aligned to Source/Drain.
3. Source/Drain is raised to reduce the access resistance.

4. Up to date gate process: low temperature, high -k dielectrics can be used.
5. The structure is quasi-planar because Si Fin is relatively short.

Disadvantage of the Fin type structure are:

1. Low current due to parasitic effects.

Vertical type:

The third type is vertical type Double Gate MOSFET Like the FinFET, it has a silicon ridge of a few tenth of nanometers in thickness, which is the active area of the transistor. But in this case, the current flow is perpendicular to the surface. Here no SOI substrate is necessary and only one sub-100nm lithography to define the ridge is required. The channel length L_g is adjusted by ion implantation and diffusion. While earlier realization of this concept suffers from low current due to parasitic effects an optimized layout is presented, with reduced series resistances and improved doping profiles due to ion implantation.

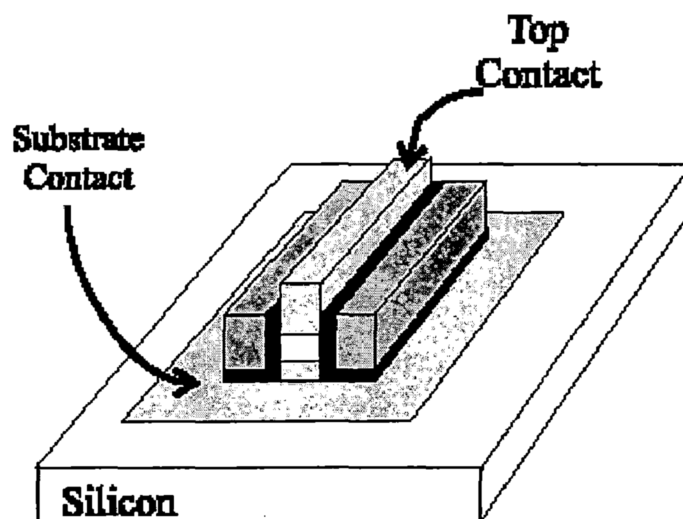


Figure.1.7: Vertical type Double Gate MOSFET [4]

Advantages of vertical type are:

1. No, silicon on insulator is necessary.
2. Transconductance, DIBL, Subthresold current improved.

1.1.2 Analytical Modeling Overview

An analytical model is a concise mathematical description of the complex device physics of the transistor. These models are convenient for use in fast circuit simulators, since they maintain a fine balance between the amount of detailed physics embedded for model accuracy and model compactness (computational efficiency). The simplifications in the physics enable very fast analysis of device/circuit behavior when compared to the much slower numerical based TCAD simulations. In an analytical model, the first step is to analyze the device behavior by looking at the embedded physics. It is also beneficial to examine the measured data from state-of-the-art devices which may reveal new physical phenomenon. The next step is to derive compact mathematical equations to capture the physics of the device. These equations may be verified against TCAD simulations for model accuracy and scalability. In a real device, quantities such as the doping profiles, junction depths, etc. are very complex. In order to precisely model the effect of quantities such as these, physics and technology related model parameters are added to the model. This forms a very important step in model formulation as the ultimate goal of a analytical model is to describe any given transistor technology accurately. The model parameters allow is to obtain a good description of technology by aiding in data fitting. Equally important is to develop a methodology to extract the value of these model parameters. A model without enough flexibility and without the ease of parameter extraction is virtually useless for real world circuit design. Once the model equations are ready, the next step is to examine the numerical robustness of the model. This may involve modifying some of the physics based equations to accelerate the model computation. The last step in model development cycle is verification against silicon data. The inability to adequately describe the measured data may require modification of the physics based equations and/or introduction of new model parameters. Successful description of silicon data over different geometry, bias and temperature marks the completion of model development. It is always preferable to verify the model against more than one technology, since the analytical model is a universal model which is not tied to any one specific technology.

Advantages of analytical models are:

1. The models are helpful in understanding the physics of the devices.

2. Computation efficiency and high accuracy.
3. Less percentage error in comparison to numerical modeling.
4. The model is particularly well suited for implementation in circuit simulators due to simple expressions for the equations.
5. This model allows for fast system level simulation of the nanoscale circuit.
6. The models are obtained by a simplification of the full physical model.

1.2 Review of Current Research

Due to the continuous scaling of MOS device channel length, short channel length effects are coming into picture. Due to high sensitivity of the electrical characteristics of short channel MOS devices to process fluctuations, it is becoming more difficult to achieve a high circuit performance with the designed device. But the problem can be solved by using an accurate device analysis. Since the last decade, two-dimensional numerical analysis has been used to investigate many device properties. Many models for different parameters of the device have been developed by various authors.

A two-dimensional (2-D) scaling-parameter dependent subthreshold swing model was developed for potential distribution in a SOI based DG-MOSFET by T.K.Chiang in [5]. Also an analytical potential model which provided an accurate description for partially and fully depleted MOSFET devices in different regions of operation was developed by Shih-Ching Loa et.al in [6]. A 2-D analytical solution of electrostatic potential was derived for undoped DG-MOSFETs in the subthreshold region by solving Poissons equation in a 2-D boundary value problem in [1] by Xiaoping Liang and Yuan Taur. A threshold voltage model for a Fully Depleted SOI based DG-MOSFET was presented by Hans van Meer and Kristin De Meyer in [7]. A short-channel threshold voltage model for an undoped symmetric DG-MOSFET was suggested by Qiang Chen et.al in [8] which included the use of mobile charge term in solving Poisons equations. A continuous analytic drain current model for double-gate (DG) MOSFETs was derived without the charge-sheet approximation by Yuan Taur et.al in [9]. All these models suffer from a drawback that they are valid only for a particular doping profile.

In this thesis, we have overcome this drawback by developing an analytical model for surface potential, potential distribution in Si film and threshold voltage of DG-MOSFET's by using Green's function. The results of this model are verified against

previous models. It should be noted that this model is developed and valid for uniform doping profile in Si film.

1.3. Problem Statement

In this dissertation, novel features offered by the introduction of a Green's function in DGMOSFETs are studied by means of two- dimensional analytical modeling. This is accomplished in terms of the following intermediate stages:

i) Develop a new 2-D analytical model for the potential distribution of symmetric DGMOSFETs using Green's function and verify it against previous model results.
ii) Threshold voltage model for symmetric DGMOSFETs is developed based on the surface potential model.

1.4 Thesis Organization

The dissertation is divided into five chapters and its outline is described as given below:

Chapter 1 discusses the fundamental concepts related to MOSFET's/DGMOSFETs devices. Analytical modeling - advantages & disadvantages, objectives of the project and outline of the thesis are presented here.

In Chapter 2, we present a basic review on how analytical modeling of a DG-MOSFET structure is performed. Two-Dimensional model for the surface potential variation along the channel, potential distribution along Si thickness (front gate to back Gate) and threshold voltage model of the undoped symmetric DGMOSFET are illustrated.

In Chapter 3, we propose a 2-D analytical model using Green's function method for the DGMOSFET structure. The surface potential along the channel, potential distribution along Si thickness (front gate to back Gate) and threshold voltage model are developed.

Chapter 4 presents the results of the proposed model and discuss about various effects on potential distribution, surface potential and threshold voltage model along with their accuracy. The performance of these models is compared with the existing analytical models.

Chapter 5 concludes this thesis.

CHAPTER 2

REVIEW OF ANALYTICAL MODELING OF DOUBLE GATE MOSFET's

2.1. Introduction

This chapter presents a review on the evolution of DG MOSFET modeling, where strengths and weaknesses of different models are discussed. At ultra deep sub-micron technology, where the gate length is around 60nm, there is an increase in the effective electric field at the drain end in a MOS device resulting in various short-channel effects like DIBL. Unconventional asymmetrical structures have been employed to reduce the drain side electric field and its consequent impact upon the channel. Double Gate MOSFET is a kind of these structures which can be employed to reduce short channel effects [1-11].

In a DG-MOSFET, there is an enhancement in the source side electric field which results in increased carrier transport efficiency in the channel region, thus leading to a suppression of short-channel effects. The unique structure of DG-MOSFET offers flexibility in choosing different values for thin-film thickness, channel doping and oxide thickness. The DG-MOSFET structure may of symmetric or asymmetric type depending on the work function (Metal-Semiconductor), gate oxide thickness, type of gate material and applied gate voltage [12].

Till now, two general approaches have been used to model the surface potential profile, the electric field pattern and their impact on the threshold voltage. One of these approaches is the two-dimensional (2-D) numerical simulation and the other approach presents an analytical solution by solving the Poisson's equation along the Silicon film (Si) [6]. One-dimensional analysis, based on Gradual Channel Approximation (GCA) fails to adequately characterize the devices with short channels and is suitable only for a long channel transistor where the "edge" effects along the sides of the channel can be neglected. In such an analysis, it is assumed that the gate side electric field lines are perpendicular to channel's length or have a component along the y-direction only. If the channel is short (i.e., L is not much larger than the sum of the source and drain depletion widths), a significant part of the electric field will have components along both the y and

x directions, the latter being the direction along the channel's length. Thus a two-dimensional analysis is needed.

A 2-D analytical model for fully depleted SOI using Green's function was presented by Hans at el. in [7, 10-11], which enables a fast-physics based analysis of the undoped symmetric DG-MOSFETs. The expressions for the surface potential and electric field under Poly-silicon gate have been derived in [5] and are briefly reviewed in this chapter.

2.2. DG-MOSFET Structure and its Parameters

Chiang[5] presented the structure of a symmetric DG-MOSFET as shown in Fig. 2.1 with poly-silicon gate whose length is given by 'L'.

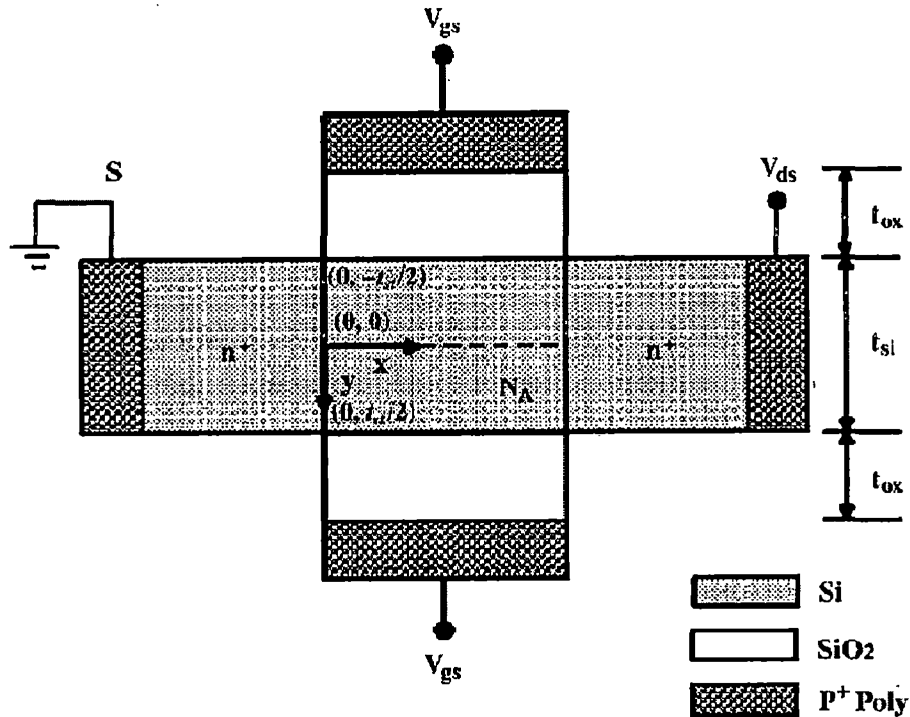


Figure 2.1: Cross-sectional view of an N-channel DG MOSFET [5]

The front and back gates are made of 'P^+' polysilicon. The figure shows the origin of the coordinate system with x-axis along the length of the channel and y-axis along the depth. The source/drain (S/D) regions are rectangular and uniformly doped at 4×10^{20} cm^{-3}. The channel doping concentration N_A is uniform at 1×10^{16} cm^{-3} typical values of the gate oxide thickness and the body-film thicknesses are 5nm and 20nm respectively.

2.3. Potential Models for the Analysis of DGMOSFET

In this section, we discuss two-dimensional potential analysis proposed by Chiang [5], threshold voltage model given by Yuan Taur and Chiang [1, 5] and drain current modeling by Yuan Taur [1].

2.3.1 Two-Dimensional Potential Analysis

In the model proposed by Chiang [5], the potential distribution along the Si thickness is assumed to be of parabolic type. Poisson's equation for potential $\Phi(x,y)$ in a fully depleted DG-MOSFET structure is given by:

$$\frac{\partial^2\Phi(x,y)}{\partial x^2}+\frac{\partial^2\Phi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{si}} \qquad 0\le x\le L \ ,0\le y\le t_{si} \tag{2.1}$$

where N_a is body concentration, ε_{si} is permittivity of Silicon dielectric constant, L is the device channel length and t_{si} is Silicon film thickness.

The parabolic potential profile in the vertical direction has been assumed to parabolic and is given by [5]:

$$\Phi(x,y)=C_1(x)+C_2(x)y+C_3(x)y^2 \tag{2.2}$$

The boundary conditions for the geometry in Fig.2.1 can be stated as follows:

(a) The central potential $\Phi_c(x)$ is a function of x only which is given as:

$$\Phi(x,y)=C_1(x)=\Phi_c(x) \tag{2.3}$$

(b) The electric field at $y=\frac{t_{si}}{2}$ is determined by the gate and the oxide thickness is shown to be:

$$\frac{\partial\Phi(x,y)}{\partial y}\Big|_{y=\frac{t_{si}}{2}}=-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(\Phi_s(x)-V_{gs}+V_{fb})}{t_{ox}} \tag{2.4}$$

Where V_{gs} and V_{fb} are the gate bias and flat band voltage, respectively.

(c) The electric field at $y=-\frac{t_{si}}{2}$ is the same as that at $y=\frac{t_{si}}{2}$ but opposite in sign which is given by:

$$\frac{\partial\Phi(x,y)}{\partial y}\Big|_{y=-\frac{t_{si}}{2}}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(\Phi_s(x)-V_{gs}+V_{fb})}{t_{ox}} \tag{2.5}$$

Where t_{ox} is the thickness of oxide. The surface potential used in (2.4) and (2.5) is of the form as shown below:

$$\Phi_s(x)=\Phi(x,y)\Big|_{y=\pm\frac{t_{si}}{2}}=\Phi_c(x)\pm C_2(x)\frac{t_{si}}{2}+C_3(x)\frac{{t_{si}}^2}{4} \tag{2.6}$$

Now, solving for values of constant functions, $C_2(x)$ and $C_3(x)$ using (2.4), (2.5) and (2.6), we get,

$$C_2(x) = 0$$

$$C_3(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{-\Phi_s + V_{gs} - V_{fb}}{t_{si}}$$

Substituting the above values into (2.6), we get the surface potential as:

$$\Phi_s(x) = \Phi_c(x) + \frac{t_{si}^2}{4} \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V_{gs} - V_{fb} - \Phi_s}{t_{si} t_{ox}} \tag{2.7}$$

Rearranging (2.7), we obtain:

$$\Phi_s(x) = \frac{\Phi_c(x) + \frac{t_{si}^2}{4} [\frac{\varepsilon_{ox}}{t_{si}\varepsilon_{si}} \frac{V_{gs} - V_{fb}}{t_{ox}}]}{1 + \frac{t_{si}^2}{4} \frac{\varepsilon_{ox}}{t_{ox} t_{si} \varepsilon_{si}}} \tag{2.8}$$

Since, $C_1(x)$, $C_2(x)$ and $C_3(x)$ are known, the 2D potential $\Phi(x, y)$ in (2.2) is given as:

$$\Phi(x, y) = \Phi_c(x) + \left[\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{-\Phi_s + V_{gs} - V_{fb}}{t_{si} t_{ox}} \right] y^2 \tag{2.9}$$

In (2.9), we need to substitute for y $= d_{eff}$(effective conducting path) which can be defined as the most leaky path for subthreshold conduction that exists between the surface where, y = $\pm\frac{t_{si}}{2}$ and the centre where y=0. The potential in this effective conducting path is given as:

$$\Phi_{d_{eff}}(x) = \Phi_c(x) + \left[\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{-\Phi_s + V_{gs} - V_{fb}}{t_{si} t_{ox}} \right] d_{eff}^2 \tag{2.10}$$

Combining (2.8) and (2.10), we get,

$$\Phi_s(x) = \frac{\Phi_{d_{eff}}(x) - A}{1 - A} \tag{2.11}$$

Where

$$A = d_{eff}^2 - \frac{t_{si}}{4} \frac{\varepsilon_{ox}}{t_{ox} \varepsilon_{si}} \tag{2.12}$$

and

$$\Phi_c(x) = \frac{\Phi_{d_{eff}}(x) - A}{1 - A} . (1 + B) - B(V_{gs} - V_{fb}) \tag{2.13}$$

Where

$$B = \frac{t_{si}}{4} \frac{\varepsilon_{ox}}{t_{ox} \varepsilon_{si}} \tag{2.14}$$

Using (2.13) and (2.11), we transform $\Phi(x,y)$ to the following expression in which the function $\Phi_{d_{eff}}(x)$ needs to be solved, for which a procedure has been laid out in [5].

$$\Phi(x,y) = \Phi_{d_{eff}}(x)\left(\frac{1+B-Cy^2}{1-A}\right) + \left(V_{gs}-V_{fb}\right)\left(Cy^2 + \frac{ACy^2}{1-A} - B - \frac{A(1+B)}{1-A}\right) \quad (2.15)$$

Where

$$C = \frac{\varepsilon_{ox}}{t_{si}t_{ox}\varepsilon_{si}} \quad (2.16)$$

Now the function, $\Phi_{d_{eff}}(x)$ needs to be solved. According to Chiang theory, the device needs to be designed for a large scaling factor (α_1) to suppress the short-channel effects which is given by:

$$\alpha_1 = \frac{L_g}{2\lambda_1} \quad (A)$$

Where λ_1 is the natural length which characterizes the short-channel effects and is given by:

$$\lambda_1 = \sqrt{\frac{t_{si}t_{ox}\varepsilon_{si}}{2\varepsilon_{ox}}}$$

The maximum potential at the centre of DG-MOSFET is more sensitive to gate length than that at its surface. Taking this factor into consideration, it was found that the scaling factor is of the same form as in (A) except that the Natural length $\lambda_1$is now modified as λ_2 which is given as:

$$\lambda_2 = \sqrt{\frac{t_{si}t_{ox}\varepsilon_{si}\left(1+\frac{t_{si}\varepsilon_{ox}}{4t_{ox}\varepsilon_{si}}\right)}{2\varepsilon_{ox}}}$$

Considering effective conduction mode, a simple equation for $\Phi_{d_{eff}}(x)$ is obtained by substituting (2.15) in (2.1) and setting y=d_{eff} instead of y=0 (bulk conduction mode) or $y = \pm\frac{t_{si}}{2}$ (surface conduction mode). It is now given as:

$$\frac{d^2\Phi_{d_{eff}}(x)}{dx} + \frac{V_{gs}-V_{fb}-\Phi_{d_{eff}}(x)}{\frac{1+B-C{d_{eff}}^2}{2C}} = \frac{qN_a}{\varepsilon_{si}}\frac{1-A}{1+B-C{d_{eff}}^2} \quad (2.17)$$

Eq.(2.17) is the key scaling equation in Chiang theory and the new modified natural length is given to be:

$$\lambda_3 = \sqrt{\frac{t_{si}t_{ox}\varepsilon_{si}\left(1 + \frac{t_{si}\varepsilon_{ox}}{4t_{ox}\varepsilon_{si}} - \frac{\varepsilon_{ox}}{t_{si}t_{ox}\varepsilon_{si}}d_{eff}{}^2\right)}{2\varepsilon_{ox}}}$$

Equation (2.17) is a second order one dimensional differential equation with respect to the potential of the effective conducting path, and it can be uniquely solved by specifying two boundary conditions that in the present case are the potential at the source (x=0) and the drain (x=L_g) which are given as:

$$\Phi_{d_{eff}}(x = 0) = v_{bi} \tag{2.18}$$

$$\Phi_{d_{eff}}(x = L_g) = v_{bi} + v_{ds} \tag{2.19}$$

Where v_{ds} is drain bias voltage and v_{bi} is the built-in voltage between the source/drain side and the silicon substrate.

Solving (2.17) using (2.18) and (2.19), we get the potential of the effective conducting path as:

$$\Phi_{d_{eff}}(x) = \frac{1}{\sinh\left(\frac{L_g}{\lambda_3}\right)}\left((v_{bi} + D)\sinh\left(\frac{L_g - x}{\lambda_3}\right) + (v_{bi} + v_{ds} + D)\sinh\left(\frac{x}{\lambda_3}\right)\right) - D \tag{2.20}$$

Where, D is given by:

$$D = \frac{qN_A}{\varepsilon_{si}}\frac{1 - A}{2C} - v_{gs} + v_{fb} \tag{2.21}$$

The subthreshold conduction causing the punch-through leakage current can be described by the minimum channel potential in the effective conducting path. The minimum potential of the channel can be calculated from (2.20) by solving

$$\frac{d\Phi_{d_{eff}}(x)}{dx}\Big|_{x=x_{min}} = 0 \tag{2.22}$$

Substituting in (2.22) for $\Phi_{d_{eff}}(x)$ from (2.20) we have:

$$x_{min} = \frac{1}{2}\lambda_3 \ln\left(\frac{P - Qexp\left(\frac{L_g}{\lambda_3}\right)}{Qexp\left(-\frac{L_g}{\lambda_3}\right) - P}\right) \tag{2.23}$$

Where

$$P = v_{bi} + v_{ds} + D \tag{2.24}$$

$$Q = v_{bi} + v_{ds} \tag{2.25}$$

According to (2.23) and (2.20), minimum potential $\Phi_{d_{eff,min}}$ with the effective conducting path, is too complex to use in deriving the subthreshold factor. For simplification of expression for $\Phi_{d_{eff,min}}$ the condition of $\frac{L_g}{\lambda_3}$ >>1 is used. The minimum potential and minimum position are now given as,

$$\Phi_{d_{eff,min}} \approx 2\sqrt{PQ}\exp\left(-\frac{L_g}{2\lambda_3}\right) - D \tag{2.26}$$

$$x_{min} \approx \frac{L_g}{2} + \frac{\lambda_3}{2}\ln\left(\frac{Q}{P}\right) \tag{2.27}$$

An expression for the electric field can be obtained by differentiating the surface potential expressions in (2.20) which is given as:

$$E_x = \frac{\partial \Phi_{d_{eff}}(x)}{\partial x}\Big|_{y=0}$$

$$= \frac{1}{\sinh\left(\frac{L_g}{\lambda_3}\right)}\left(-\frac{(v_{bi}+D)}{\lambda_3}\cosh\left(\frac{L_g - x}{\lambda_3}\right) + \frac{(v_{bi}+v_{ds}+D)}{\lambda_3}\cosh\left(\frac{x}{\lambda_3}\right)\right) - D \tag{2.28}$$

We note that if $v_{ds} \ll 1.0$V (this can be true for devices at subthreshold operation with a small drain bias), then $P \approx Q$, which results in $x_{min} \approx \frac{L_g}{2}$ and causes the leakage current to flow near to the middle of channel. Because the punch-through current at the subthreshold depends mainly on the potential difference between the minimum potential of the effective conducting path and that of the source, from the exponential term of (2.26), the effective conducting path- dependent scaling factor is chosen as

$$\alpha_3 = \frac{L_g}{2\lambda_3} \tag{2.29}$$

Fig.2.2 – Fig.2.4 show the potential distribution along Si thickness by varying different parameters viz., gate bias voltage, gate oxide thickness and channel doping concentration respectively. All these variations are of parabolic nature.

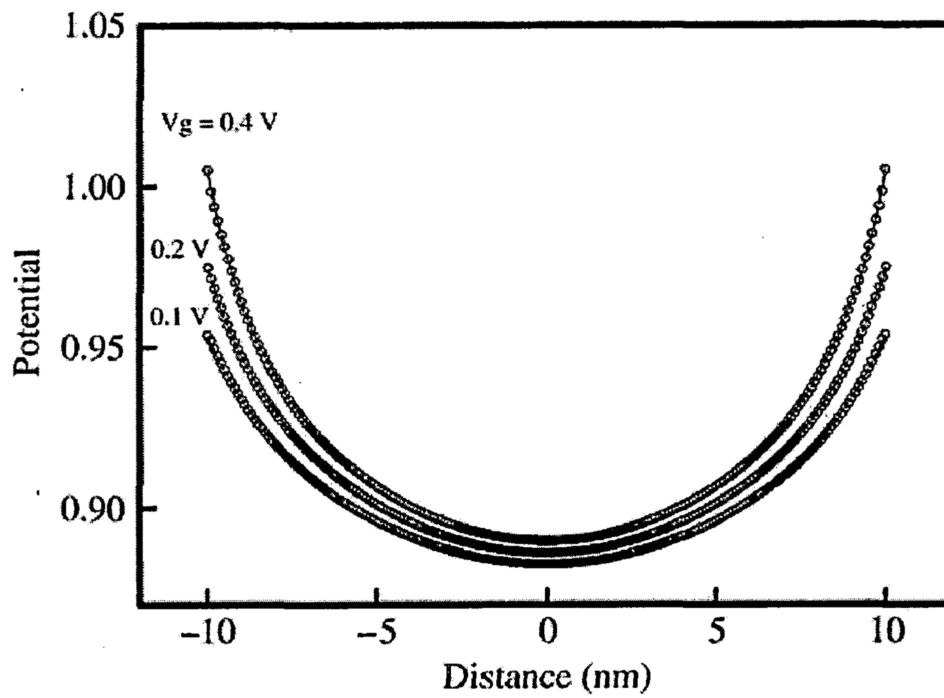


Figure 2.2: Variation of potential distribution along Si thickness with different Gate bias voltage in DGMOSFETs [6]

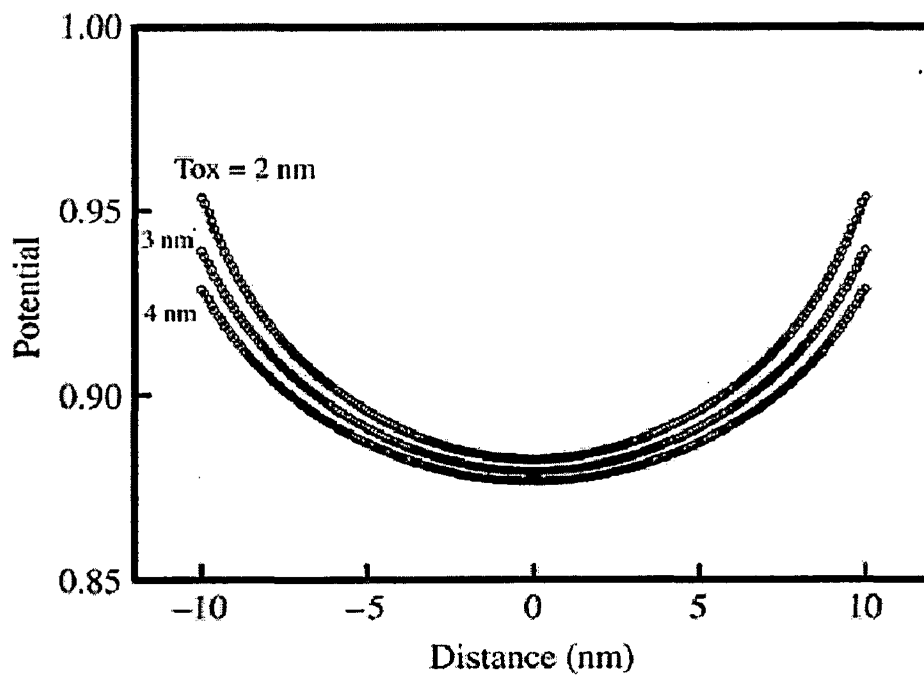


Figure.2.3: Variation of potential distribution along Si thickness with different Gate oxide thickness in DGMOSFETs [6]

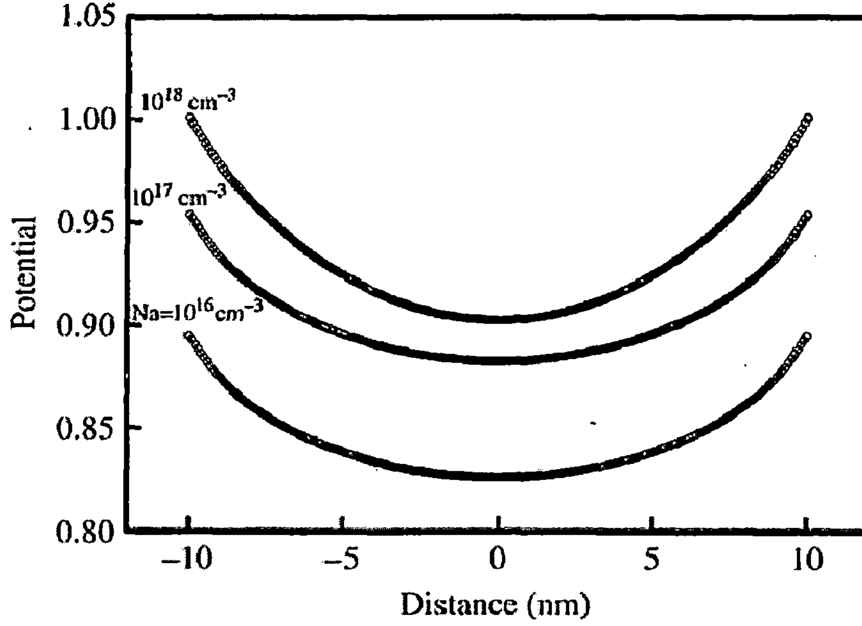


Figure 2.4: Variation of potential distribution along Si thickness with different Channel doping concentration in DGMOSFETs [6]

2.3.2. Threshold Voltage Model

The threshold voltage model was proposed by Yuan Taur in [1] and Chiang in [5]. We present here the details given by both the authors. The threshold voltage V_{th} can be defined as that value of the gate voltage V_{gs} at which a conducting channel is induced at the surface of the DG-MOSFET. Therefore, the threshold voltage is taken to be the value of gate source voltage for which the minimum surface potential is given $\Phi_{s,min} = 2\Phi_f$, where Φ_f is the fermi potential at the Si-SiO_2 interface which is given by:

$$\Phi_f = \frac{kT}{q}.\ln\left(\frac{N_A}{n_i}\right) \tag{2.30}$$

Hence we can determine the value of threshold voltage from (2.26) by substituting $\Phi_{d_{eff,min}} = 2\Phi_f$ and $V_{gs} = V_{th}$ which is given as:

$$\Phi_{d_{eff,min}} \approx 2\sqrt{PQ}\exp\left(-\frac{L_g}{2\lambda_3}\right) - D \tag{2.31}$$

Therefore

$$2\Phi_f \approx 2\sqrt{(v_{bi} + v_{ds} + D)Q}\exp\left(-\frac{L_g}{2\lambda_3}\right) - \frac{qN_A}{\varepsilon_{si}}\frac{1-A}{2C} + V_{th} - v_{fb} \tag{2.32}$$

Now, substituting the values of D in (2.32) from (2.21), we get,

$$2\Phi_f \approx 2\sqrt{\left(v_{bi} + v_{ds} + \frac{qN_A}{\varepsilon_{si}}\frac{1-A}{2C} - V_{th} + v_{fb}\right) Q \exp\left(-\frac{L_g}{2\lambda_3}\right)} - \frac{qN_A}{\varepsilon_{si}}\frac{1-A}{2C} + V_{th} - v_{fb}$$

.... (2.33)

We now get the expression for threshold voltage as:

$$V_{th} \approx \frac{2\Phi_f + v_{fb} + \frac{qN_A}{\varepsilon_{si}}\frac{1-A}{2C} - 2\sqrt{\left(v_{bi} + v_{ds} + \frac{qN_A}{\varepsilon_{si}}\frac{1-A}{2C} + v_{fb}\right) Q \exp\left(-\frac{L_g}{2\lambda_3}\right)}}{1 + Q\exp\left(-\frac{L_g}{2\lambda_3}\right)} \quad (2.34)$$

The general short channel V_{th} model shown in (2.34) reduces to a long channel one, when $L_g = \infty$ (large value of channel length), for which the expression is as shown below:

$$V_{th,long} \approx \frac{2\Phi_f + v_{fb} + \frac{qN_A}{\varepsilon_{si}}\frac{1-A}{2C}}{1 + Q\exp\left(-\frac{L_g}{2\lambda_3}\right)} \quad (2.35)$$

The threshold voltage model presented in [5] did not take into account the presence of mobile carriers in the channel. Hence,the model cannot clearly demarcate the transition between the weak and strong inversion regions.

The threshold voltage roll-off given in [1,] is the difference between long and short channel V_{th} which is given by: $\Delta V_{th} = V_{th,long} - V_{th,short}$,

$$\Delta V_{th} = \frac{2\sqrt{\left(v_{bi} + v_{ds} + \frac{qN_A}{\varepsilon_{si}}\frac{1-A}{2C} + v_{fb}\right) Q \exp\left(-\frac{L_g}{2\lambda_3}\right)}}{1 + Q\exp\left(-\frac{L_g}{2\lambda_3}\right)} \quad (2.36)$$

Fig.2.5 and Fig.2.6 show the variation of threshold voltage roll-off with different parameters like drain bias voltage and thickness of the silicon film.

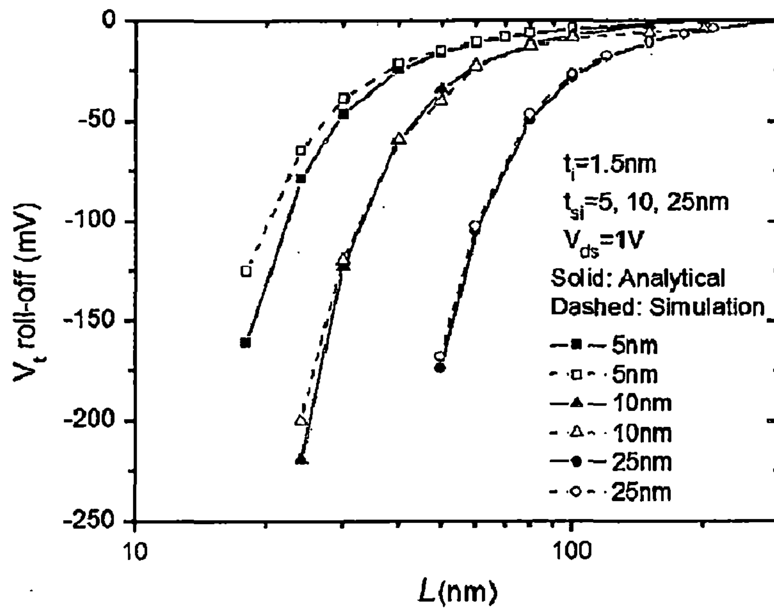


Figure 2.5: Variation of threshold voltage rolloff with different t_{si} for fixed $t_{ox} = 1.5nm$ [1]

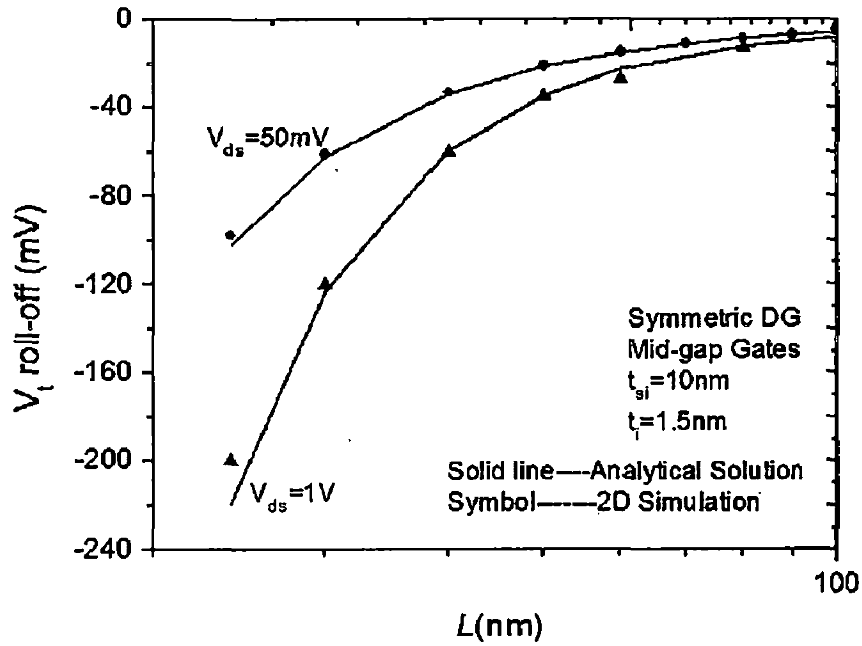


Figure 2.6: Low drain and high drain threshold voltage rolloff for $t_{ox} = 1.5nm$[1]

Figure 2.7 variation of threshold voltage with Si film thickness in DGMOSFET [8]

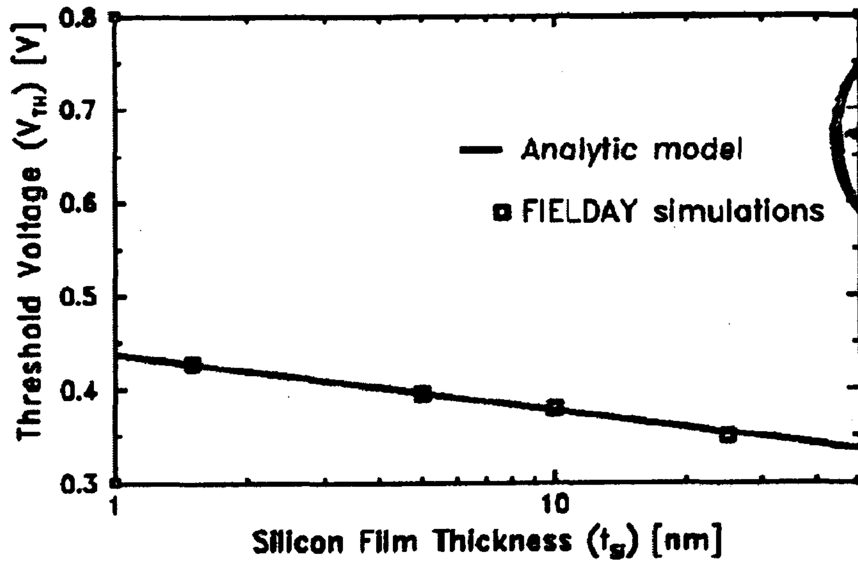


Figure 2.7: Dependence of long-channel threshold voltage on silicon film thickness [8]

2.3.3. Subthreshold Drain Current Model

The subthreshold drain current model was given by Yuan Taur in [1]. The MOSFET current density J predominantly flows in the x direction (from source to drain). The current density (both drift and diffusion) can be given as:

$$J = -q\mu n(x,y)\frac{d\Phi_n(x)}{dx} \tag{2.34}$$

Where the electron quasi–Fermi potential Φ_n is essentially constant in the y direction.

$$I_{ds} = -\mu w\frac{d\Phi_n(x)}{dx}Q_i(x) \tag{2.35}$$

Where

$$Q_i(x) = \int_{-t_{si}/2}^{t_{si}/2} n(x,y)dy = \int_{-t_{si}/2}^{t_{si}/2} n_i e^{q[\Phi(x,y)-\Phi_n(x)]/kT}dy \tag{2.36}$$

Where Q_i is the inversion charge per gate area and Φ (x, y) is given by (2.15). Current continuity condition requires I_{ds} to be independent of x. The subthreshold current can be calculated analytically as a function of V_{gs} and V_{ds} as shown below:

$$I_{ds} = \frac{\mu w \int_0^{V_{ds}} e^{-q\Phi_n(x)/kT} d\Phi_n(x)}{\int_0^L \frac{dx}{\int_{-t_{si}/2}^{t_{si}/2} n_i e^{q\Phi(x,y)/kT}dy}} = \frac{\mu w\left(\frac{kT}{q}\right)\left[1-exp\left(-\frac{qV_{ds}}{kT}\right)\right]}{\int_0^L \frac{dx}{\int_{-t_{si}/2}^{t_{si}/2} n_i e^{q\Phi(x,y)/kT}dy}} \tag{2.37}$$

Fig.2.8 shows the variation of subthreshold current with V_{gs} in DGMOSFET for different channel length values.

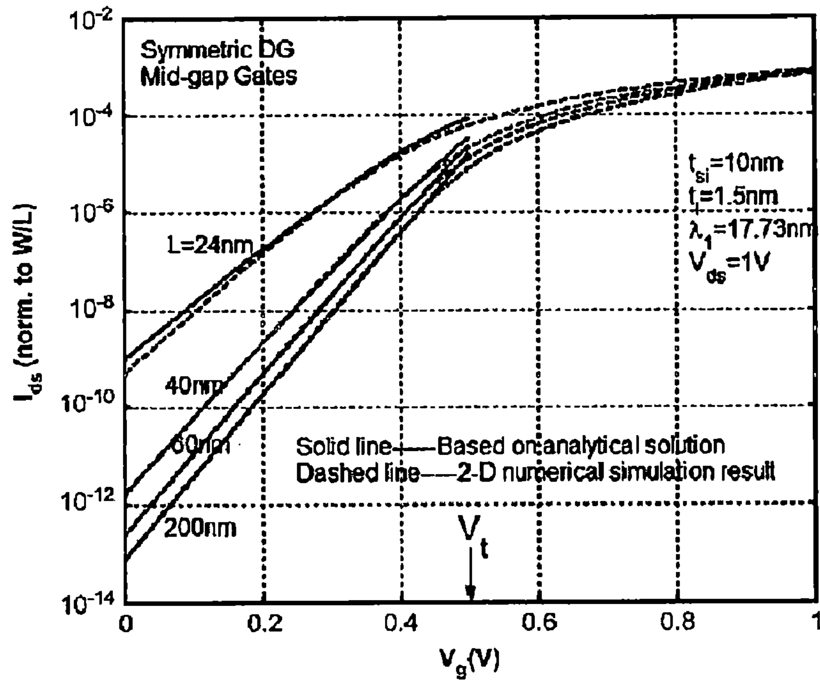


Figure 2.8: I_{ds}-V_{gs} curves for symmetric DGMOSFETs [1]

From (2.37) we can observe that the subthreshold current depends exponentially on the values of V_{gs} and this was observed in the graph shown in Fig.2.8 by [1]. Also from the graph, it can be observed that the maximum barrier or the minimum potential point is located approximately midway between the source and the drain.

This completes the review on analytical modeling of DG-MOSFET. In this chapter, we have seen the modeling of potential distribution along Si film thickness, threshold voltage modeling and subthreshold drain current modeling. In the next chapter, we propose a new scheme of two dimensional analytical modeling of DG-MOSFET using Green's functions.

CHAPTER 3

TWO DIMENSIONAL ANALYTICAL MODELING OF DOUBLE GATE MOSFET USING GREEN'S FUNCTIONS

3.1 Introduction

The two dimensional modeling of potential distribution, surface potential and threshold voltage of DG-MOSFETs with uniform doping profile has been done with the help of Green's function. The advantage of using Green's function is that it simplifies the modeling of DG-MOSFET parameters for any generic doping profile. The proposed model is valid for uniform doping profile of symmetric DG-MOSFET but it can be extended easily for any doping profile. The accuracy of the model has been verified by comparison with existing models from literature.

3.2 DG-MOSFET Device structure:

The cross-sectional view of symmetrical DG-MOSFET's is shown in Fig. 3.1. in which both the gates consist of p+ poly of length L. The doping of p type body and n+ source/drain regions is kept constant at 1 x 10^{15} cm^{-3}. Typical values of the gate oxide thickness and the thin-film thickness are 5nm and 20nm respectively.

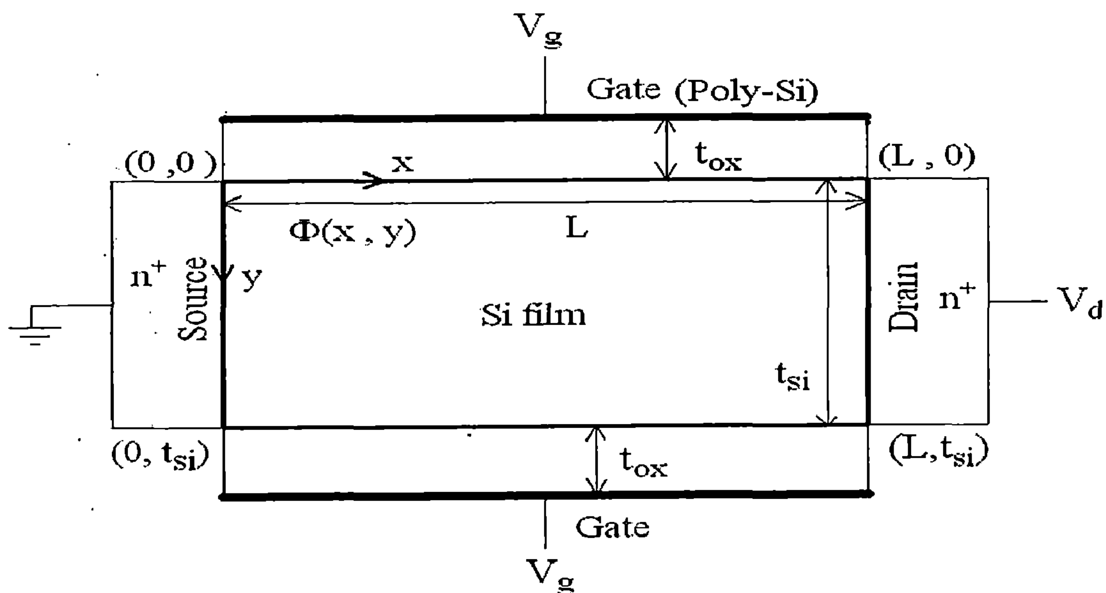


Figure. 3.1: Cross-sectional view of DG-MOSFET

3.3 Model Formulation

3.3.1 Surface Potential Derivation:

The potential distribution in the silicon thin-film, before the onset of strong inversion can be expressed as:

$$\frac{\partial^2\Phi(x,y)}{\partial x^2}+\frac{\partial^2\Phi(x,y)}{\partial y^2}=\frac{\rho(x,y)}{\varepsilon_{si}} \qquad 0\le x\le L\ ,0\le y\le t_{si} \tag{3.1}$$

Where $\rho(x,y)=-qN_af(y)$, is the charge density of Silicon region.

Where q is the electronic charge, $f(y)$ is the doping profile in the channel region, N_a is body concentration, ε_{si} is permittivity of Silicon dielectric constant, L is the device channel length and $t_{si}$is Silicon thickness. Here we assume parabolic potential distribution in the vertical direction of gate length. In a DG-MOSFET the gate consists of only one material i.e., p+ poly, with work functionΦ_M, respectively. Therefore interface (Si-SiO_2) flat-band voltage of the p+ poly at the gate

$$V_{fb}=\Phi_{MS}=\Phi_M-\Phi_{Si} \tag{3.2}$$

Where Φ_M is gate work function and Φ_{Si} is silicon work function which is given by

$$\Phi_{Si}=\chi_{Si}+\frac{E_g}{2q}+\Phi_f \tag{3.3}$$

Where E_g is the silicon band gap at 300K,

χ_{Si} is the electron affinity of silicon,

$\Phi_f=V_t\ln\left(\frac{N_A}{n_i}\right)$ is the Fermi potential, $V_t$is the thermal voltage and

$n_i(1.5\times10^{15})$ is the intrinsic carrier concentration of silicon.

The Poisson's equation is solved under the gate materials (p+ poly) using the following boundary conditions:

1. Electric flux at the front gate-oxide interface is continuous for the DG-MOSFET's. Therefore,

$$\frac{\partial\Phi\,(x,y)}{\partial y}\bigg|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Phi_S-V'_{gs}}{t_{ox}} \tag{3.4}$$

Where ε_{ox} is the dielectric constant of the oxide,

t_{ox} is the gate oxide thickness and

$$V'_{gs} = V_{gs} - V_{fb} \tag{3.5}$$

Where V_{gs} is the gate-to-source bias voltage, V_{fb} is the flat-band voltages of p^+ polysilicon, respectively, and are given by (3.3).

2. Electric flux at the back gate-oxide interface is also continuous for the DGMOSFET's. Therefore,

$$\left.\frac{\partial\Phi\,(x,y)}{\partial y}\right|_{y=t_{si}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Phi_S - V'_{gs}}{t_{ox}} \tag{3.6}$$

3. Electric field at the centre of Si, is zero.

$$\left.\frac{\partial\Phi\,(x,y)}{\partial y}\right|_{y={t_{si}}/{2}} = 0 \tag{3.7}$$

4. The potential at the source end is

$$\Phi\,(0,y) = V_{bi} \tag{3.8}$$

Where $V_{bi} = V_t \ln\left(\frac{N_D N_A}{n_i^2}\right)$ the built-in potential is across the Si body-source junction and N_A and N_D are the Si body and source/drain doping respectively.

5. The potential at the drain end is

$$\Phi\,(L,y) = V_{bi} + V_{ds} \tag{3.9}$$

Where V_{ds} is the applied drain-source bias voltage.

The Green's function for the potential in rectangular region is

$$\left.\begin{aligned}
G_x(x,y;\,x',y') &= \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(k_n x')\sin(k_n x)\sinh(k_n y)\sinh k_n(t_{si}-y')}{K_n\sinh(k_n t_{si})} && \text{For } y < y' \\
G_x(x,y;\,x',y') &= \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(k_n x')\sin(k_n x)\sinh(k_n y')\sinh k_n(t_{si}-y)}{K_n\sinh(k_n t_{si})} && \text{For } y > y' \\
G_y(x,y;\,x',y') &= \frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sin(k_m y')\sinh(k_m x)\sinh k_m(L-x')}{k_m\sinh(k_m L)} && \text{For } x < x' \\
G_y(x,y;\,x',y') &= \frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sin(k_m y')\sinh(k_m x')\sinh k_m(L-x)}{k_m\sinh(k_m L)} && \text{For } x > x'
\end{aligned}\right\}$$

Derivation of Green's function in rectangular region given in Appendix.

Therefore Potential distribution in Si region in DG-MOSFETs by Green's theorem [18], which is given as

$$\Phi(x,y) = \iint \frac{\rho(x',y')}{\varepsilon_{si}} G(x,y;\, x',y')dx'\,dy' + \int G(x,y;\, x',y')\frac{\partial\phi}{\partial n'}ds' - \int \Phi(x',y')\frac{\partial G}{\partial n'}ds' \quad (3.10)$$

Where $G(x,y;\, x',y')$ is the Green's function satisfying $\nabla^2 G(x,y;\, x',y') = -\delta(x-x')\delta(y-y')$. $\Phi(x',y')$ is the potential distribution on the boundary, $\frac{\partial\phi}{\partial n'}$ & $\frac{\partial G}{\partial n'}$ is the outward normal on the boundary surface, ε_{si} is dielectric constant in Si region and $\rho(x',y') = -qN_A f(y')$ Charge density in Si region. This is two dimensional surface integration (along the channel length and Si film).

$$\iint \frac{\rho(x',y')}{\varepsilon_{si}} G(x,y;\, x',y')dx'\,dy' = I_1 + I_2 + I_3 + I_4 \quad (3.11)$$

Where I_1, I_2, I_3 & I_4 is

$$I_1 = \frac{4}{Lt_{si}}\sum_{n=1}^{\infty}\frac{\sin(k_n x)\sinh(k_n y)}{k_n\sinh(k_n t_{si})}\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sinh(k_m x)}{k_m\sinh(k_m L)}\int_0^{y'}\frac{\rho(x',y')}{\varepsilon}\sinh k_n(t_{si}-y')\sin k_m y'\,dy'\int_0^{x'}\sin k_n x'\,\sinh k_m(L-x')dx' \quad (3.12)$$

$$I_2 = \frac{4}{Lt_{si}}\sum_{n=1}^{\infty}\frac{\sin(k_n x)\sinh(k_n y)}{k_n\sinh(k_n t_{si})}\cdot\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sinh k_m(L-x)}{k_m\sinh(k_m L)}\int_0^{y'}\frac{\rho(x',y')}{\varepsilon}\sinh k_n(t_{si}-y')\sin k_m y'\,dy'\int_{x'}^{L}\sin k_n x'\,\sinh k_m(L-x')dx' \quad (3.13)$$

$$I_3 = \frac{4}{Lt_{si}}\sum_{n=1}^{\infty}\frac{\sin(k_n x)\sinh k_n(t_{si}-y)}{k_n\sinh(k_n t_{si})}\times\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sinh(k_m x)}{k_m\sinh(k_m L)}\int_{y'}^{t_{si}}\frac{\rho(x',y')}{\varepsilon}\sinh k_n y'\sin k_m y'\,dy'\int_0^{x'}\sin k_n x'\,\sinh k_m(L-x')dx' \quad (3.14)$$

$$I_4 = \frac{4}{Lt_{si}}\sum_{n=1}^{\infty}\frac{\sin(k_n x)\sinh k_n(t_{si}-y)}{k_n\sinh(k_n t_{si})}\times\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sinh k_m(L-x)}{k_m\sinh(k_m L)}\int_{y'}^{t_{si}}\frac{\rho(x',y')}{\varepsilon}\sinh k_n y'\sin k_m y'\,dy'\int_{x'}^{L}\sin k_n x'\,\sinh k_m x'dx' \quad (3.15)$$

Where $k_n = \frac{n\pi}{L}$ is Eigen value in x direction.

$k_m = \frac{m\pi}{t_{si}}$ is Eigen value in y direction.

All these value put in (3.11), and get the

$$\iint \frac{\rho(x',y')}{\varepsilon_{si}} G(x,y;\ x',y')dx'\,dy' =$$

$$\left\{\frac{4}{Lt_{si}}\sum_{n=1}^{\infty}\frac{\sin(k_n x)\sinh(k_n y)}{k_n \sinh(k_n t_{si})}\int_0^{y'}\frac{\rho(x',y')}{\varepsilon} sinhk_n(t_{si} - y')sink_m y'dy' + \frac{4}{Lt_{si}}\sum_{n=1}^{\infty}\frac{\sin(k_n x)\sinh k_n(t_{si}-y)}{k_n \sinh(k_n t_{si})}\int_{y'}^{t_{si}}\frac{\rho(x',y')}{\varepsilon} sinhk_n y' sink_m y'dy'\right\} \times \left\{\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sinh(k_m x)}{k_m \sinh(k_m L)}\int_0^{x'} sink_n x'\ sinhk_m(L - x')dx' + \sum_{m=1}^{\infty}\frac{\sin(k_m y)\sinh k_m(L-x)}{k_m \sinh(k_m L)}\int_{x'}^{L} sink_n x'\ sinhk_m x'dx'\right\} \quad (3.16)$$

Now solve this term

$$\int G(x,y;\ x',y')\frac{\partial\phi}{\partial n'}ds'$$

where $\frac{\partial\phi}{\partial n'}$ is normal to surface. DG-MOSFETs width is nanometer, therefore assume surface integral is convert to line integral, therefore ds' convert to $\partial x'$or $\partial y'$.

at $x' = 0$(source side) , $\frac{\partial\phi}{\partial n'} = -\frac{\partial\phi}{\partial x'}$.

$$\int_0^{t_{si}} -\frac{\partial\phi(x',y')}{\partial x'}\left[u(x - x')G_y{}^2 + u(x' - x)G_y{}^1\right]\partial y' \quad (3.17)$$

Similarly at drain side, at $x' = L$ (drain side), $\frac{\partial\phi}{\partial n'} = \frac{\partial\phi}{\partial x'}$

$$\int_0^{t_{si}} \frac{\partial\phi(x',y')}{(\partial x')}\left[u(x - x')G_y{}^2 + u(x' - x)G_y{}^1\right]\partial y' \quad (3.18)$$

and along the front channel, at $y' = 0$, $\frac{\partial\phi}{\partial n'} = \frac{\partial\phi}{\partial y'}$

$$\int_0^{L} \frac{\partial\phi(x',y')}{\partial y'}\left[u(y - y')G_x{}^2 + u(y' - y)G_x{}^1\right]\partial x' \quad (3.19)$$

and back channel, at $y' = t_{si}$, $\frac{\partial\phi}{\partial n'} = -\frac{\partial\phi}{\partial y'}$

$$\int_0^{L} -\frac{\partial\phi(x',y')}{\partial y'}\left[u(y - y')G_x{}^2 + u(y' - y)G_x{}^1\right]\partial x' \quad (3.20)$$

Eq.(3.17),(3.18),(3.19) and (3.20) put in expression $\int G(x,y;\ x',y')\frac{\partial\phi}{\partial n'}ds'$ and get the

$$\int G(x,y;\ x',y')\frac{\partial\phi}{\partial n'}ds' = 0 \quad (3.21)$$

Now solve this term

$$\int \Phi\,(x',y')\frac{\partial G}{\partial n'}\mathrm{d}s'$$

Where G is Green's function,

At the source side, $\frac{\partial G}{\partial n'} = -\frac{\partial G}{\partial x'}$

$$\int_0^{t_{si}} \Phi\,(0,y')\frac{\partial G_y}{\partial x'}\mathrm{d}y' = \frac{-2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y)\sinh K_m(L-x)}{\sinh K_m L}\int_0^{t_{si}} \Phi\,(0,y')\sin k_m y'\mathrm{d}y' \quad (3.22)$$

At the drain side, $\frac{\partial G}{\partial n'} = \frac{\partial G}{\partial x'}$

$$\int_0^{t_{si}} \Phi\,(L,y')\frac{\partial G_y}{\partial x'}\mathrm{d}y' = \frac{-2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y)\sinh K_m x}{\sinh K_m L}\int_0^{t_{si}} \Phi\,(L,y')\sin k_m y'\mathrm{d}y' \quad (3.23)$$

At the front channel, $\frac{\partial G}{\partial n'} = \frac{\partial G}{\partial y'}$

$$\int_0^{L} \Phi\,(x',0)\frac{\partial G_x}{\partial y'}\mathrm{d}x' = \frac{-2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x)\sinh k_n(t_{si}-y)}{\sinh k_n t_{si}}\int_0^{L} \Phi\,(x',0)\sin k_n x'\,\mathrm{d}x' \quad (3.24)$$

At the back channel, $\frac{\partial G}{\partial n'} = -\frac{\partial G}{\partial y'}$

$$\int_0^{L} \Phi\,(x',t_{si})\frac{\partial G_x}{\partial y'}\mathrm{d}x' = \frac{-2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x)\sinh k_n y}{\sinh k_n t_{si}}\int_0^{L} \Phi\,(x',t_{si})\sin k_n x'\,\mathrm{d}x' \quad (3.25)$$

Eq.(3.22),(3.23),(3.24) and (3.25) substitute in $\int \Phi\,(x',y')\frac{\partial G}{\partial n'}\mathrm{d}s'$, and get the

$$\int \Phi\,(x',y')\frac{\partial G}{\partial n'}\mathrm{d}s' = \frac{-2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y)\sinh K_m(L-x)}{\sinh K_m L}\int_0^{t_{si}} \Phi\,(0,y')\sin k_m y'\mathrm{d}y' -$$
$$\frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y)\sinh K_m x}{\sinh K_m L}\int_0^{t_{si}} \Phi\,(L,y')\sin k_m y'\mathrm{d}y' - \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x)\sinh k_n(t_{si}-y)}{\sinh k_n t_{si}}\times$$
$$\int_0^{L} \Phi\,(x',0)\sin k_n x'\,\mathrm{d}x' - \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x)\sinh k_n y}{\sinh k_n t_{si}}\int_0^{L} \Phi\,(x',t_{si})\sin k_n x'\,\mathrm{d}x' \quad (3.26)$$

Eq.(3.26),(3.21) and (3.16) substitute (3.10), 2D potential distribution in Si region is

$$\Phi\,(x,y) = \Big\{\frac{4}{Lt_{si}}\sum_{n=1}^{\infty}\frac{\sin(k_n x)\sinh(k_n y)}{k_n\sinh(k_n t_{si})}\int_0^{y'}\frac{\rho(x',y')}{\varepsilon_{si}}\,sinhk_n(t_{si}-y')sink_m y'dy' +$$
$$\frac{4}{Lt_{si}}\sum_{n=1}^{\infty}\frac{\sin(k_n x)\sinh k_n(t_{si}-y)}{k_n\sinh(k_n t_{si})}\int_{y'}^{t_{si}}\frac{\rho(x',y')}{\varepsilon_{si}}\,sinhk_n y' sink_m y'dy'\Big\}\times$$
$$\Big\{\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sinh(k_m x)}{k_m\sinh(k_m L)}\int_0^{x'} sink_n x'\ sinhk_m(L-x')dx' +$$
$$\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sinh k_m(L-x)}{k_m\sinh(k_m L)}\int_{x'}^{L} sink_n x'\ sinhk_m x'dx'\Big\} +$$
$$\frac{-2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y)sinhK_m(L-x)}{sinhK_m L}\int_0^{t_{si}}\Phi\,(0,y')\sin k_m y'dy' -$$
$$\frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(K_m y)sinhK_m x}{sinhK_m L}\int_0^{t_{si}}\Phi\,(L,y')\sin k_m y'dy' -$$
$$\frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x)\sinh k_n(t_{si}-y)}{\sinh k_n t_{si}}\int_0^{L}\Phi\,(x',0)\sin k_n x'\,dx' -$$
$$\frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(K_n x)\sinh k_n y}{\sinh k_n t_{si}}\int_0^{L}\Phi\,(x',t_{si})\sin k_n x'\,dx' \qquad (3.27)$$

$$\text{Where } \rho(x',y') = -qN_A f(y') \qquad (3.28)$$

is charge density in Si region, q is electronic charge, N_A doping concentration in channel and f(y') is doping profile in Si region. This general electrostatic potential distribution in Si region in eq. (3.27) can deal with any arbitrary doping profile (like uniform, step index etc.). But we have assumed now uniform doping profile (f(y') = 1) in Si region and calculate potential distribution.

$$\Phi\,(x,y) = \frac{Q_B^0}{2\varepsilon_{si}}x(L-x) + \sum_{m=1}^{\infty}\frac{Q_B^n}{\varepsilon_{si}}\frac{cosK_m y}{(K_m)^2}\left[\frac{sinhK_m x + sinhK_m(L-x)}{sinhK_m L}\right] + B_0^s\left(1-\frac{x}{L}\right) + B_0^D\frac{x}{L} +$$
$$\sum_{m=1}^{\infty}\frac{cosK_m y}{sinhK_m L}\left[B_m^s sinhK_m(L-x) + B_m^D sinhK_m x\right] +$$
$$\sum_{n=1}^{\infty}\frac{sinK_n x}{\varepsilon_{si}k_n\sinh k_n t_{si}}\left[D_{sf}^m coshk_n(t_{si}-y) - D_{sb}^m coshk_n y\right] \qquad (3.29)$$

Where $\Phi\,(0,y') = V_{bi}$

$\Phi\,(L,y') = V_{bi} + V_{ds}$

D_{sf}^m and D_{sb}^m is charge density in front and back gate oxide

$$D_{sf}^m = \frac{2}{L}\int_0^L D_{sf}(x)\sin(k_n x)\,dx$$

$$D_{sb}^m = \frac{2}{L}\int_0^L D_{sb}(x)\sin(k_n x)\,dx$$

Where

$$D_{sf}(x,0) = \varepsilon_{si}\frac{\partial\Phi\,(x,y)}{\partial y}$$

$$D_{sb}(x,t_{si}) = -\varepsilon_{si}\frac{\partial\Phi\,(x,y)}{\partial y}$$

D_{sf} is the charge density of Si-SiO_2 interface of front and back gate side.

Bulk charge density

$$Q_B^n = \frac{2}{t_{si}}\int_0^{t_{si}} -qN_A f(y')\cos K_m y\, dy$$

$$Q_B^0 = \frac{2}{t_{si}}\int_0^{t_{si}} -qN_A f(y')\, dy$$

Source boundary potential

$$B_m^S = \frac{2}{t_{si}}\int_0^{t_{si}} V_{bi}\cos K_m y\, dy$$

$$B_0^S = \frac{1}{t_{si}}\int_0^{t_{si}} V_{bi}\, dy \qquad \text{and}$$

Drain boundary potential

$$B_m^D = \frac{2}{t_{si}}\int_0^{t_{si}} (V_{bi}+V_{ds})\cos K_m y\, dy$$

$$B_0^D = \frac{2}{t_{si}}\int_0^{t_{si}} (V_{bi}+V_{ds})\, dy$$

Therefore, the 2D potential distribution at Si region

$$\Phi\,(x,y) = \frac{-qN_A}{2\varepsilon_{si}}x(L-x) + V_{bi} + V_{ds}\frac{x}{L} + \sum_{n=1}^{\infty}\frac{\sin K_n x}{\varepsilon_{si}k_n \sinh k_n t_{si}}\left[D_{sf}^m \cosh k_n(t_{si}-y) - D_{sb}^m \cosh k_n y\right] \qquad (3.30)$$

Surface potential distribution in the Si film region is y=0(front gate) and y= t_{si}(back gate), put in eq. (3.30),

$$\Phi\,(x,0) = \frac{-qN_A}{2\varepsilon_{si}}x(L-x) + V_{bi} + V_{ds}\frac{x}{L} + \sum_{n=1}^{\infty}\frac{\sin K_n x}{\varepsilon_{si}k_n \sinh k_n t_{si}}\left[D_{sf}^m \cosh k_n t_{si} - D_{sb}^m\right] \qquad (3.31)$$

The potential $\Phi\,(x,y)$ must satisfy the continuous of the transverse electric field and normal electric displacement at the SiO_2-Si interface, therefore D_{sf}^m and D_{sb}^m is

$$D_{sf}^m = \frac{\varepsilon_{ox}[B.D\varepsilon_{si}k_n \sinh k_n t_{si} - C.\sin K_n x]}{[B.\varepsilon_{si}\sinh k_n t_{si} + B.\varepsilon_{ox}\cosh k_n t_{si} - A.\varepsilon_{ox}].\sin K_n x} \qquad (3.32)$$

and $\quad D_{sb}^m = -D_{sf}^m \qquad (3.33)$

Where coefficient is

$$A = \frac{sinK_n x}{K_n}\left\{\frac{1}{\varepsilon_{ox}} + \frac{1}{\varepsilon_{si}\tanh k_n t_{si}} - \frac{1}{\varepsilon_{si}\sinh k_n t_{si}}\right\} \tag{3.34}$$

$$B = \frac{sinK_n x}{K_n}\left\{\frac{1}{\varepsilon_{si}\sinh k_n t_{si}} - \frac{1}{\varepsilon_{si}\tanh k_n t_{si}} - \frac{\tanh k_n t_{ox}}{\varepsilon_{ox}}\right\} \tag{3.35}$$

$$C = \frac{2sinK_m t_{ox}}{t_{ox}K_m \sinh k_m L}\{V_{bi} sinhK_m(L-x) + (V_{bi}+V_{ds})sinhK_m x\} \tag{3.36}$$

$$D = \frac{4(V_{gs}-V_{fb})sinhK_n x}{n\pi coshk_n t_{ox}} + \frac{qN_A}{2\varepsilon_{si}}x(L-x) - V_{bi} - V_{ds}\frac{x}{L} \tag{3.37}$$

$$E = sinK_n x\{\varepsilon_{si}\sinh k_n t_{si} + \varepsilon_{ox}\cosh k_n t_{si} - \frac{A}{B}\varepsilon_{ox}\} \tag{3.38}$$

The position of the minimum potential along the surface of the Si film can be calculated,

$$\frac{\partial\Phi\,(x,0)}{\partial x}\Big|_{x=x_{min}} = 0 \tag{3.39}$$

Where x_{min} is the position of the minimum surface potential.

Therefore eq. (3.39)

$$\frac{\varepsilon_{ox}\cosh k_n t_{si}}{E}\left\{\frac{qN_A}{\varepsilon_{si}}\frac{x_{min}(L-x_{min})K_n}{tanK_n x_{min}} - \frac{qN_A}{2\varepsilon_{si}}x_{min}(L-2x_{min}) - \frac{V_{ds}}{L} - \frac{2V_{ds}}{L}\frac{x_{min}K_n}{tanK_n x_{min}} - \frac{2V_{bi}K_n}{tanK_n x_{min}} + \frac{4(V_{gs}-V_{fb})}{L.coshk_n t_{ox} tanK_n x_{min}}\right\} - \frac{qN_A}{2\varepsilon_{si}}x_{min}(L-2x_{min}) + \frac{V_{ds}}{L} = 0 \tag{3.40}$$

However, the position of the minimum surface potential x_{min} can only be solved iteratively and no explicit form of x_{min} can be obtained .put this value in eq. (3.31) so we can get minimum surface potential

$$\Phi_{min}(x_{min}, 0) = \frac{-qN_A}{2\varepsilon_{si}}x_{min}(L-x_{min}) + V_{bi} + V_{ds}\frac{x_{min}}{L} + \sum_{n=1}^{\infty}\frac{sinK_n x_{min}}{\varepsilon_{si}k_n \sinh k_n t_{si}}\left[D_{sf}^m coshk_n t_{si} - D_{sb}^m\right] = \Phi_{s,min} \tag{3.41}$$

The above two equations are quite useful in determining how the potential distribution in Si film region and surface potential to is modified by the proposed DG-MOSFET's structure.

$$E(x) = \frac{\partial\Phi\,(x,0)}{\partial x} = \frac{\varepsilon_{ox}\cosh k_n t_{si}}{E}\left\{\frac{qN_A}{\varepsilon_{si}}\frac{x(L-x)K_n}{tanK_n x} - \frac{qN_A}{2\varepsilon_{si}}x(L-2x) - \frac{V_{ds}}{L} - \frac{2V_{ds}}{L}\frac{xK_n}{tanK_n x} - \frac{2V_{bi}K_n}{tanK_n x} + \frac{4(V_{gs}-V_{fb})}{L.coshk_n t_{ox} tanK_n x}\right\} - \frac{qN_A}{2\varepsilon_{si}}x(L-2x) + \frac{V_{ds}}{L} \tag{3.42}$$

This equation is useful in determine the electric field along the Si film at the interface of Si-Sio_2.

3.3.2 Threshold Voltage Model

The threshold voltage V_{th} is that value of the gate voltage (V_{gs}) at which a conducting channel is induced at the surface of the DG-MOSFET. The channel doping is uniform with an acceptor concentration of $10^{16}\ cm^{-3}$ as in [20]. The threshold voltage, V_{th} for the DG-MOSFET model is derived from the analytical approach followed in [22].

The threshold voltage definition in terms of surface potential is taken to be that value of gate source voltage for which $\Phi_{s,min} = 2\Phi_f$, where $\Phi_f = \frac{kT}{q}.\ln\left(\frac{N_A}{n_i}\right)$ and $V_{gs} = V_{th}$ put in eq. (3.41),therefore

$$2\Phi_f = \frac{-qN_A}{2\varepsilon_{si}} x_{min}(L - x_{min}) + V_{bi} + V_{ds}\frac{x_{min}}{L} + \sum_{n=1}^{\infty}\frac{sinK_n x_{min}}{\varepsilon_{si}k_n \sinh k_n t_{si}}\left[D_{sf}^m coshk_n t_{si} - D_{sb}^m\right] \quad (3.43)$$

Therefore threshold voltage

$$V_{th} = V_{fb} + \left\{2\Phi_f + \frac{-qN_A}{2\varepsilon_{si}} x_{min}(L - x_{min}) - V_{bi} - V_{ds}\frac{x_{min}}{L}\right\}\frac{\{sinK_n x_{min}\}^{-1}}{2G_f} - \frac{P}{2G_f} \quad (3.44)$$

Where

$$G_f = [1 - (-1)^n]\frac{R}{d_0}\left[\frac{2}{m\pi coshk_n t_{ox}} + \sum_{m=1}^{\infty}\frac{t}{(m-.5)\pi}\left[(-1)^m - \frac{1}{(m-.5)\pi}\right]\right]$$

$$R = -\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\tanh k_n t_{ox}}{\sinh k_n t_{si}}$$

$$t = \frac{4}{n\pi}\left[1 + \frac{L^2(m-.5)^2}{{t_{ox}}^2 n^2}\right]$$

$$d_0 = \frac{1}{(\sinh k_n t_{si})^2} - \left\{\frac{\varepsilon_{si}\tanh k_n t_{ox}}{\varepsilon_{ox}} + \frac{1}{\tanh k_n t_{si}}\right\}^2$$

$$P = \frac{1}{d_0}\{[1 - (-1)^n]\frac{qN_A L^2}{2\varepsilon_{si}}\frac{8R}{(n.\pi)^3} + T[V_{bi}(1 - (-1)^n) + V_{ds}(-1)^{n+1}]\}$$

$$T = \sum_{m=1}^{\infty} 2Rt((m - .5)\pi)^{-2} - \frac{4R}{n\pi}$$

Therefore (3.44) is explicit expression of short channel V_{th} model. The general short channel V_{th} model is reduced to long channel {(L=∞) in a long channel threshold voltage model} one

$$V_{th,long} = V_{fb} - \frac{P}{2G_f} \quad (3.45)$$

The threshold voltage rolloff ΔV_{th} , which is the difference between short and long-channel V_{th} is obtained from (3.44) and (3.45) as

$$\Delta V_{th} = \left\{2\Phi_f + \frac{-qN_A}{2\varepsilon_{si}} x_{min}(L - x_{min}) - V_{bi} - V_{ds}\frac{x_{min}}{L}\right\}\frac{\{\sin K_n x_{min}\}^{-1}}{2G_f} \qquad (3.46)$$

In summary, this chapter presents 2-D potential distribution and threshold voltage analytical models of symmetric undoped DG-MOSFETs using Green's functions. Here channel doping profile is uniform. We will verify these models and discuss the results in Chapter IV with various effects like variation of film thickness, gate oxide thickness and substrate concentration etc.

CHAPTER 4

RESULTS AND DISCUSSION

In this chapter, results of developed analytical models have been presented. Simulations have been done in MATLAB and graphs for potential distribution along the silicon film depth, surface potential distribution along the channel, threshold voltage roll-off are drawn by varying different model parameters like silicon thickness, Gate oxide thickness, Gate bias voltage, Drain bias voltage and channel doping concentration. In the following section, we show potential distribution characteristics along depth of silicon film.

4.1. Potential Distribution along Silicon Film Thickness (Depth)

Fig.4.1 shows the potential variation along the Si thickness (front gate to back gate) for different gate bias voltages ($V_{gs} = 0.1V, 0.2V$ and $0.4V$). Constant values of gate oxide thickness, $t_{ox} = 2nm$, silicon thickness, $t_{si} = 20nm$ and doping concentration, $N_a = 10^{17}cm^{-3}$ are taken.

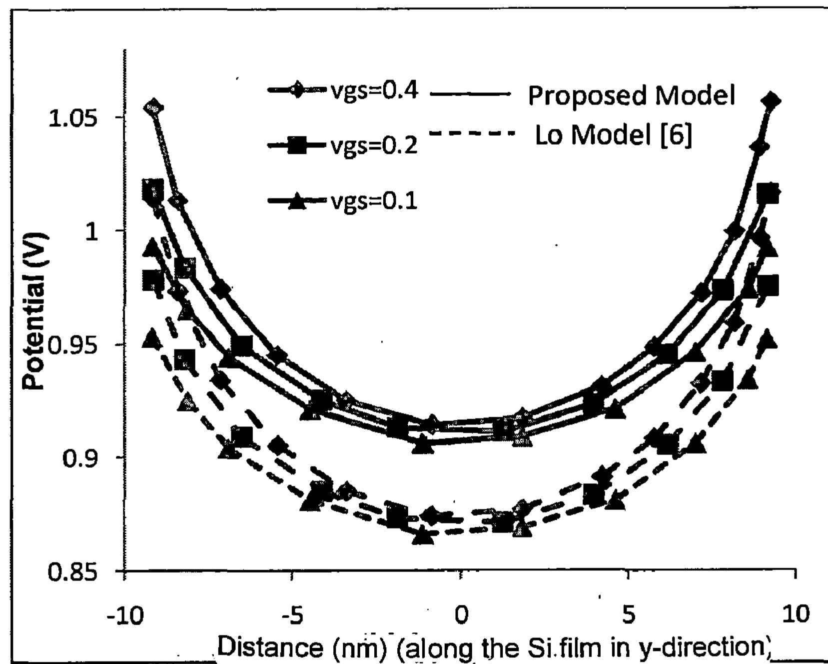
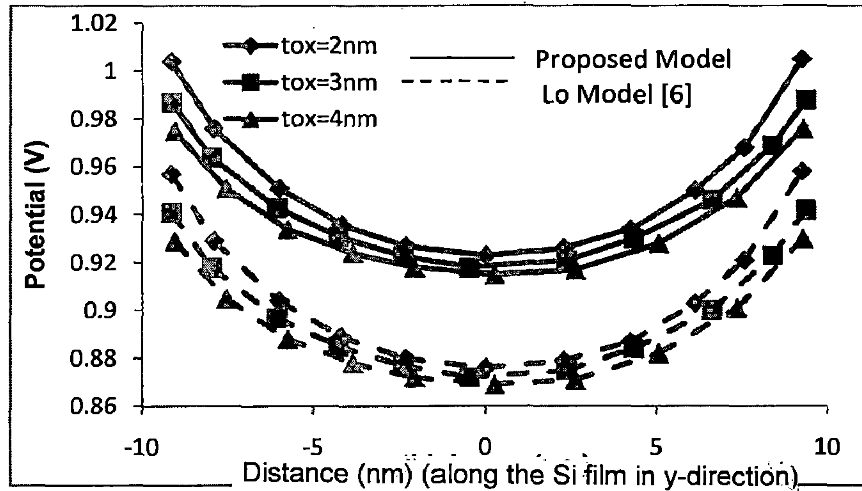


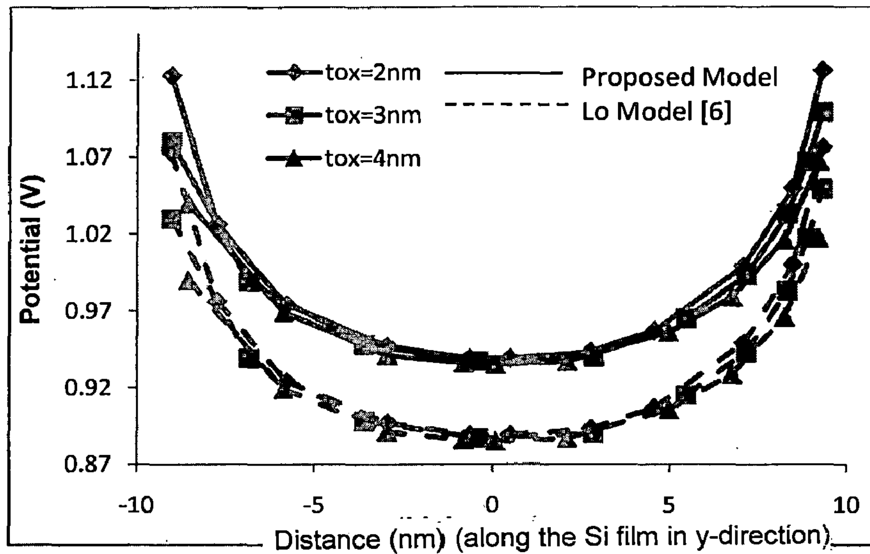
Figure.4.1: Comparison of the Lo [6] and proposed analytical potential model for the DG-MOSFET, where$t_{si} = 20nm$,$N_A = 10^{23}\mathrm{m}^{-3}$, and $t_{ox} = 2nm$.

The graph was observed to be of parabolic nature. We can see that this profile is symmetric about center of Si thickness. This can be attributed to the fact that the structure of DG-MOSFET is itself symmetric. This potential profile shifted upwards for increasing gate bias voltages. This is because of increase in Normal electric field for increasing gate bias voltages.

Fig.4.2 shows the variation of this potential distribution for different values of gate oxide thickness ($t_{ox} = 2nm, 3nm\ and\ 4nm$). Fig.4.2(a) and (b) parts are for different gate bias voltages $V_{gs} = 0.1V$ and $V_{gs} = 1.0V$ respectively. Values of other parameters are: $t_{si} = 20nm$ and doping concentration$N_a = 10^{17}cm^{-3}$.



(a)



(b)

Figure.4.2: Comparison of the Lo [6] and proposed analytical potential model for the DG-MOSFET .Where $t_{si} = 20nm$ and $N_a = 10^{17}cm^{-3}$ (a) $V_{gs} = 0.1V$ and (b) $V_{gs} = 1.0V$

The graph was observed to be of parabolic nature. We can see that this profile is symmetric about center of Si thickness. This can be attributed to the fact that the structure of DG-MOSFET is itself symmetric. This potential profile shifted upwards for increasing gate bias voltages. This is because of increase in Normal electric field for increasing gate bias voltages.

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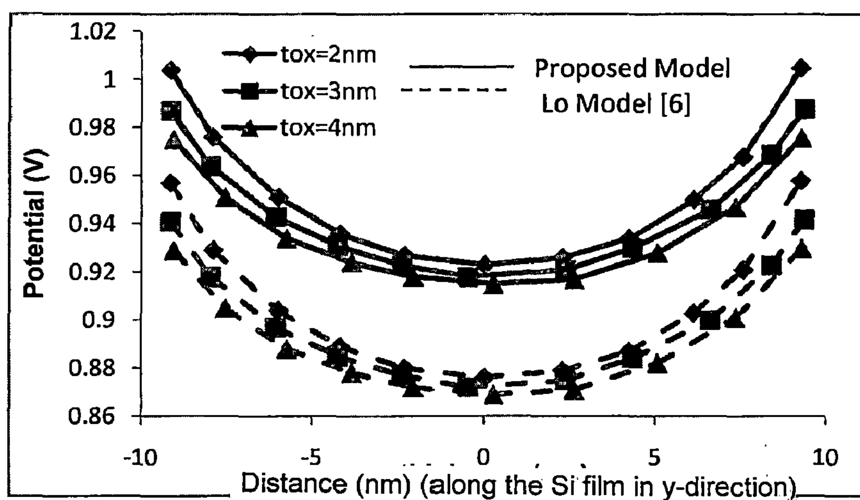
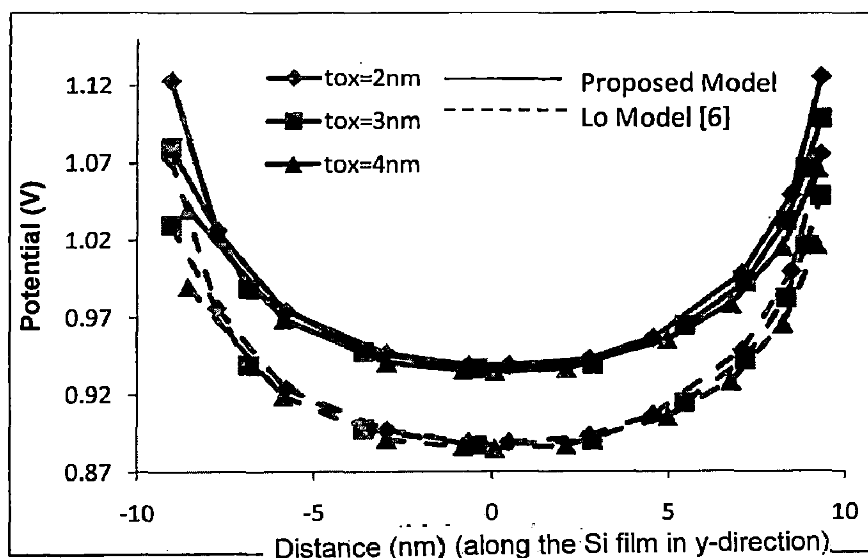


(a)

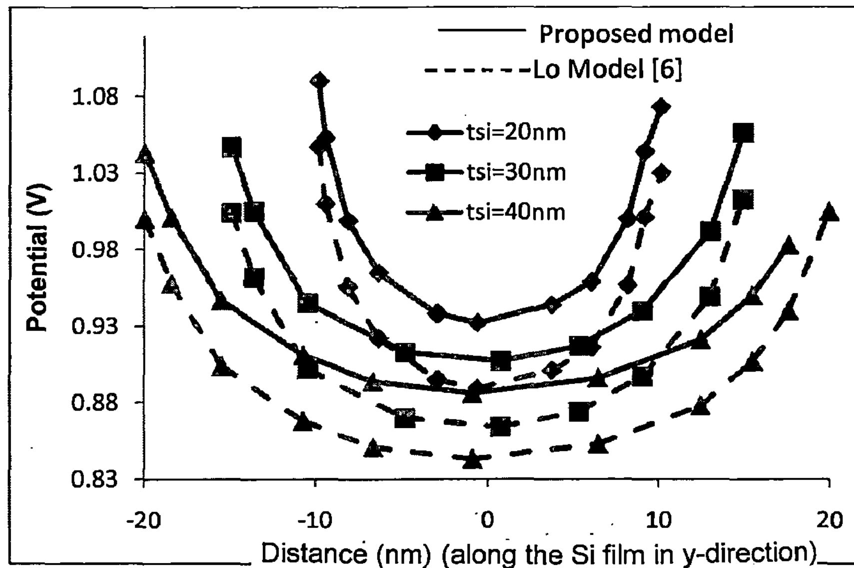


(b)

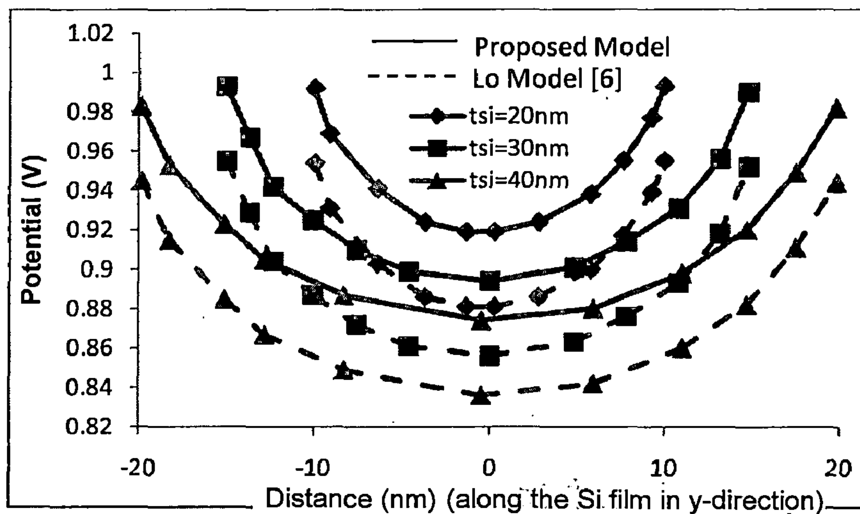
Figure.4.2: Comparison of the Lo [6] and proposed analytical potential model for the DG-MOSFET .Where $t_{si} = 20nm$ and $N_a = 10^{17}cm^{-3}$ (a) $V_{gs} = 0.1V$ and (b) $V_{gs} = 1.0V$

It can be seen that parabolic nature of the curve is maintained. The curves in this case shifted downwards with increasing gate oxide thickness because of decrease in magnitude of Normal electric field.

Fig.4.3 shows potential variation along the Si thickness with varying Si film thickness values. The values of other parameters are gate oxide thickness$t_{ox} = 2nm$, gate bias voltage $V_{gs} = 0.1V$ [Fig.4.3(a)]and $V_{gs} = 1.0V$ [Fig.4.3(b)] and doping concentration $N_a = 10^{17}cm^{-3}$.



(a)

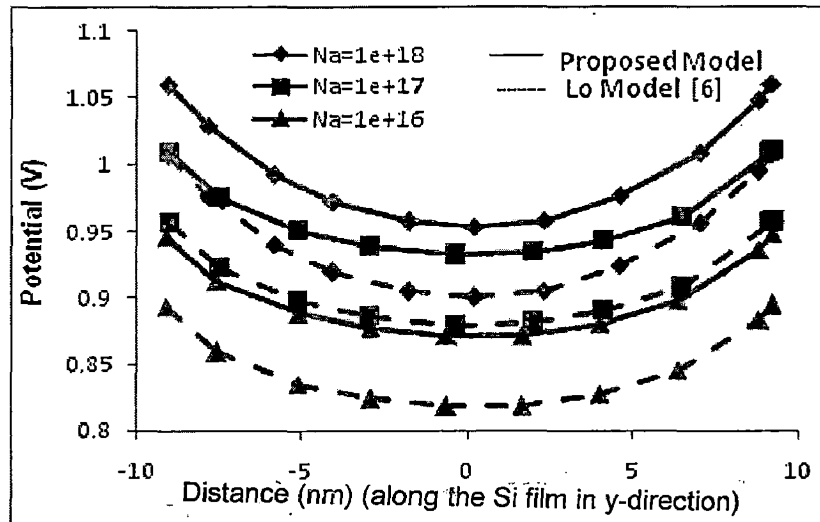


(b)

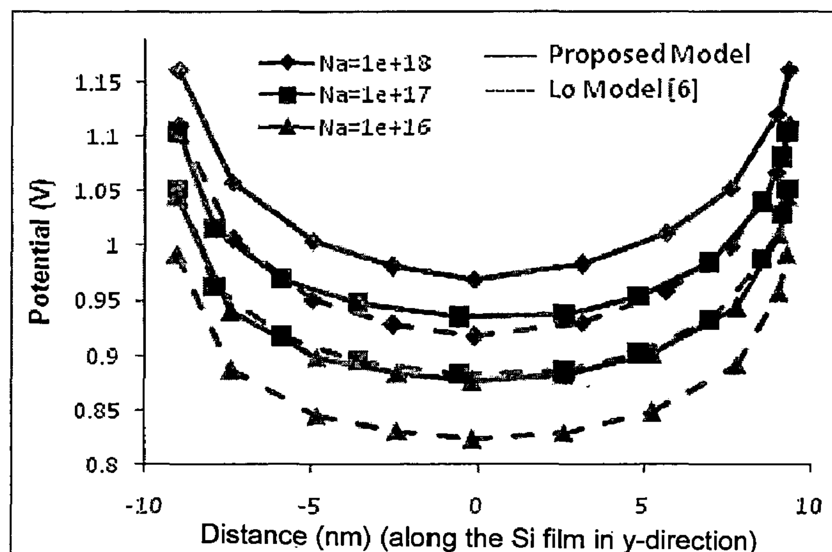
Figure4.3: Comparison of the Lo [6] and proposed analytical potential model for the DG-MOSFET . Where $t_{ox} = 2nm$ and$N_a = 10^{17}cm^{-3}$ (a) $V_{gs} = 0.1V$ and (b) $V_{gs} = 1.0V$

As we increase the silicon film thickness, it can be observed that the potential distribution curves are becoming wider which is true for obvious reasons. The curves are shifting upwards for increasing values of gate bias voltages.

Fig.4.4 shows the potential variation along the Si thickness for different channel doping concentration values, $N_a = (10^{16}cm^{-3}, 10^{17}cm^{-3}, 10^{18}cm^{-3})$. The values of other parameters are: gate oxide thickness$t_{ox} = 2nm, t_{si} = 20nm$ and gate bias voltage $V_{gs} = 0.1V$ in part (a) and $V_{gs} = 1.0V$ in part (b).



(a)



(b)

Figure 4.4: Comparison of the Lo [6] and proposed analytical potential model for the DG-MOSFET. Where$t_{ox} = 2nm$, $t_{si} = 20nm$ (a) $V_{gs} = 0.1V$ and (b) $V_{gs} = 1.0V$

Potential profile shows an increase with increase in doping concentration, which is intern due to an increase in the number of free carriers in the channel region. Our proposed potential model variation with different parameter in [fig.(4.1),(4.2),(4.3)and (4.4)] is deflected 4-6% with existing model.

4.2. Surface Potential Variation along the Channel

Fig.4.5 shows the Surface potential Φ(x, 0) as a function of the normalized position along the channel for different drain bias voltages; V_{ds} = (0.5,1.0 and 1.5V). The values of other parameters are: gate oxide thickness, $t_{ox} = 2nm$, Si film thickness, $t_{si} = 20nm$ and gate bias voltage $V_{gs} = 0.2V$

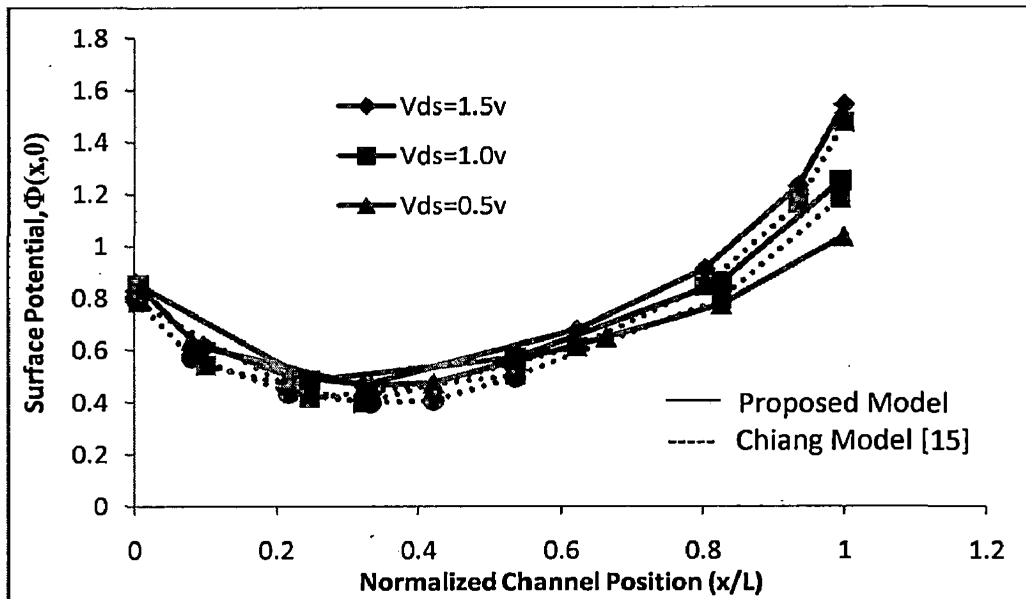


Figure 4.5: Comparison of the Chiang [15] and proposed model for the DG-MOSFET. Where $t_{ox} = 2nm$, $t_{si} = 20nm$ and $V_{gs} = 0.2V$

In the figure, position of minima has been iteratively found and it can be observed that the shift in the point of the minimum potential is almost fixed regardless of the applied drain bias.

The minimum Surface potential variation along the gate bias voltage for different channel length L = (10, 25,100nm) is shown in Fig.4.6. The values of other parameters are: gate oxide thickness$t_{ox} = 5nm$, Si film thickness, $t_{si} = 20nm$, drain bias voltage $V_{ds} = 0.05V$ and channel doping concentration $N_a = 10^{16}cm^{-3}$

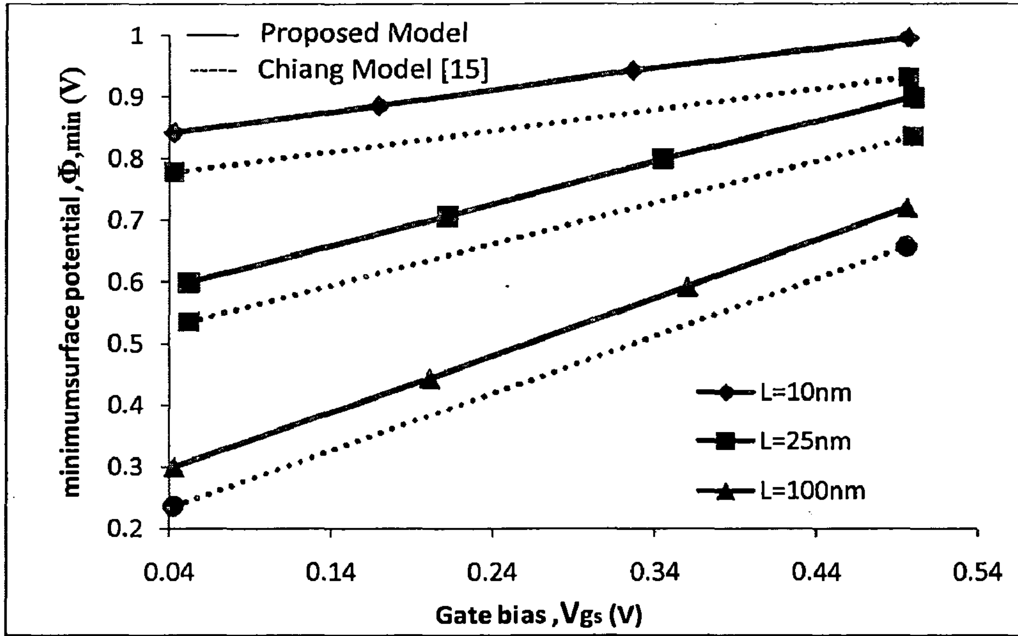


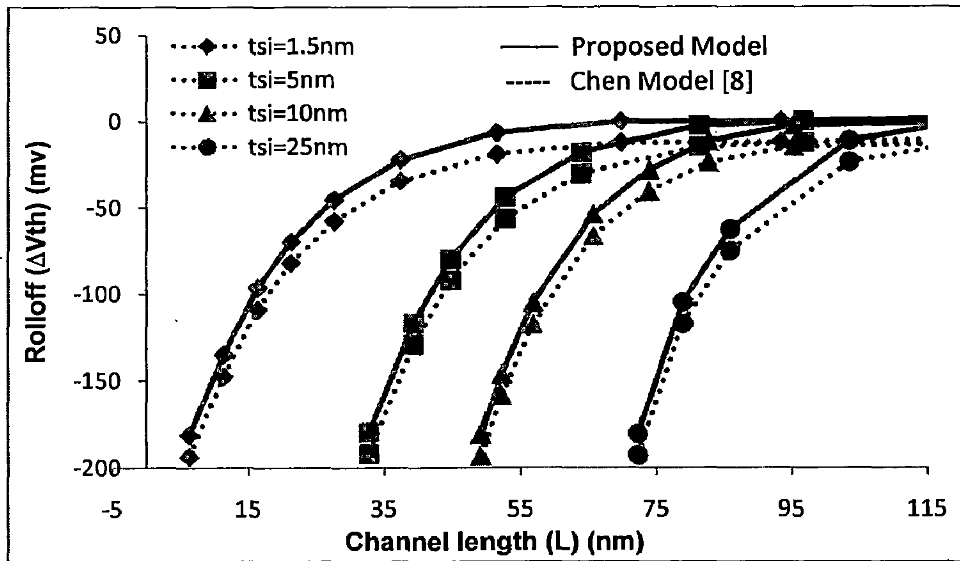
Figure 4.6: Comparison of the Chiang [15] and proposed model for the DG-MOSFET. Where$V_{ds} = 0.05V$, $t_{si} = 20nm$, $t_{ox} = 5nm$ and$N_a = 10^{16}cm^{-3}$.

If we increase the gate bias voltage, then the minimum surface potential increases due to an increase in the electric field both in longitudinal and lateral directions of the device. As the lateral Electric field varies the gate length (inversely proportional), hence for increasing device lengths, we observe a decrease in minimum surface potential curves. It can be seen that the smallest channel length of L=10nm has the least slope in the above graph.

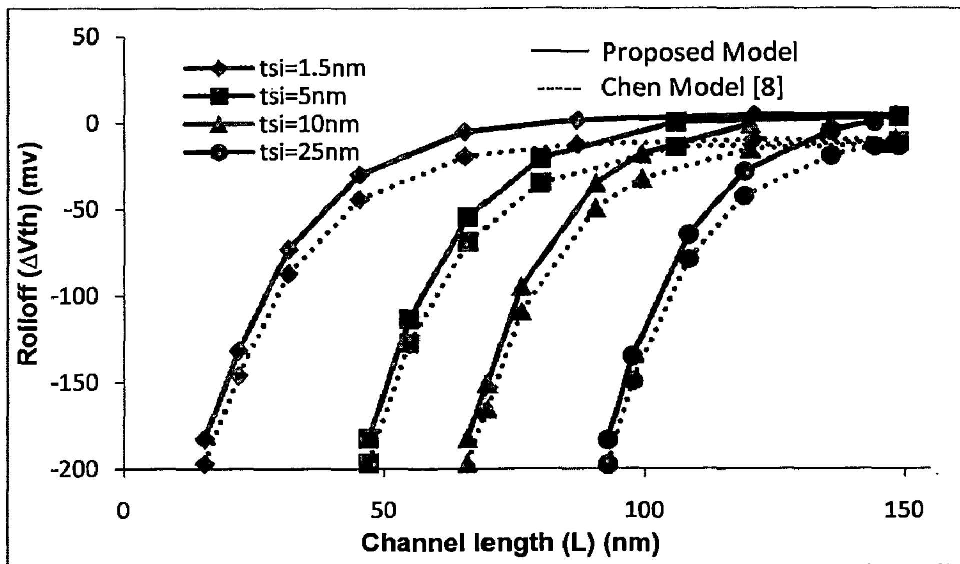
The subthreshold slope swing is inversely proportional to $\frac{\partial \Phi_{1,min}}{\partial V_{gs}}$. It can be concluded that as the channel length of the device is reduced, $\frac{\partial \Phi_{1,min}}{\partial V_{gs}}$, decreases and the subthreshold swing will increase. Our proposed minimum surface potential model variation with different parameter in [fig.(4.5)and (4.6)] is error 4-6% with existing model.

4.3. Threshold voltage roll-off Variation along the Channel

Threshold voltage roll-off ΔV_{th}, is the difference between the threshold voltages of short and long channel devices. The variation of threshold voltage roll-off along the channel length for different silicon film thickness t_{si}= (1.5,5,10,and 25nm) is shown in Fig.4.7. The values of other parameters are: Gate oxide thickness $t_{ox} = 1nm$[in part(a)] and $t_{ox} = 1.5nm$ [in part(b)]. $V_{ds} = 0.05V$.



(a)



(b)

Figure 4.7: Comparison of the Chen [8] and proposed model for the DG-MOSFET. (a) $t_{ox} = 1nm$ and (b) $t_{ox} = 1.5nm$

As can be observed from the above graphs, threshold voltage roll-off ΔV_{th} is sensitive to devices parameters like channel length, gate oxide thickness, Si film thickness, channel doping concentration and drain bias voltage. It can be seen that as the channel length of the device is decreased, the threshold voltage roll-off increases. Also, as the thickness of

Si film increases, threshold voltage roll-off also increases as it is directly promotional to it.

In Fig.4.8, we have shown the variation of threshold voltage roll-off along the channel length for different drain bias voltages V_{ds}=(0.005,1.0V). The values of other parameters are: gate oxide thickness $t_{ox} = 1.5nm$ and silicon film thickness $t_{si} = 10nm$.

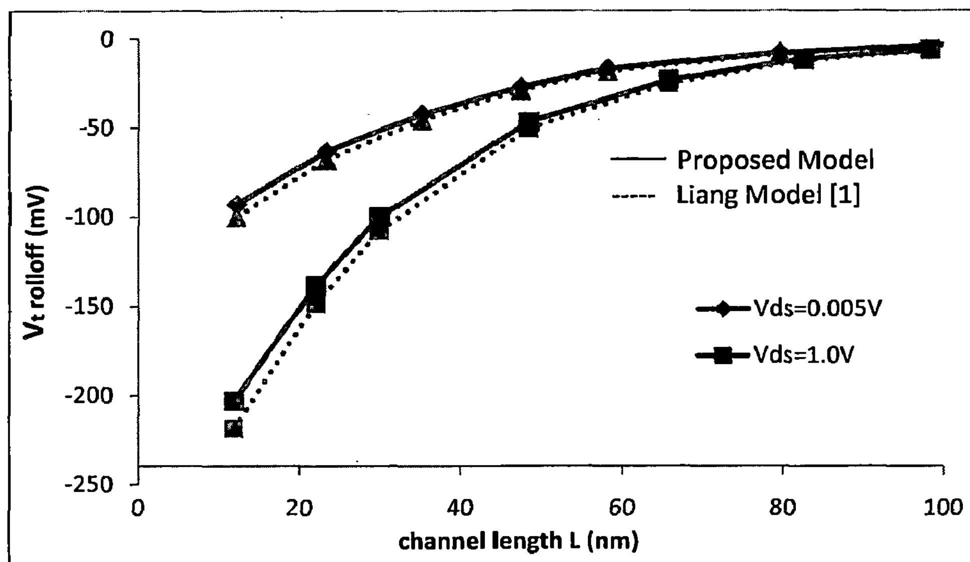


Figure 4.8: Comparison of the Liang [1] and proposed model for the DG-MOSFET. $t_{si} = 10nm$ and $t_{ox} = 1.5nm$

Above figure shows the threshold voltage roll-off ΔV_{th} for both low drain and high drain bias voltages. It can be observed that for higher drain bias, the roll-off is also higher. This is due to the fact that for a fixed high drain bias voltage, the shift in threshold voltage is higher for a long channel device as compared to the short channel device. Our proposed threshold voltage model variation with different parameter in [fig.(4.7)and (4.8)] is error 5-7% with existing model.

In the summary of this chapter, we can state that, our model developed by using Green's function for a DGMOSFET has shown satisfactory results. In the next chapter, we present various conclusions that can be drawn when we compare our model with the existing models.

CHAPTER 5

CONCLUSIONS

In this thesis, analytical model has been developed for the analysis of DG-MOSFET based upon Green's function techniques.

Analytical model of the potential distribution along Si thickness, surface potential along the channel and of threshold voltage in a DG-MOSFETs device has been developed by solving the 2-D Poisson's equation using a Green's function method. The conclusions are:

1) The 2D surface potential and potential distribution along Si thickness model assumed a uniform channel doping profile due to the presence of the two symmetric gate materials with the finite work function and the controllable gate length. Our proposed potential model is in error of 4-7% with existing chiang model.
2) The minimum surface potential point can be found only by iterative method. Shift in the surface channel potential minima position is negligible with the increasing drain bias..
3) The potential distribution along front gate to back gate (perpendicular to channel) is parabolic type, meeting the shape recommended by most models.
4) The analytical threshold voltage model has been derived based on the surface potential model. The threshold voltage roll-off with decreasing channel length in DGMOSFETs down to 100nm.
5) The developed models righty describes the effects of various DGMOSFET parameter variations like body doping concentration, applied drain and gate bias voltage, the thickness of the Si film and gate oxide.
6) The main advantage of these models is that if we can develop a model for any arbitrary doping profile, no need to develop a new model from scratch. Just by only changing the doping profile in the explicit model, we will get model for that particular profile. So this model saves the time in calculating some complex expressions.

SCOPE FOR FUTUER WORK

Several possible extensions could be attempted as ongoing research work. Some specific recommendations based on the present work are as follows:

1. The proposed structures can be applied at the circuit level (e.g. inverter) and the performance of the resulting circuit can be compared with a circuit that is composed of the compatible conventional structures.
2. The cylindrical GAA MOSFET is inherently a 3D device, therefore above approach can be use in analytical modeling of Gate All Around (GAA) DG-MOSFET.
3. The FinFET configuration is another next generation device type which could have the potential to fit into the modeling framework presented here in this thesis. Same approach can be use in a FinFET analytical modeling.

APPENDIX

Green's functions in Rectangular region

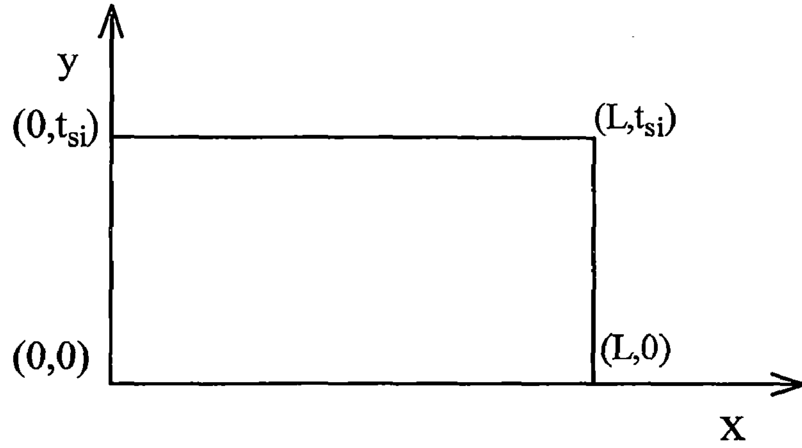


Fig.5.1 rectangular region

Determination of Eigen function and Eigen value in x direction (along the channel)

$$\frac{d^2\Phi}{dx^2} + k_n\Phi = 0, \qquad \Phi = 0 \text{ at } x = 0, L \qquad \text{(A)}$$

$$\Phi = A\sin k_n x + B\cos k_n x$$

$$\Phi = 0, \quad \text{at } x = 0 \Rightarrow B = 0$$

$$\Phi = 0, \text{at } x = L \Rightarrow \sin k_n L = 0$$

Eigen value is $\quad k_n = \frac{n\pi}{L}$

and Eigen function is $\sin\frac{n\pi}{L}x$

Similarly Eigen value in y direction (along the Si film thickness)

$$\frac{d^2\Phi}{dy^2} + k_m\Phi = 0 \qquad \Phi = 0 \text{ at } y = 0, t_{si}$$

$$\Phi = C\sin k_m y + D\cos k_m y$$

$$\Phi = 0, \qquad \text{at } y = 0 \Rightarrow C = 0$$

$$\Phi = 0, \qquad \text{at } y = t_{si} \Rightarrow \sin k_m t_{si} = 0$$

Eigen value is $\qquad k_m = \frac{m\pi}{t_{si}}$

and Eigen function $\sin\frac{m\pi}{t_{si}}y$

Along x-direction

Sturm-lioville eq. is

$$\frac{d}{dx}\left[p\frac{d\Phi}{dx}\right] + (q + \sigma\lambda)\Phi = 0 \tag{B}$$

Where λ is a separation constant. P and σ is usually positive & continuous function of x.

Compare (A) and (B) q=0, $\sigma = 1$

$$\int_0^L \sigma\Phi_n \Phi_m dx = 1 \;, \qquad m = n \tag{5.1}$$

$$= 0, \qquad m \neq n$$

Eigen function $\sin(\frac{n\pi}{L}x)$

$$\int_0^L \sin\left(\frac{n\pi}{L}x\right)\sin\left(\frac{m\pi}{L}x\right)dx = \frac{L}{2} \qquad \text{if } m = n \tag{5.2}$$

$$\int_0^L sin^2\left(\frac{n\pi}{L}x\right)dx = \frac{L}{2}$$

$$\int_0^L \sqrt{\frac{2}{L}}\sin\left(\frac{n\pi}{L}x\right)\sqrt{\frac{2}{L}}\sin\left(\frac{n\pi}{L}x\right)dx = 1$$

$$\Phi_n = \sqrt{\frac{2}{L}}\sin\left(\frac{n\pi}{L}x\right) \tag{5.3}$$

$$\text{Let} \qquad G = a_n(y)\Phi_n(x) \tag{5.4}$$

One dimensional green's function is

$$\frac{d^2G}{dx^2} + \lambda G = -\delta(x - x') \tag{5.5}$$

Method -1

$$G = \sum_{n=1}^{\infty} a_n(y)\psi_n(x) = \sum_{n=1}^{\infty} a_n(y)\sqrt{\frac{2}{L}}\sin(\frac{n\pi}{L}x) \tag{5.6}$$

Eq.(5.5) and (5.6)

$$\sum_{n=1}^{\infty}\sqrt{\frac{2}{L}}\,\{-(\frac{n\pi}{L})^2\}\sin(\frac{n\pi}{L}x)+\lambda\sum_{n=1}^{\infty}a_n(y)\sqrt{\frac{2}{L}}\sin(\frac{n\pi}{L}x) = -\delta(x-x') \qquad (5.7)$$

$$\sum_{n=1}^{\infty}a_n(y)\sqrt{\frac{2}{L}}\left\{\lambda-\left(\frac{n\pi}{L}\right)^2\right\}\sin(\frac{n\pi}{L}x) = -\delta(x-x')$$

$$\sum_{n=1}^{\infty}a_n(y)\frac{2}{L}\left\{\lambda-\left(\frac{n\pi}{L}\right)^2\right\}\int_0^L\sin\left(\frac{n\pi}{L}x\right)\sin\left(\frac{m\pi}{L}x\right)dx = -\int_0^L\sqrt{\frac{2}{L}}\delta(x-x')\sin(\frac{m\pi}{L}x)dx$$

$$a_n(y)\frac{2}{L}\left\{\lambda-\left(\frac{n\pi}{L}\right)^2\right\}\frac{L}{2} = \sqrt{\frac{2}{L}}\sin\left(\frac{m\pi}{L}x'\right)$$

$$a_n(y) = \frac{\sqrt{\frac{2}{L}}\sin\left(\frac{m\pi}{L}x'\right)}{\left\{\lambda-\left(\frac{n\pi}{L}\right)^2\right\}} \qquad (5.8)$$

$$G(x,x') = \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin\left(\frac{n\pi}{L}x\right)\sin\left(\frac{m\pi}{L}x'\right)}{\left\{\lambda-\left(\frac{n\pi}{L}\right)^2\right\}} \qquad (5.9)$$

Green's function in two dimensional is

$$G(x,y;x',y') = \sum_{n=1}^{\infty}a_n(y)\Phi_n(x) \qquad (5.10)$$

$$\Rightarrow \quad \sum_{n=1}^{\infty}\left[\frac{d^2a_n(y)}{dy^2}-\left(\frac{n\pi}{L}\right)^2a_n(y)\right]\Phi_n(x) = -\delta(x-x')\,\delta(y-y') \qquad (5.11)$$

$$\Rightarrow \quad \sum_{n=1}^{\infty}\left[\frac{d^2a_n(y)}{dy^2}-\left(\frac{n\pi}{L}\right)^2a_n(y)\right]\int_0^L\Phi_n(x)\,\Phi_m(x)\,dx = -\delta(y-y')\int_0^L\Phi_m(x)\,\delta(x-x')\,dx$$

$$\frac{d^2a_n(y)}{dy^2}-\left(\frac{n\pi}{L}\right)^2a_n(y) = -\Phi_m(x')\delta(y-y') \quad \{ \quad \text{if } m=n$$

$$\int_0^L\Phi_n(x)\Phi_m(x)dx = 1$$

$$\Phi_1(y) = \sinh\left(\frac{n\pi y}{L}\right)$$

$$\Phi_2(y) = \sinh\frac{n\pi(t_{si}-y)}{L}$$

Therefore

$$W = \Phi_1(y)\Phi_2'(y) - \Phi_2(y)\Phi_1'(y) \quad (5.12)$$

$$W = \sinh\left(\frac{n\pi y}{L}\right)\left\{-\frac{n\pi}{L}cosh\frac{n\pi(t_{si}-y)}{L}\right\} - \sinh\frac{n\pi(t_{si}-y)}{L}\left\{\frac{n\pi}{L}cosh\frac{n\pi y}{L}\right\} \quad (5.13)$$

$$W = -\frac{n\pi}{L}\left[\sin\left(\frac{n\pi y}{L} + \frac{n\pi t_{si}}{L} - \frac{n\pi y}{L}\right)\right]$$

$$W = -\frac{n\pi}{L}\sin\left(\frac{n\pi t_{si}}{L}\right)$$

$$a_n(y) = \frac{-\Phi_n(x')\Phi_1(y_<)\Phi_2(y_>)}{p(y')W(y')} \quad (5.14)$$

Let $p(y') = 1$

And $y_< \equiv$ the greater of x & x'

$y_> \equiv$ the smaller of x & x'

Therefore in above equation

$$a_n(y) = -\sqrt{\frac{2}{L}}\frac{\sin\left(\frac{n\pi x'}{L}\right)\sinh\left(\frac{n\pi y_<}{L}\right)\sinh\frac{n\pi(t_{si}-y')}{L}}{\frac{n\pi}{L}\sinh\left(\frac{n\pi t_{si}}{L}\right)} \quad (5.15)$$

Put these value in equation (5.10)

$$G_x(x, y;\ x', y') = \sum_{n=1}^{\infty}\frac{2}{n\pi}\frac{\sin\left(\frac{n\pi x'}{L}\right)\sin\left(\frac{n\pi x}{L}\right)\sinh\left(\frac{n\pi y}{L}\right)\sinh\frac{n\pi(t_{si}-y')}{L}}{K_n\sinh\left(\frac{n\pi t_{si}}{L}\right)}$$

$$G_x(x, y;\ x', y') = \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin\left(\frac{n\pi x'}{L}\right)\sin\left(\frac{n\pi x}{L}\right)\sinh\left(\frac{n\pi y}{L}\right)\sinh\frac{n\pi(t_{si}-y')}{L}}{K_n\sinh\left(\frac{n\pi t_{si}}{L}\right)} \quad (5.16)$$

$$G_x(x, y;\ x', y') = \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(k_n x')\sin(k_n x)\sinh(k_n y)\sinh k_n(t_{si}-y')}{K_n\sinh(k_n t_{si})} = G_x^{\,1} \quad \text{for } y < y'$$

$$G_x(x, y;\ x', y') = \frac{2}{L}\sum_{n=1}^{\infty}\frac{\sin(k_n x')\sin(k_n x)\sinh(k_n y')\sinh k_n(t_{si}-y)}{K_n\sinh(k_n t_{si})} = G_x^{\,2} \quad \text{for } y > y'$$

Therefore write Green's function

$$G_x = u(y - y')G_x^{\,2} + u(y' - y)G_x^{\,1} \quad (5.17)$$

Where u(y - y') & u(y' - y) is unit step function.

Similarly find in y direction green's function

$$\frac{d^2G}{dy^2} + \lambda_y G = -\delta(y - y') \qquad \text{One dimensional}$$

$$\Phi_m = \sqrt{\frac{2}{t_{si}}}\sin\left(\frac{m\pi}{t_{si}}y\right)$$

Similar to eq.(4.3)

And two dimensional green's function in y-direction

$$G(x, y; x', y') = \sum_{m=1}^{\infty} a_m(x)\Phi_m(y) \qquad (5.18)$$

$$\Rightarrow \quad \sum_{m=1}^{\infty}\left[\frac{d^2a_m(x)}{dx^2} - \left(\frac{m\pi}{t_{si}}\right)^2 a_m(x)\right]\Phi_m(y) = -\delta(x - x')\,\delta(y - y')$$

$$\Rightarrow \sum_{m=1}^{\infty}\left[\frac{d^2a_m(x)}{dx^2} - \left(\frac{m\pi}{t_{si}}\right)^2 a_m(x)\right]\int_0^{t_{si}}\Phi_n(y)\,\Phi_m(y)\,dy = -\delta(x - x')\int_0^{t_{si}}\Phi_n(y)\,\delta(y - y')dy$$

$$\frac{d^2a_m(x)}{dx^2} - \left(\frac{m\pi}{t_{si}}\right)^2 a_m(x) = -\Phi_n(y')\,\delta(x - x') \qquad \{ \quad \text{if } m = n$$

$$\int_0^{t_{si}}\Phi_n(y)\Phi_m(y)\,dy = 1$$

$$\Phi_1(x) = \sinh\left(\frac{m\pi x}{t_{si}}\right)$$

$$\Phi_2(x) = \sinh\frac{m\pi(L-x)}{t_{si}}$$

Therefore

$$W = \Phi_1(x)\Phi_2'(x) - \Phi_2(x)\Phi_1'(x) \qquad (5.19)$$

$$W = \sinh\left(\frac{m\pi x}{t_{si}}\right)\left\{-\frac{m\pi}{t_{si}}\cosh\frac{m\pi(L-x)}{t_{si}}\right\} - \sinh\frac{m\pi(L-x)}{t_{si}}\left\{\frac{m\pi}{t_{si}}\cosh\frac{m\pi x}{t_{si}}\right\}$$

$$W = -\frac{m\pi}{t_{si}}\sin\left(\frac{m\pi L}{t_{si}}\right)$$

$$a_m(x) = \frac{-\Phi_n(y')\Phi_1(x_<)\Phi_2(x_>)}{p(x')W(x')}$$

Let $p(x')=1$

And $x_{<} \equiv$ the greater of y & y'

$x \equiv$ the smaller of y & y'

Therefore in above equation

$$a_m(x) = -\sqrt{\frac{2}{t_{si}}} \frac{\sin\left(\frac{m\pi y'}{t_{si}}\right)\sinh\left(\frac{m\pi x_{<}}{t_{si}}\right)\sinh\frac{m\pi(L-x')}{t_{si}}}{\frac{m\pi}{t_{si}}\sinh\left(\frac{m\pi L}{t_{si}}\right)} \quad (5.20)$$

Put these value in equation (5.18)

$$G_y(x,y;\ x',y') = \sum_{m=1}^{\infty}\frac{2}{m\pi}\frac{\sin\left(\frac{m\pi y}{t_{si}}\right)\sin\left(\frac{m\pi y'}{t_{si}}\right)\sinh\left(\frac{m\pi x}{t_{si}}\right)\sinh\frac{m\pi(L-x')}{t_{si}}}{\sinh\left(\frac{m\pi L}{t_{si}}\right)} \quad (5.21)$$

$$G_y(x,y;\ x',y') = \frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sin(k_m y')\sinh(k_m x)\sinh k_m(L-x')}{k_m\sinh(k_m L)} = G_y^{\ 1} \qquad \text{for } x < x'$$

$$G_y(x,y;\ x',y') = \frac{2}{t_{si}}\sum_{m=1}^{\infty}\frac{\sin(k_m y)\sin(k_m y')\sinh(k_m x')\sinh k_m(L-x)}{k_m\sinh(k_m L)} = G_y^{\ 2} \qquad \text{for } x > x'$$

Therefore

$$G_y = u(x - x')G_y^{\ 2} + u(x' - x)G_y^{\ 1} \quad (5.22)$$

Where $u(x - x')$ & $u(x' - x)$ is unit step function.

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