# DESIGN OF SWITCHED CAPACITOR BASED LOW PASS SIGMA DELTA MODULATOR

**A DISSERTATION**

***Submitted in partial fulfillment of the requirements for the award of the degree of***

MASTER OF TECHNOLOGY

*in*

ELECTRONICS AND COMPUTER ENGINEERING

With Specialization in Semiconductor Devices and VLSI Technology)

*By*

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## CANDIDATE'S DECLARATION

I hereby declare that the work, presented in this dissertation, entitled, **"DESIGN OF SWITCHED CAPACITOR BASED LOW PASS SIGMA DELTA MODULATOR"** is submitted in partial fulfillment of the requirements of the award of degree **MASTER OF TECHNOLOGY** in Electronics and Computer Engineering, with the specialization in Semiconductor Devices and VLSI Technology submitted to the department of Electronics and Computer Engineering, IIT Roorkee (India) is an authentic record of my own, carried out under the guidance of Dr. A. K. Saxena, Professor, E&C Dept., Dr. S. Dasgupta, Assistant Professor, E&C Dept., IIT Roorkee (India).

The matter presented in this dissertation report has not been submitted by me for award of any other degree or diploma in any institute.

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Place: Roorkee

## CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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# ABSTRACT

The need to develop cost effective high resolution converters which can be integrated on the same chip along with the digital circuits led to the use of sigma-delta modulator (ΣΔM). For the on-chip integration of these modulators design of ΣΔM at low supply voltages becomes necessary.

In audio and biomedical applications, low pass ΣΔM is used. For implementing these modulators, Switched Capacitor (SC) technique is widely used due to its compatibility with the standard CMOS technology its ability to realize accurate signal processing function. The design of these modulators at low supply voltages of 1 V is challenging in terms of analog circuit performance.

The design of low pass second order ΣΔM at low supply voltage of 1 V has been presented in this dissertation. Behavioral modeling of the SC ΣΔM using *SD toolbox* was done and simulated in *Matlab* and *Simulink* environment optimise SNR at architecture level and also to obtain the required circuit level specifications for achieving > 10 bits resolution.

The nonidealities where reduced by proper selection and designing of circuit topologies. Two stage opamp has been used to account for reduction of magnitude and phase error of the integrator transfer function due to finite gain. Integrator has been designed to minimize distortion and charge injection. Dynamic latched comparator has been employed for power reduction. This modulator employs Auto-Zeroed Integrator for operation at high frequencies by eliminating the critical switches.

This can be used to digitize electrical biomedical signals like Electro-cardiogram (ECG), Electroencephalogram (EEG), and Electroretinogram (ERG). The simulated results of the proposed ΣΔM in standard CMOS 0.18 μm technology, using Tanner tools gave about 10 bits resolution for input at 4 kHz and clock frequency of 1 MHz with 1 V power supply.

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| | |
|---|---|
| ΣΔM | Sigma Delta Modulator |
| ΣΔ | Sigma Delta |
| ADC | Analog to Digital Converter |
| AZI | Auto-Zeroed Integrator |
| CMRR | Common Mode Rejection Ratio |
| CT | Continuous Time |
| DAC | Digital to analog converters |
| DR | Dynamic Range |
| DSP | Digital Signal Processors |
| DT | Discrete Time |
| ECG | Electrocardiogram |
| EEG | Electroencephalogram |
| EGG | Electrogastrogram |
| ENOB | Effective Number of Bits |
| ERG | Electroretinogram |
| FOM | Figure Of Merit |
| GBW | Gain Bandwidth |
| ICMR | Input Common Mode Range |
| ITRS | International Technology Roadmap for Semiconductors |
| OSR | Over Sampling Ratio |
| OTA | Operational Transconductance Amplifier |
| PM | Phase Margin |
| PSD | Power Spectral Density |
| PSRR | Power Supply Rejection Ratio |
| SC | Switched Capacitor |
| SI | Switched Current |
| SO | Switched Opamp |
| SNR | Signal to Noise Ratio |
| SDM | Sigma Delta Modulator |
| SD Toolbox | Sigma Delta Toolbox |
| SR | Slew rate |
| VHDL-AMS | VHDL Analog and Mixed Signal |

# Chapter 1
# INTRODUCTION

The real world signals are analog in nature. There is a necessity for these signals to be converted into the digital domain using an Analog to Digital Converter (ADC). This conversion to digital domain is essential as digital processing, transmission and storage of signals is more efficient compared to analog.

The portable electronic systems such as wireless communication devices, consumer electronics and battery powered biomedical devices include an ADC in their circuitry. The use of ADC in battery operated systems places a need to operate ADCs at low powers and low voltages. Thus, the design of ADCs for high speed, high precision and low power dissipation is one of many difficult challenges in analog design.

The technological improvement in digital VLSI circuits has increased the need for low cost high performance A/D (Analog to Digital) and D/A (Digital to Analog) converters, which can be integrated on the same chip with digital circuits. Thus, low voltage, low-power, yet inexpensive VLSIs are getting focus recently.

Sigma-delta modulator (SDM or ΣΔM) has become a usual technique for A/D conversion as it relaxes the anti-alias filter requirement and minimizes the digital noise coupling on chip. It is very suitable for low frequency, high performance and low power application [1].

## 1.1 MOTIVATION

In biomedical instrumentation, biomedical signals such as Electrocardiogram (ECG), Electroencephalogram (EEG), Electrogastrogram (EGG), Electroretinogram (ERG) are analog in nature. These biomedical signals are low frequency signals. The voltage and frequency ranges of some common biomedical signals are shown in Fig. 1 [2]. There is a necessity for biomedical signals to be converted into the digital domain for further analysis and signal processing using either conventional digital computers or special purpose digital signal processors (DSPs).

The need to limit power consumption (and hence, heat dissipation) in very-high density ULSI chips have led to rapid and innovative developments in low-power design during

the recent years. The rules for analog circuits are quite different to those applied to digital circuits. The decreasing supply voltage unfortunately does not reduce the power consumption of analog circuits. This is mainly due to the fact that the power consumption of analog circuits at a given temperature is basically set by the required signal-to-noise ratio (SNR) and the frequency of operation (or the required bandwidth). A first-order analysis also shows that the absolute minimum power consumption required to process analog signals is almost independent of the supply voltage reduction.

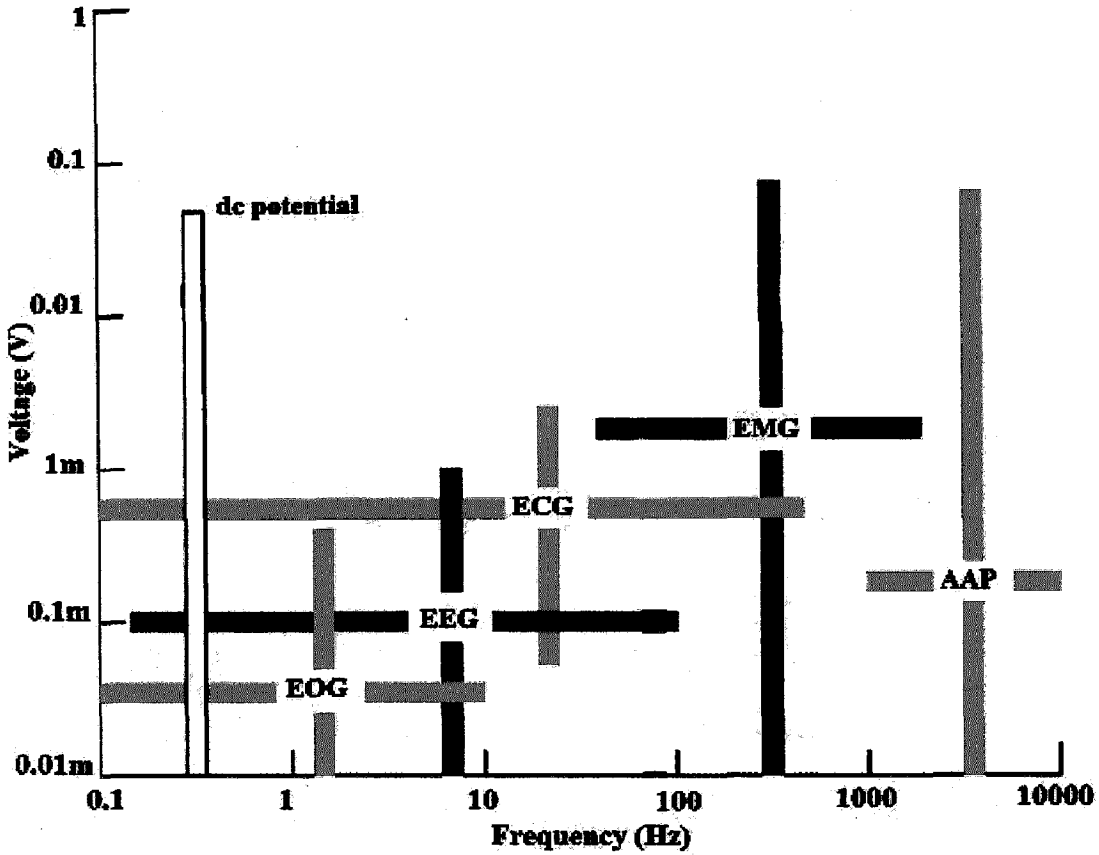



Fig. 1.1 Voltages and Frequency Ranges of Some Common Bio-Potential Signals [2]

The need for precision usually leads to the use of larger dimensions for active and passive components, with a resulting increase in parasitic capacitors and power [3]. Thus, proper selection of ADC architecture can help reduce the power of the biomedical instrument.

As sigma-delta ADC can achieve the highest resolution for relatively low signal bandwidths [1], without use of very precise components due to relaxed anti-alias filter requirement, oversampled sigma-delta converters are ideally suited for biomedical applications. These biomedical applications require ADC with 10 bits resolution. Hence,

design of SDM with about 10 bit resolution which operates at low frequencies of order of 4 kHz was chosen.

## 1.2 PROBLEM DEFINITION

**Circuit Technique used:** In analog circuit design, the voltage or current mode methodologies can be used for signal processing. In the voltage (current) mode design, information is encoded by voltage (current) or its derivatives. The Switched Capacitor (SC) technique has been extensively used in the voltage mode design while Switched Current (SI) techniques in the current mode design. Due to its ability to realize accurate signal processing function SC technique was used.

The CMOS technology is driven by the needs of digital VLSI. The power supply is reduced along with the scaling down to avoid any transistor breakdown as shown in Fig. 1.2. The integrated analog SC circuits must operate at low voltage.

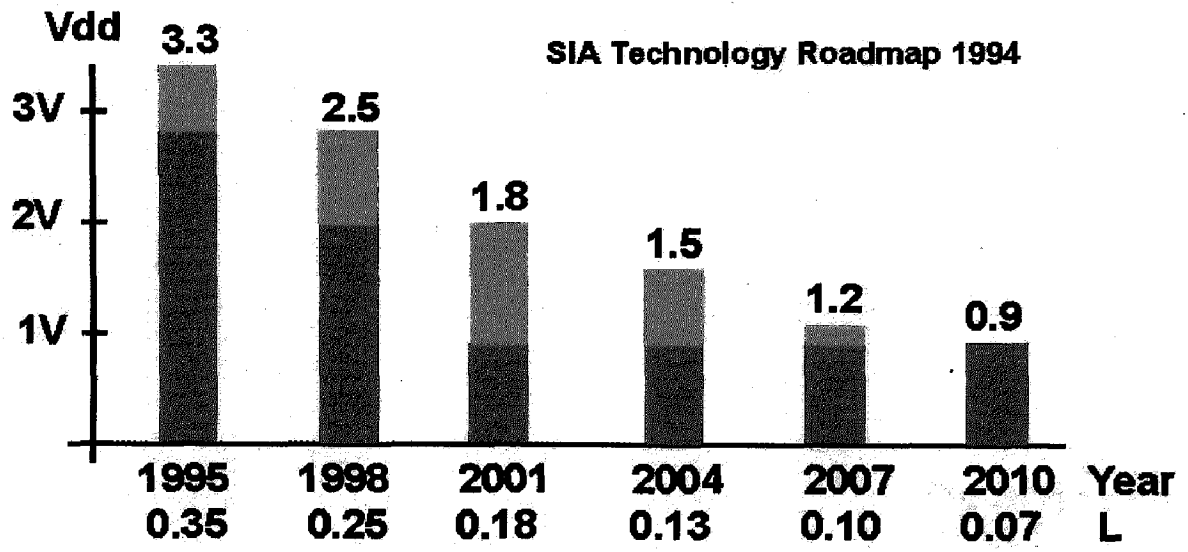



Fig. 1.2 Future of CMOS Voltage Scaling

So, supply voltage of 1 V was chosen to design the SDM in 0.18 μm CMOS technology. For supply voltages below about 1.5 V, the design of these components becomes quite challenging. There are fundamental limitations on the operation of switches when the supply voltage becomes less due to the presence of 'critical switches' in the conventional switched capacitor circuitry.

The fundamental blocks of SC ΣΔMs are SC integrators, ADCs, feedback DACs. SC circuits use MOS switches, op-amps, and capacitors as components which contribute to the nonidealities in the modulator. At low voltages, the nonidealities increase if conventional SC integrator is used in the circuit realisation. Hence, proper selection of SC integrator has to be done at low voltage and high frequencies.
Although Switched Opamp (SO) is used at low supply voltages, it becomes inefficient at high clock frequencies due to the large time needed to switch 'on' and 'off' the opamp. Hence, Auto-Zeroed Integrator (AZI) is more advanced methodology to eliminate critical switches where the switching on and off of the opamp is replaced by switching action of a simple switch.

The thesis presents the design of switched capacitor based sigma delta modulator for low frequency applications. The design of SC sigma delta modulator with reduced nonidealities, by proper selection of modulator architecture and circuit topologies, is the main aim of this thesis.

## 1.3 THESIS ORGANISATION

The organization of the remaining parts of this thesis is as follows:

- **Chapter 2** briefly discusses the limitations of Nyquist rate analog-to-digital (A/D) converter architectures, reviews fundamental concepts and SDM architectures.
- **Chapter 3** discusses the nonidealities present in SC SDM, MATLAB & SIMULINK simulation results for the behavioral model is presented.
- **Chapter 4** provides details about the building blocks of SDM and about topology selection for reducing nonidealities in the modulator.
- **Chapter 5** design procedure for the circuits discussed in Chapter 4 is presented.
- **Chapter 6** shows the T-Spice simulated results for the circuits designed (in 4$^{th}$ Chapter) and the thus designed SC SDM.
- **Chapter 7** concludes the dissertation work and gives suggestions for future work.

# Chapter 2

# ΣΔ ADC ARCHITECTURE & OPERATION

## 2.1 ANALOG TO DIGITAL CONVERTER

An analog-to-digital converter (ADC) converts an analog signal which is continuous in time and amplitude to a digital signal which is discrete in both time and amplitude. Thus, the ADC output is a digital best approximation of its input signal with the approximation error (or quantization error) being related to the ADC resolution. The design of ADCs for high speed, high precision and low power dissipation is one of many difficult challenges in analog design.

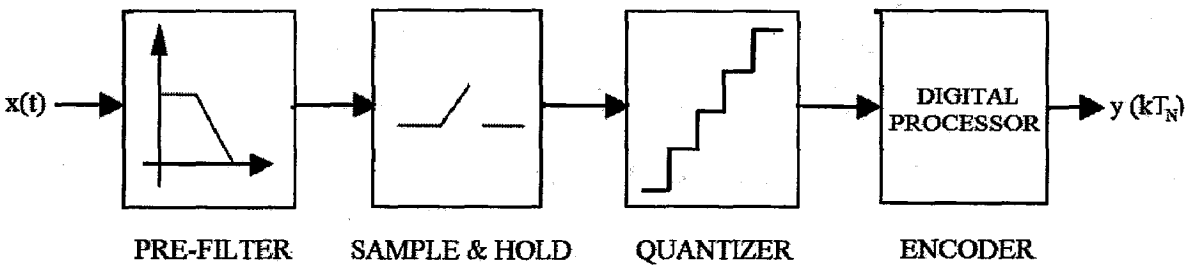



Fig. 2.1 General Block Diagram for an ADC

Fig. 2.1 shows the general block diagram for an ADC. It consists of prefilter, sample and hold, quantizer and encoder blocks. A prefilter also called the anti-aliasing filter avoids the aliasing of higher frequency signal back into the base-band of the ADC. The prefilter is followed by a sample-and-hold circuit that maintains the input analog signal to the ADC constant during the time this signal is converted to an equivalent output digital code. This period of time is called the conversion time of the ADC, which is accomplished by quantization step. The quantizer divides the reference into sub-ranges. Generally, there are $2^N$ sub-ranges, where N is the number of bits of the digital output data. The quantization block finds the sub-range that corresponds to the sampled analog input. Consequently, the encoder i.e., digital processor in the block diagram encodes the corresponding digital bits. Thus, within the conversion time, a sampled analog input signal is converted to an equivalent digital output code.

ADCs can be classified as one of two types: Nyquist-rate or oversampling. Sampling the input signal at rates much higher than the Nyquist rate and shaping the quantization noise results in improved performance.

### 2.1.1 Limitations of Nyquist-Rate A/D Converters

Nyquist-rate converters exhibit two major significant limitations: the anti-alias filter and the quantization noise.

The requirements of an anti-alias filter are

- the passband must accurately pass the desired input signals
- the stop-band must attenuate any interferer outside the passband.

The design of anti-alias filters can be very challenging if out-of-band interferers are both very strong and very near the pass frequency of the desired signal. To meet the severe requirements for filter stop-band and narrowness of the transition band higher order filters are to be used which in may tend to introduce phase distortion at the edge of the passband.

The second limitation of Nyquist-rate converters is the quantization noise. Nyquist-rate data converters use the minimal required sampling frequency, determined by the Nyquist criteria allowing a maximal quantization error which degrades SNR.

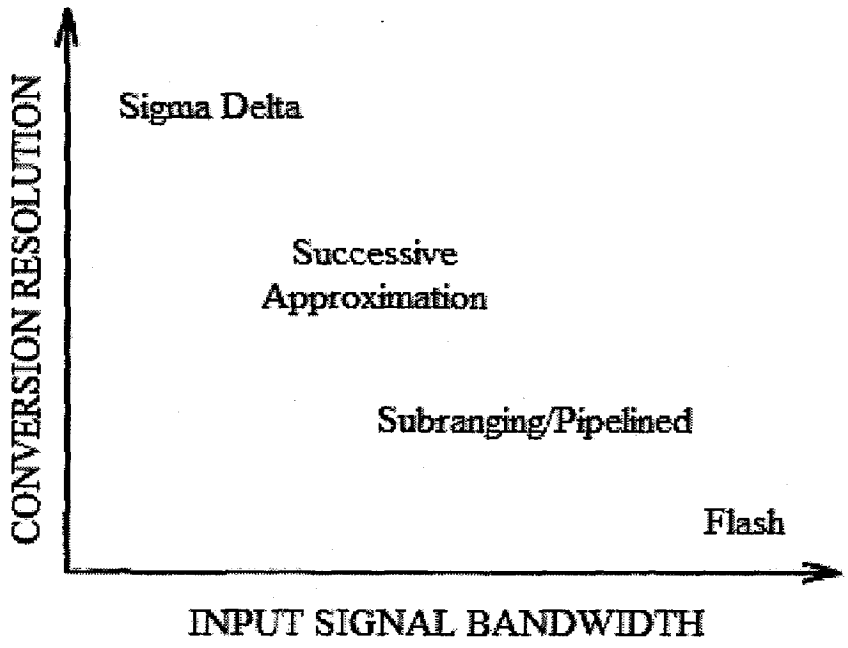



Fig. 2.2 Bandwidth Resolution Tradeoffs [1]

Qualitative bandwidth and resolution tradeoffs of some of the Nyquist-rate A/D techniques, as well as sigma-delta conversion, are shown in Fig. 2.2. Sigma-delta A/D converters attain the highest resolution for relatively low signal bandwidths [1].

### 2.1.2 SIGMA DELTA ADC – a good choice at low frequency applications

The technological improvement in digital VLSI circuits has increased the need for low cost high performance A/D and D/A converters, which can be integrated on the same chip with digital circuits. In order to relax the anti-alias filter requirement and to minimize the digital noise coupling on chip, oversampled sigma-delta converters are used. Hence, ΣΔ ADCs are used in many applications where a low-cost, low-bandwidth, low-power, high-resolution ADC is required. As they can achieve the highest resolution for relatively low conversion speed, it is ideally suited for speech applications and biomedical applications.

## 2.2 FUNDAMENTAL CONCEPTS OF SIGMA DELTA ADC

An oversampling converter has a sampling clock frequency that is much higher than the input signal's Nyquist rate. Oversampling converters are more commonly called delta-sigma converters or charge balancing A/D converters. Sigma-delta converters consist of two major modules: the sigma-delta modulator and the digital filter. With their sampling rate several orders higher than the Nyquist rate, oversampling converter make extensive use of digital signal processing and may eliminate the need for both an analog anti-aliasing filter and a sample and hold cell at the input of the ADC.

### 2.2.1 Block Diagram of 1$^{st}$ Order ΣΔM

The simplest form of ΣΔ modulator combines a low-pass analog filter consisting of a single integrator with an l-bit quantizer.
A block diagram of a first order sigma-delta modulator A/D system is shown in Fig. 2.3. The system consists of an analog sigma-delta modulator, followed by a digital decimator. The modulator consists of an integrator, an internal A/D converter or quantizer, and a D/A converter (DAC) used in the feedback path.

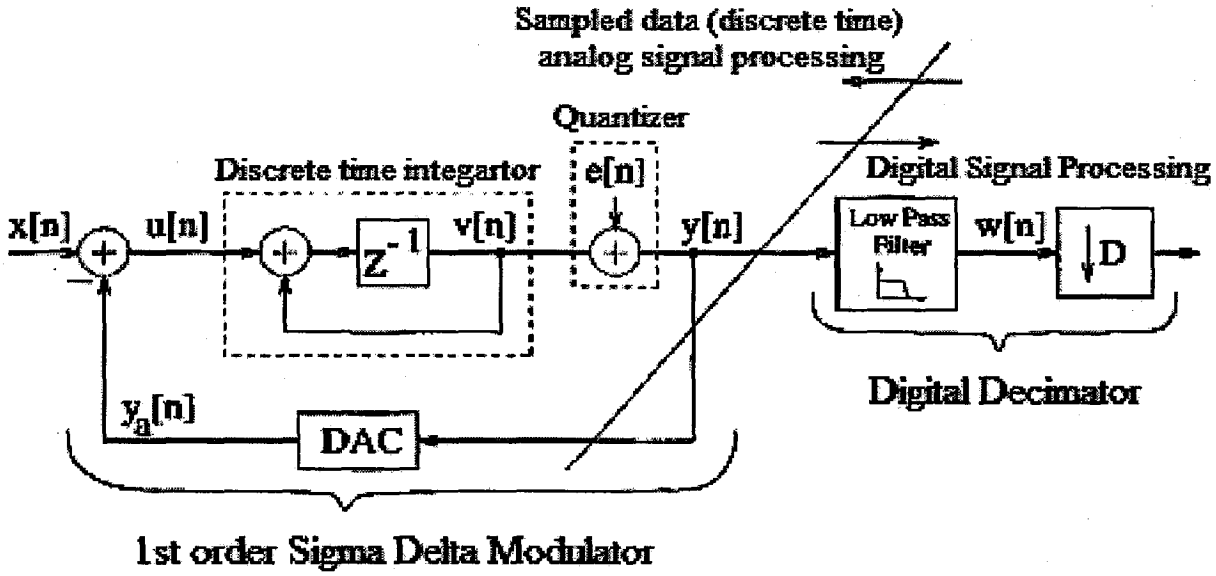



Fig. 2.3 Simple 1st Order Sigma-Delta Modulator A/D System [1]

**Oversampling & Noise Shaping**

Oversampling reduces the quantization noise power in the signal band by spreading a fixed quantization noise power over a bandwidth that is much larger than the signal band, while noise-shaping further attenuates this noise in the signal band and amplifies it outside the signal band.

### 2.2.2 Oversampling

Oversampling theory is based on an exact quantization model that the output quantized signal y(n) is the sum of the input signal value x(n) and the quantization error e(n) which is strongly related to the input signal [1], [4]. For a rapidly and randomly active input signal x(n), r(n) can be assumed to be a statistically uncorrelated white-noise signal leading to an approximate quantizer model with reasonably accurate results.

In an oversampling converter, the same noise power produced as a Nyquist-rate converter is uniformly distributed between $-f_s/2$ and $f_s/2$, where $f_s$ is the sampling frequency. Because fs, is much greater than the signal Nyquist-rate and the overall quantization error energy is constant, only a small fraction of the total noise power falls in the signal band, which is given by [4]

$$P_E = \int_{-f_b}^{f_b} \left( \frac{\Delta^2}{12} \frac{1}{f_s} \right) df = \frac{\Delta^2}{12} \frac{2f_b}{f_s} = \frac{\Delta^2}{12} \frac{1}{OSR} \qquad (2.1)$$

where OSR is the oversampling ratio, defined as the ratio between $f_s$ and $2f_b$, $f_b$ is the signal bandwidth. $\Delta^2/12$ is actually the quantization noise power of a Nyquist converter where $\Delta$ is the quantizer step size.

For an N-bit quantizer with $2^N$ quantization levels, the maximum signal power is

$$P_S = \left(\frac{2^N \Delta}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 . 2^N}{8} \tag{2.2}$$

Thus the ratio of an oversampling converter is given by

$$SNR_{max} = 10\log\left(\frac{P_S}{P_E}\right) = 6.02N + 1.76 + 10\log\,(OSR) \tag{2.3}$$

The last term in the RHS of the eq. (2.3) is SNR increment due to the oversampling, while the sum of the first two terms represents the SNR resulting from an N-bit quantizer. Increasing the quantizer bit-resolution N and the oversampling ratio OSR results in an enhanced SNR. However, when taking the advantage of the inherent linearity of a 1-bit quantizer (N = 1), the oversampling alone usually cannot make the SNR high enough with a practical sampling rate. For efficiency, noise-shaping needs to be introduced to achieve a high resolution.

### 2.2.3 Noise Shaping

Using the feedback loop configuration illustrated in Fig. 2.3, noise-shaping in a SD modulator increases the baseband signal-to-noise ratio by virtue of attenuating quantization noise at low frequencies.

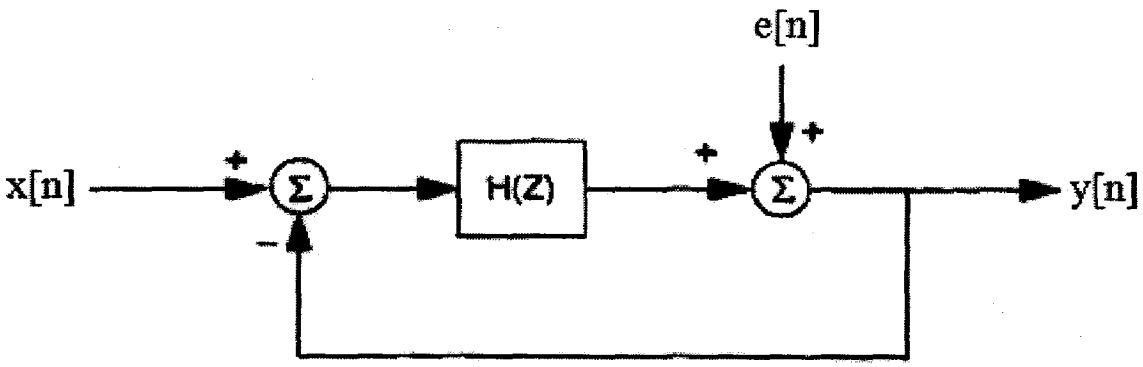



Fig. 2.4 Modulator Linear Model [2]

Figure 2.4 illustrates a linearized z-domain model of a sigma delta modulator [1], [2]. The model assumes that the quantization error can be modelled as additive white noise, with properties that it is independent of the input, uniformly distributed in [-Δ/2, Δ/2] where Δ is the step size of the quantizer, and has a at (white) power spectral density. Thus, this quantization error or noise, denoted e[n], can be decoupled from the input and represented as an additional input to the system.

Using the approximation of the quantization noise, the output of the modulator $Y(z)$ can be expressed as

$$Y(z) = STF(z).U(z) + NTF(z).E(z) \tag{2.4}$$

where $STF(z)$ is the signal transfer function and $NTF(z)$ is the noise transfer function. Solving Equation (2.2) for the $STF(z)$ and $NTF(z)$, and expressing them in terms of the $H(z)$ yields

$$STF(z) = \left.\frac{Y(z)}{U(z)}\right|_{E(Z)\equiv 0} = \frac{H(z)}{1+H(z)} \tag{2.5}$$

and

$$NTF(z) = \left.\frac{Y(z)}{E(z)}\right|_{U(z)\equiv 0} = \frac{1}{1+H(z)} \tag{2.6}$$

Equation (2.6) illustrates that, if $H(z)$ is a low pass function the quantization noise is shaped by a high-pass type function. By proper design of the modulator, most of the quantization noise can be removed from the signal band. By increasing the order of the loop filter $H(z)$, more of the quantization noise is removed from the signal band.

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate ($Kf_s$) and still satisfy the Nyquist criterion, from Fig. 2.5. This may be achieved by passing every $M^{th}$ result to the output and discarding the remainder. The process is known as "decimation" by a factor of M. Decimation does not cause any loss of information [3]. If we simply use over sampling to improve resolution, we must over-sample by a factor of $2^{2N}$ to obtain an N-bit increase in resolution. The Sigma Delta converter does not need such a high over sampling ratio because it not only

limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband.

The ΣΔ converter does not need such a high oversampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband as shown in Fig. 2.5C.

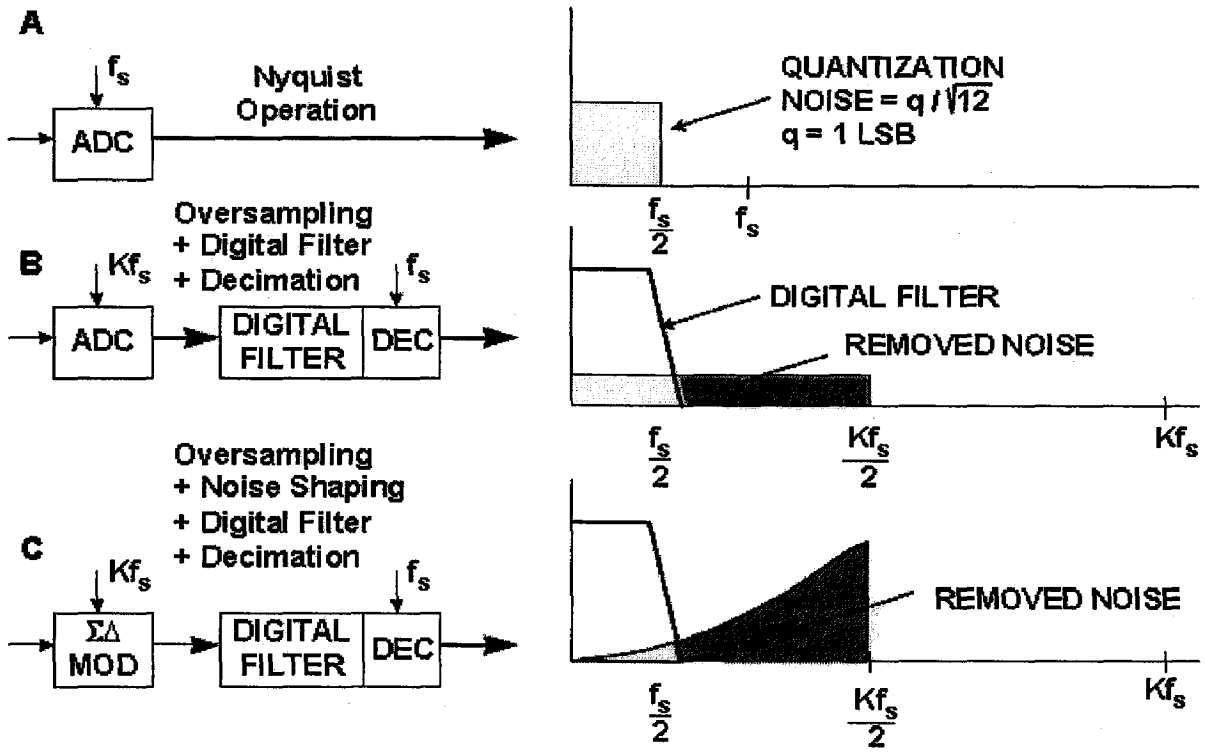



Fig. 2.5 Oversampling, Digital Filtering, noise Shaping and Decimation [5]

By using more than one integrator and summing stage in the ΣΔM, we can achieve higher orders of quantization noise shaping for a given over-sampling ratio as is shown in Fig. 2.6.

Figure 2.7 shows the relationship between the order of the SD modulator and the amount of over-sampling necessary to achieve a particular SNR. For instance, if the OSR is 64, an ideal second-order system is capable of providing an SNR of about 80dB. This implies approximately 13 effective number of bits (ENOB) [5].
Thus shaping the quantization noise through the use of feedback is often used to achieve a converter resolution up to 20 bits.

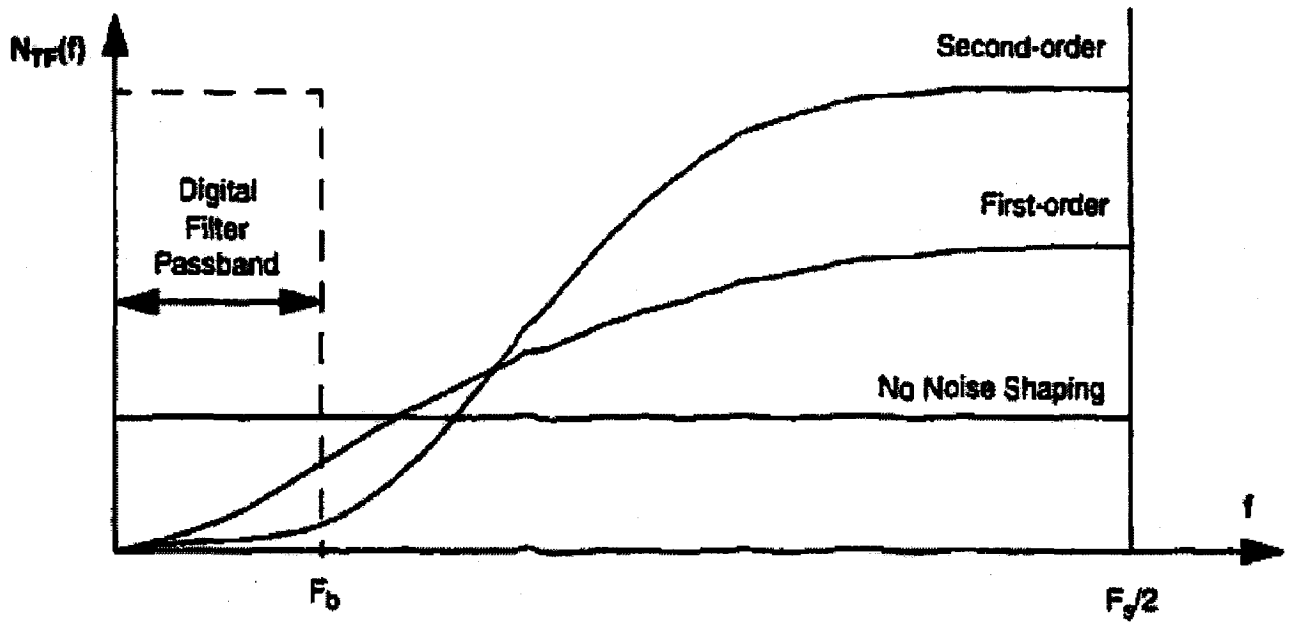



Fig. 2.6 Sigma-Delta Quantization Noise Spectrum [5]

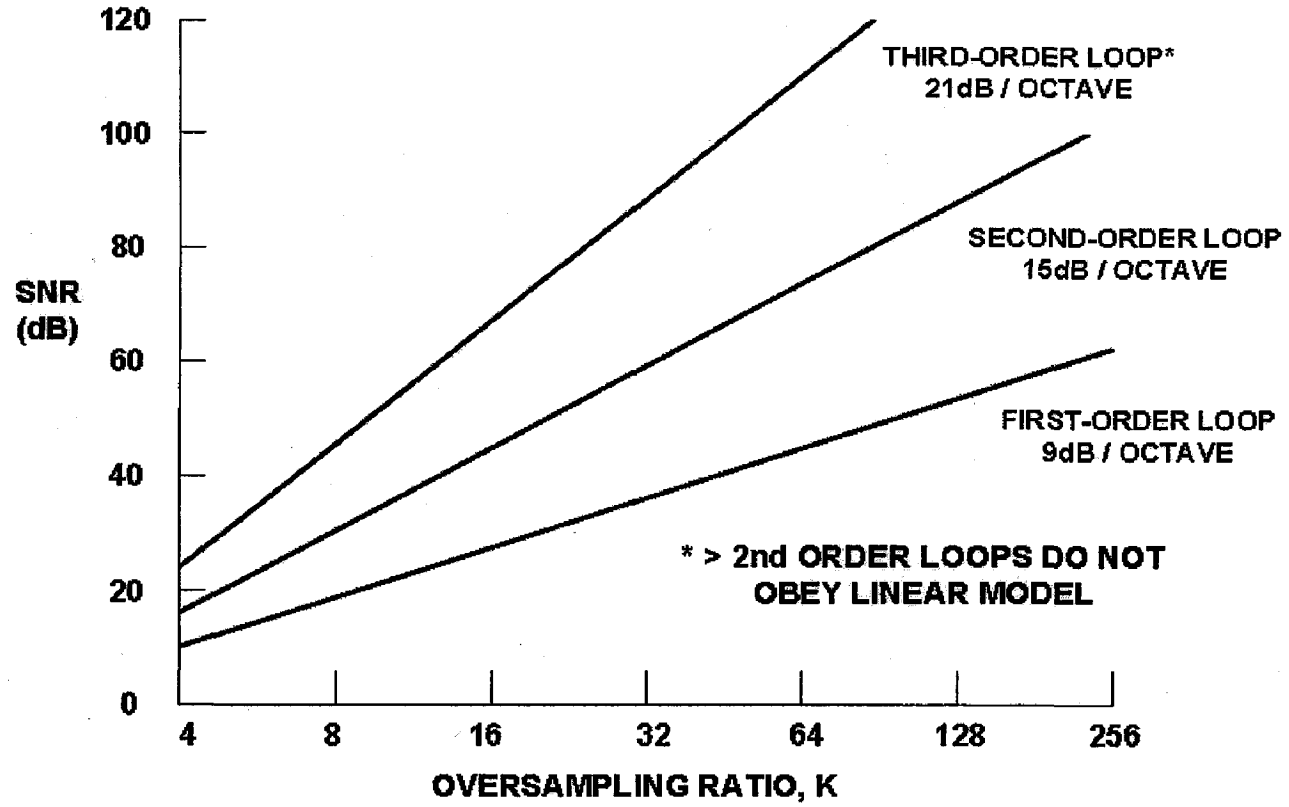



Fig. 2.7 SNR vs. OSR for 1st, 2nd, 3rd Order Loops [5]

## 2.3 ΣΔM ARCHITECTURES FOR DATA CONVERTERS

### 2.3.1 First order and Higher order SD Modulators

Sigma-delta converters realizing higher order achieve even higher resolution by pushing even more noise power outside the signal band. Alternatively, a lower sampling rate can be used to achieve the same resolution for a given signal bandwidth. In this case, the speed requirements on the analog hardware are relaxed. For every doubling of the oversampling ratio, the modulator provides an extra
$(6L+3)$ dB of SNR, or an extra $(L+1/2)$ bits of resolution, where L is the order of the modulator [4].

### 2.3.2 Single bit and Multi bit SD Modulators

The ADC resolution at a low OSR (Over Sampling Ratio) can be improved by using a higher-order loop filter, and/or by increasing the internal quantizer resolution. For single-bit, single-loop modulators, the integrator's gain must be reduced to preserve the loop stability. Therefore, simply increasing the loop filter order at a low OSR will result in a poor Signal to Noise Ratio (SNR) improvement. To achieve high resolution at a low OSR multi bit internal quantization is widely used. Since multi bit quantizers have a more linear gain than single-bit quantizers, the stability of multi bit, single-loop SD modulators is significantly improved.

### 2.3.3 Single loop and cascaded loop SD modulators

Cascaded loops, also called MASH structure, are popular for high dynamic range applications at low OSR because they facilitate higher-order SD loops that do not suffer from stability problems [1], [6].
However, cascaded modulators rely on good matching properties between analog and digital transfer functions. When the quantization noise of the first-stage quantizer is not fully cancelled in the digital error cancellation logic block due to a non-ideal matching, leakage noise appears at the output of the modulator, rapidly decreasing the SNR

performance. Cascaded loops have larger FOM (figure of merit) and are more silicon area-consuming than single-loop structures.

### 2.3.4 Continuous-time and discrete-time SD modulators

In an SD modulator loop, it is possible to build up the noise-shaping filter as a discrete-time (DT) or a continuous- time (CT) circuit.
DT SD modulators are implemented using switched-capacitor (SC) circuit techniques. In SC circuits, amplifiers with high gain bandwidth product (GBW) satisfy the settling requirements. Typically, the GBW is seven times higher than the sampling frequency [7]. CT SD modulators are not sensitive to settling behaviour. As a result, CT SD modulators can potentially operate at higher clock frequency and/or with less power consumption. CT modulators have smaller FOM and are less silicon area-consuming than DT counterparts. CT modulator achieves better linearity performance.

### 2.3.5 Band-pass and base-band Sigma-Delta Modulators

For low-pass signals, the highest frequency component is also the signal bandwidth $f_b$. Then sampling frequency is much greater than the Nyquist rate, which is twice the highest frequency component in the input signal, which is the case for base-band sigma delta modulator.
If a signal with bandwidth $f_b$ is band-pass but is located at a centre frequency $f_c$ its highest frequency is $f_c+f_b/2$.Band-pass sigma-delta modulation allows high resolution [7]. Band-pass sigma-delta modulators can be used in AM digital radios or receivers for digital cellular mobile radios.

# Chapter 3

# SYSTEM LEVEL ARCHITECTURE

## 3.1 ΣΔM - ARCHITECTURE SELECTION

As the order of ΣΔM goes beyond two, the system experiences potential instability [6] while the usage of first order modulator to achieve required dynamic range results in large over sampling ratio (OSR) thus large power. A multi bit quantizer produces harmonic distortion due to step-size mismatch. Thus, second order modulator with 1-bit quantizer is used in our design.

The architecture implementation of second order ΣΔM is shown in Fig. 2. The values for integrators' gain $b_1$ and $b_2$ are used to protect integrators from saturation. The block diagram of the second order ΣΔM using 1-bit quantizer is shown in Fig. 3.1.

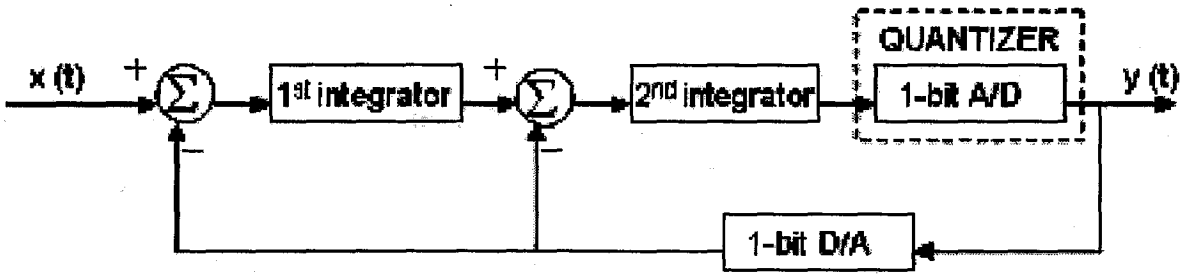



Fig. 3.1 Block Diagram of Second Order ΣΔM

## 3.2 DESIGN ENVIRONMENT

The design of Switched Capacitor Sigma-Delta modulators includes optimization of a large set of parameters, in order to achieve the desired SNR. The fundamental step in the design cycle of mixed signal systems is modeling and simulation. Many simulation approaches exist for evaluating the performance of ΣΔMs. Among all, device-level simulation is the most accurate approach. But, this method becomes impractical for complex systems such as ΣΔM due to the long computational time required. For this reason device-level simulation, normally, is left to the final design verification i.e. Top-

Down design methodology [8] is used for designing these modulators. Also the use of top-down design methodology can reduce the number of iterations in the ΣΔM design cycle.

Due to the inherent non-linearity of the Sigma-Delta modulator loop and more number of parameters for designing, the fundamental step in the design cycle of ΣΔM is modeling and simulation. The simulation of ΣΔMs using behavioral models is a more time-efficient and practical solution. Behavioral models provide the designer good estimates for stability, SNR, and distortion for the chosen architecture. These models offer the designer a set of reusable building blocks that represent components and its nonidealities which results in simulation results closer to logic simulation.
VHDL-AMS, which provides ways of using both event-driven and normal circuit simulation methods, can be used for behavioral modelling of ΣΔM. Nevertheless, VHDL-AMS models for ΣΔMs are rare in literature because of the recent standardization of the language. MATLAB SIMULINK has been widely accepted to model and simulate Sigma Delta Modulators. The optimization process has to be carried out with behavioral simulations in MATLAB and SIMULINK using SD toolbox [9], [10].

This chapter discusses the nonidealities of different blocks in a second order sigma delta modulator and using the SD Toolbox [optimised specification values of different blocks is obtained. Finally the simulation results in MATLAB & SIMULINK environment are presented.

## 3.3 IDEAL SECOND ORDER SC ΣΔM

The second order SC Sigma-Delta modulator consists of two SC integrators, a comparator and feedback system. Fig. 3.2 is the behavioral model of ideal modulator in SIMULINK. This modelling uses the basic building blocks such as discrete time integrator, constant and relay for SC integrator, gain and comparator respectively.
The output spectrum for the ideal modulator simulated using MATLAB and SIMULINK environment is shown in Fig.3.3 for a sinusoidal input signal with 0.2 V amplitude and 200 Hz frequency.

Figure 3.4 shows power density spectrum for second-order sigma-delta modulator. It is seen that the noise is rejected toward the high frequencies through 'noise shaping'.

But in real-time simulations, the modulator includes many non-idealities. The most important non-idealities such as sampling jitter, kT/C noise, internal ADC/DAC's parameters mismatch and non-linearity, operational amplifier parameters (white noise, 1/f noise, finite dc gain, finite bandwidth, slew rate and saturation voltages) have been modeled in Simulink.

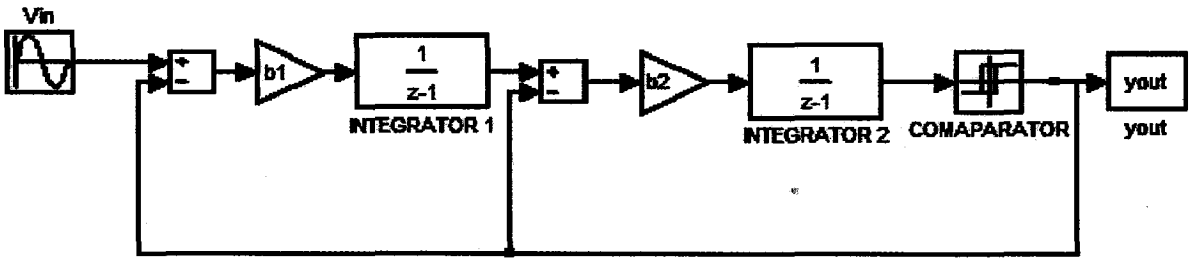



Fig. 3.2 Ideal Second Order Sigma Delta Modulator

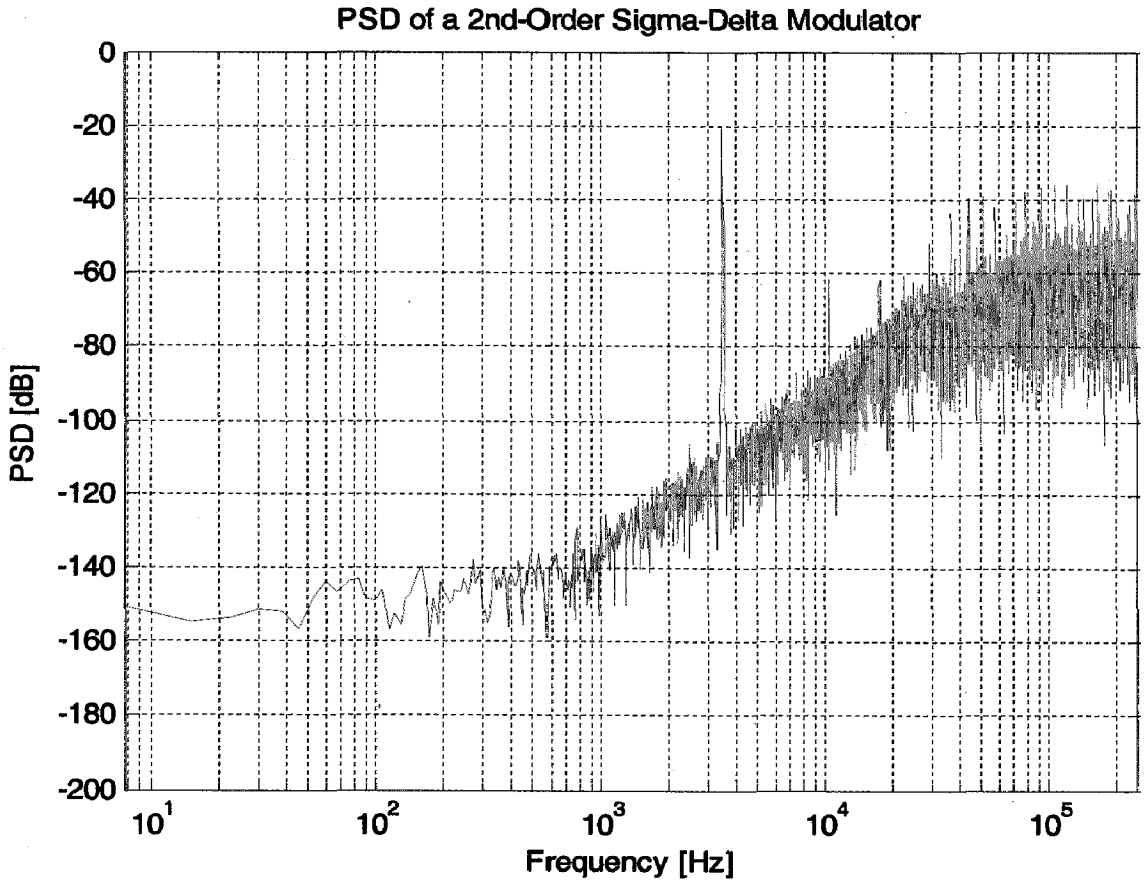



Fig. 3.3 PSD for Ideal Second Order Modulator

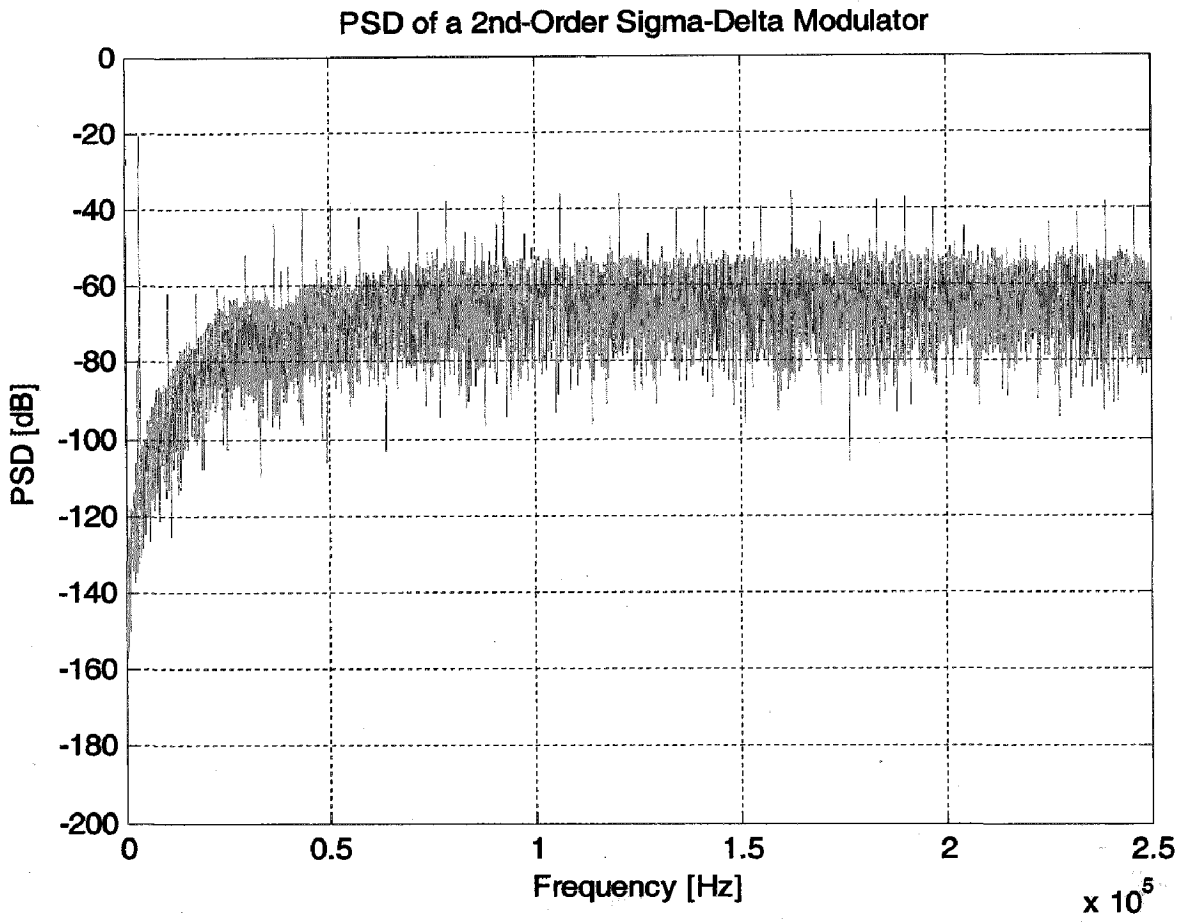



Fig. 3.4 PSD Showing Noise Shaping

## 3.4 NON-IDEALITIES OF SC ΣΔM

The modulator consists of input samplers, an SC integrator, a quantizer and a feedback digitalto-analog converter (DAC).

The non-idealities can be categorized into six classes:

- Sampler related errors, such as sampling jitter;
- integrator related noises, such as kT/C and opamp noises,
- integrator related non-idealities, which are caused by finite key parameters of opamps (finite gain, finite bandwidth, slew-rate and saturation voltages);
- comparator related ones and
- the DAC non-idealities.

**Thermal Noise**

Thermal noise (kT/C noise) is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. In ΣΔMs, kT/C noise is associated with the amplifier and the finite switch resistance of the switched-capacitor integrator.
Thermal noise has a white spectrum and wide band limited only by the time constant of the switched capacitors or the bandwidth of the operational amplifiers. The sampling capacitor $C_s$ of a Switched-Capacitor (SC) Sigma-Delta modulator is in series with a switch, with finite resistance Ron, that periodically opens, thus sampling a noise voltage onto $C_s$. The total noise power can be found evaluating the integral [11]

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1+(2\Pi fR_{on}C_S} df = \frac{kT}{C_S} \tag{3.1}$$

where k is the Boltzmann's constant, T the absolute temperature and $4kTR_{on}$ the noise power spectral density associated with the switch on-resistance. The switch thermal noise voltage $e_T$ (usually called kT/C noise) is then superimposed on the input voltage.
For more than one input SC integrator, each branch has to be modeled with a separate kT/C noise block.

**Jitter Noise**

As the sampling period of switched-capacitor circuits is not constant, this shift in the sampling period introduces a noise source known as jitter. The operation of a Switched Capacitor (SC) circuit depends on complete charge transfers during each of the clock phases. Once the analog signal has been sampled, the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the sampling of the input signal. This also means that the effect of clock jitter on a Sigma-Delta modulator is independent of the structure or order of the modulator.
Clock jitter results in a non-uniform sampling time sequence, and produces an error which increases the total error power at the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the modulator input signal. The error introduced when a sinusoidal signal x(t) with amplitude A and frequency fin is sampled at an instant, which is in error by an amount delta, is given by [10], [11]

$$x(t+\delta)-x(t) \approx 2\pi f_{in}\delta A\cos(2\pi f_{in}t) = \delta\frac{d}{dt}x(t) \tag{3.2}$$

**Switch Non-linearity**

The Switch Non-linearity block models the non-linear on-resistance of the sampling switch assuming a complementary CMOS switch with equally sized N-MOS and P-MOS transistors. The on-conductance of a complementary CMOS switch with equally sized N-MOS and P-MOS transistors, assuming that the input and output voltages are equal is given by [11]

$$G_{SP} = K_N'\frac{W}{L}(V_{DD}-V_{thN}-V_{in}) + K_P'\frac{W}{L}(-V_{SS}+V_{thP}+V_{in}) \tag{3.3}$$

where $V_{in}$ is the input voltage W and L are the width and the length of the transistors, $V_{thN}$ (positive) and $V_{thP}$ (negative) are the threshold voltages of the N-MOS and P-MOS transistors, $K'_N$ and $K'_P$ are the gain factors of the N-MOS and P-MOS transistors and $V_{DD}$ and $V_{SS}$ are the positive and negative supply voltages used for driving the gates of the N-MOS and P-MOS transistors, respectively.

This conductance, which depends on the input signal, together with the sampling capacitance $C_s$, produces a settling transient which leads at the end of the clock cycle (typically after $T_s/2$) to an output value given by [11]

$$V_{out} = V_{in}\left(1-e^{-\frac{T_S G_S}{2C_S}}\right) \tag{3.4}$$

which is in error with respect to the ideal value. This error depends on the input signal and hence gives rise to non-linearity.

**Integrator Settling**

The incomplete settling of switched-capacitor integrators has become one of the most limiting factors in the performance of ΣΔMs. The integrator defective settling is mostly due to the operational transconductance amplifier characteristics such as the finite and nonlinear DC gain, the finite gain-bandwidth, and the slew-rate limitations.

**DC Gain**

The dc gain of the ideal integrator is infinite. In practice, however, the actual gain is limited by circuit constraints and in particular by the operational amplifier open-loop gain $A_0$ (considering also the integrator feedback factor). The consequence of this integrator "leakage" is that only a fraction a of the previous output of the integrator is added to each new input sample. The limited dc gain of the integrator increases the in-band noise. The transfer function of the integrator with leakage becomes

$$H(z)= \frac{z^{-1}}{1-\alpha z^{-1}} \tag{3.5}$$

The dc gain of the integrator $H_0$, therefore, becomes

$$H_0 = H(1)= \frac{1}{1-\alpha} \tag{3.6}$$

and hence the parameter alpha is given by

$$\alpha = \frac{A_0 - 1}{A_0} \tag{3.7}$$

**Bandwidth & Slewrate**

The finite bandwidth and the slew-rate of the operational amplifier are modelled with a building block placed in front of the integrator, which implements a MATLAB function. The effect of the finite bandwidth and the slew-rate are related to each other and may be interpreted as a non-linear gain. In fact, finite bandwidth and slew-rate in SC circuits lead to a non-ideal transient response within each clock cycle, thus producing an incomplete or inaccurate charge transfer to the output at the end of the integration period. The evolution of the output node during the nth integration period is given by [11]

$$v_0(t) = v_0(nT_S - T_S) + \alpha V_S(1-e^{-\frac{1}{\tau}}) \text{ for } 0 < t < T_S/2 \tag{3.7}$$

where $V_s = V_{in}(nT_s - T_s/2)$, alpha is the integrator leakage (which accounts for the operational amplifier finite gain $A_0$) and $\tau = 1/(2\text{PiGBW})$ is the time constant of the integrator (GBW is the unity gain frequency of the integrator loop-gain during the considered clock phase). The slope of this curve reaches its maximum value when t = 0, resulting in

$$\frac{d}{dt}v_0(t)\Big|_{max} = \alpha\frac{V_S}{\tau} \tag{3.8}$$

**Saturation**

The swing of signals in a Sigma-Delta modulator is a major concern. It is therefore important to take into account the saturation levels of the operational amplifier used. This can simply be done using a saturation block inside the feedback loop of the integrator.

**Mismatches**

The gain factors in switched-capacitor integrators are implemented using capacitor ratios. The accuracy of these ratios is restricted by the matching accuracy of fabrication processes. Consequently, the capacitance mismatch turns in gain variations which affect the transfer functions of the integrator, and potentially the system's stability. A second effect of mismatch becomes critical in multi-bit designs. Mismatch in the internal D/A converter causes inaccurate output levels such that the output contains harmonic distortion. This harmonic distortion makes the system integral linearity no better than that of the internal D/A converter. Dynamic element matching techniques are used to reduce the effects of component mismatch inside the D/A converter.

## 3.5 NONIDEAL BEHAVIORAL MODEL

The non-ideal ΣΔM including all the above discussed nonidealities has been modelled in SIMULINK using SD toolbox is shown in Fig. 3.2. The SD toolbox is a toolbox created to simulate SC ΣΔM at behavioral level, within Simulink environment [4], [5]. Table 3.1 summarises all the non-idealities observed in a practical ΣΔM.

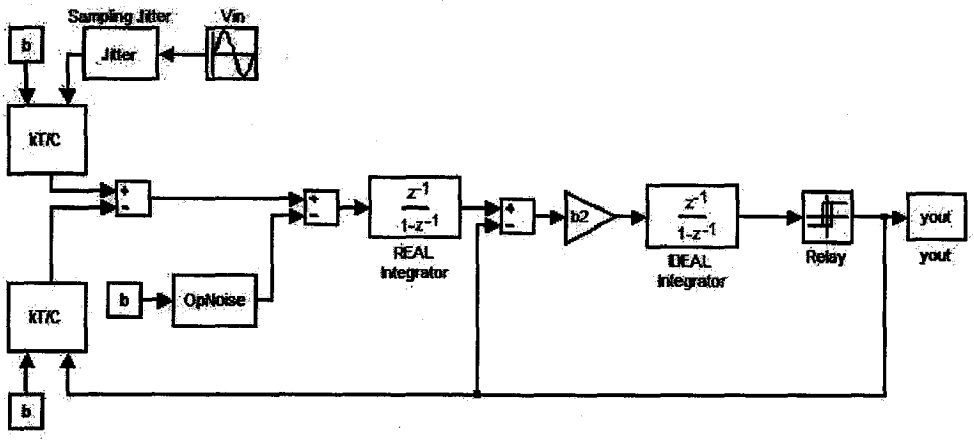



Fig. 3.5 Non ideal ΣΔM

Table 3.1 Basic building blocks and its nonidealities

| BLOCK | NONIDEALITIES |
|---|---|
| Opamp | Finite and non-linear gain, dynamic limitations (incomplete settling error, harmonic distortion), output range, thermal noise. |
| Capacitor | Non-linearity, mismatching |
| Switches | Thermal noise, finite and non-linear resistance |
| Clock | Jitter |
| Comparator | Offset, hysteresis |

And the behaviorally modeled nonideal second order modulator resulted in Power Spectral Density (PSD) as shown in Fig. 3.4. The Signal to Noise Ratio (SNR) for ideal modulator is 71.6 dB while the SNR for non-ideal modulator is 68.9 dB.

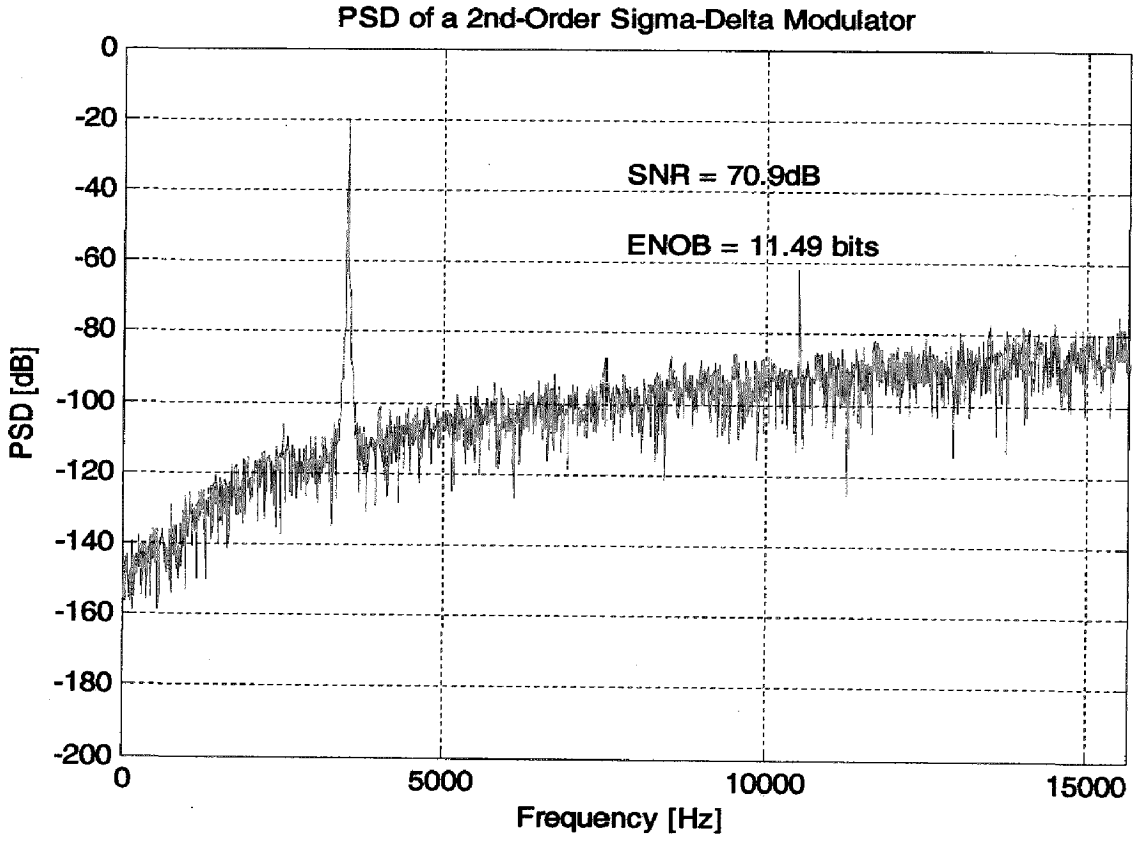



Fig. 3.6 PSD for Nonideal Second Order ΣΔM

# Chapter 4

# CIRCUIT LEVEL IMPLEMENATION

The second order sigma delta modulator realised using SC technique consists of two switched capacitor integrators, a comparator, and feedback circuitry.

## 4.1 SWITCHED CAPACITOR INTEGRATOR

The switched capacitor (SC) technique Switched capacitor (SC) techniques have been demonstrated to be an efficient way of implementing analog functions in CMOS technology. The elements required for the realization of SC circuits are capacitors, switches, and opamps [12]. The major advantages of SC circuits are

- → Low cost integration, as it is compatible with standard CMOS technology
- → Realization of highly accurate signal processing function
- → Good voltage linearity
- → Good temperature characteristics

Thus integrator realised using SC technique provides us with highly accurate transfer function with a low distortion and programmability on the time constants.

### 4.2.1 CONVENTIONAL SWITCHED CAPACITOR INTEGRATOR

Switched capacitor integrator is the circuit obtained by replacing resistor in continuous time integrator by its discrete time equivalent of resistor as shown in Fig. 4.1.

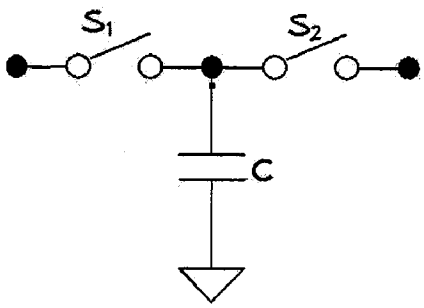



Fig. 4.1 Discrete Time Resistor Equivalent

The resistor value realised using the above circuitry is $T/C$, where T is the clock period of the nonoverlapping clock used to switch on and off switched $S_1$ and $S_2$. The SC

integrator using this discrete resistor suffers from nonlinearity due to parasitic capacitances. The single ended SC integrator which is parasitic insensitive is shown in Fig. 4.2.

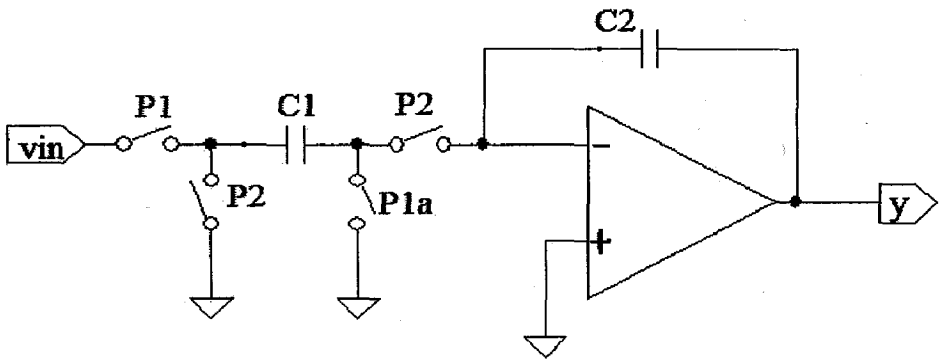



Fig. 4.2 Parasitic Insensitive Non inverting Integrator

It is driven by two non-overlapping clock phases P1 and P2 to realize an integrator with a positive input and a unit delay with the transfer function given by [13]

$$H(z) = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{4.1}$$

The switches that have P1 as trigger is conducting in phase 1 and the switches triggered by P2 are conducting in phase 2. During the phase P1, integrator is in sampling mode and in phase P2, it is in integrating mode.

## DRAWBACKS OF CONVENTIONAL SC INTEGRATOR

### → TRIGGERING SIGNALS

To minimize distortion, dc error and to keep dc offset low, clocks $P_1$, $P_2$, $P_{1a}$ (slightly advanced wrt P1), $P_{2a}$ are to be employed to turn off the switches near the virtual ground first as shown in Fig. 4.3. By delaying clock $P_1$, for switch S1 wrt clock $P_{1a}$ for switch S3, the input dependent offset voltage appearing at the output can be removed [4].

### → PROBLEM WITH CRITICAL SWITCHES

The switches can be realized using NMOS/PMOS transistor. But reducing the supply voltage correspondingly reduces the overdrive voltage of the MOS switches, and the classical approach based on the use of transmission gate (complementary switches) is no more effective. The switch connected to input in Fig. 4.2 is termed as 'critical switch'

[14] as the overdrive voltage $V_{GS}$ keeps varying according to the input signal and to turn on this switch it is difficult to satisfy $V_{GS}>V_{DD}-V_{th}$. Therefore critical switches are switches which have signal dependent $V_{GS}$.

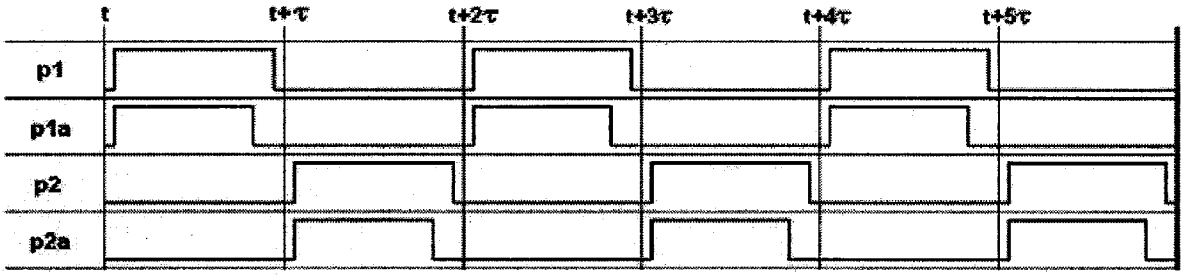



Fig. 4.3 Timing diagram of Triggering Signals

At very low supply voltage, the reduction of the signal swing causes problem in the conduction of critical switches decreasing its performance drastically. Thus, specific approaches different from the standard SC design have to be used to overcome this problem. Four solutions to this limitation have been proposed in the bibliography.

- Use of an on-chip voltage multiplier
- Use of low $V_{th}$ transistors.
- Switched opamp (SO) approach
- Auto-zeroed integrator(AZI)

The deep sub-micron technologies will not sustain the multiplied voltage, whereas the low $V_{th}$ transistors results in the leakage current which causes large harmonic distortion and also involves high cost. In SO technique, critical switches are eliminated and replaced by opamps which are switched on and off. However, this solution is not suitable for high speed SC circuits applications, since turning on/off opamps needs more time than turning on/off switches. In AZI, integrating capacitor is switched instead of the opamp in a switched opamp integrator. This technique is faster than the switched opamp approach [15].

## AUTO-ZEROED INTEGRATOR

In an AZI, the charge is transferred by switching the integrating capacitor of the previous integrator, not by switching the opamp as in a switched-opamp integrator. A noninverting

integrator realised using auto zeroing technique is shown in Fig. 4.4. The low-voltage AZI can work at clock speeds very close to the speed of a conventional SC circuit. Moreover, the working conditions (voltage and current biases) of the opamp are not disturbed during operations [15]. This makes AZI more suitable than switched-opamp circuits for the design of high-speed SC circuits

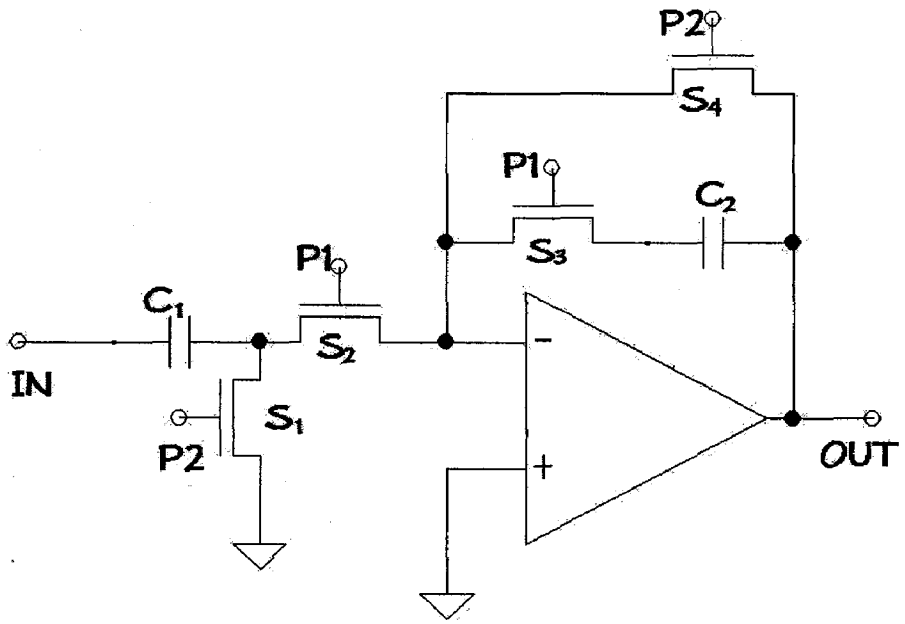



Fig. 4.4 Auto-Zeroed Integrator [15]

During phase P2, the capacitor $C_1$ is charged to input voltage through switch $S_1$ while the output is maintained at common mode voltage as switch $S_4$ is conducting. During phase $P_2$ the charge stored on $C_2$ is not lost as there is no discharge path available due to $S_3$ off. This phase is called 'reset phase' as output is reset to ground or virtual ground. During phase $P_1$, the switches $S_2$, $S_3$ conduct and $S_1$, $S_4$ are in nonconducting state. The charge on $C_1$ is transferred to $C_2$, leaving the total charge on $C_2$ to be equal to its previous charge plus the charge transferred from $C_1$. This is called 'integrating phase'.

NMOS transistors can be used to realise all these switches. The switches whose sources are connected to virtual ground and gates to supply voltage should satisfy VGS=VDD-$V_{CM}$ for transistor to conduct properly. To keep a reasonable output swing range if $V_{CM} \approx 0.5$ V (to keep a reasonable output swing range) for supply voltage of $V_{DD}$=1 V, the $V_{th}$ of NMOS transistor should be less than 0.5 V. In 0.18 μm CMOS technology, $V_{th}$ of NMOS is around 0.38 V. Hence, AZI can be used at 1 V supply voltage for 0.18 μm technology to eliminate critical switches for efficient low voltage operation.

Because the channel voltages of the NMOS switch are fixed at $V_{CM}$, there is no signal-dependent switch channel voltage, and therefore no signal-dependent charge injections. It is clear that there is no need to use the delayed clock phases as used in conventional SC circuits.

For the same reason, the on-resistance of all switches is not related to the signal level.

So, AZI does not have these two major sources of distortion appearing in conventional SC circuits.

## 4.2 OPERATIONAL AMPLIFIER

The main building block of SC integrator is an operational amplifier that performs the role of an active amplifier to form a negative feedback loop. An operational amplifier, usually referred to as 'opamp', is defined generally, as a high-gain differential input amplifier [16] and they are used to realise a feedback system to perform an operation precisely.

### OPAMP TOPOLOGY SELECTION

- In a low voltage low power analog design environment, the dynamic range is lowered due to the lower allowable signal swing and due to the larger noise voltages that arise as a result of the smaller supply currents. In order to maximise the dynamic range, a low voltage amplifier must be able to deal with signal voltages that extend from rail-to-rail.
- The unity-gain frequency of operational amplifiers is greatly affected by the low power condition. The lower supply currents will drastically reduce the bandwidth for cases where the load capacitance cannot be lowered. To obtain sufficient low frequency gain, low voltage amplifiers often require cascaded gain stages, which results in more complex frequency compensation schemes.
- Due to the fact that transistors in an opamp are required to operate in the saturation region, cascoding transistors to realize a higher equivalent impedance becomes more difficult because they reduce the available voltage swing. It is necessary to have the largest voltage swing to maintain a certain amount of noise margin when working with a reduced voltage supply. [3]

To obtain a maximum SNR in the inverting feedback applications:

• The output voltage has to be able to swing from rail-to-rail

• The common mode input voltage has only to be biased at a fixed voltage

As a result, to meet the above requirements telescopic cascoded opamp is impractical when working with low voltage applications. A feasible opamp topology is the two-stage Miller compensated opamp as they provide the high DC gain by cascading a transconductance (*Gm*) stage with an output stage (providing the large swing). It is inappropriate to cascade more than two stages, because each stage adds at least one pole in the open loop response of the amplifier.

**Two Stage Opamp**

The first stage of an op-amp is a differential amplifier. This is followed by another gain stage, such as common source stage, and finally an output buffer, as shown in Fig. 4.5.

If the op-amp is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. On the other hand, if the op-amp is to drive a resistive load or a large capacitive load, the output buffer is used. The two stage opamp with no buffering stage is generally termed as Operational Transconductance Amplifier (OTA) [13].

As ΣΔ modulators find most of its applications at low frequencies and output load capacitance is small, two stage OTA can be used although its achievable bandwidth is low due to the nondominant pole formed by the load capacitance and the output impedance of the second stage. Thus two stage OTA provides with a high gain input stage and an output stage with high driving capabilities which helps maximising SNR as large output voltage range is attainable [3].

The two-stage CMOS opamp shown in Fig. 4.6 is widely used because of its simple structure and robustness. Two-stage Operational Transconductance Amplifier (OTA) has many advantages - high open-loop voltage gain, rail-to-rail output swing, large common-mode input range, only one frequency compensation capacitor, and a small number of transistors.

The differential pair in Fig. 4.2 is formed by n-channel MOSFETs, M1 and M2. The first stage gives a high differential gain and performs the differential to single ended

conversion. This first stage of op-amp also had the current mirror circuit formed by a p-channel MOSFETs, M3 and M4. The transistor M6 serves as an n-channel common source amplifier which is the second stage of op-amp and is aided by current load M7. The bias of the op-amp circuit is provided by M8 and $I_B$.

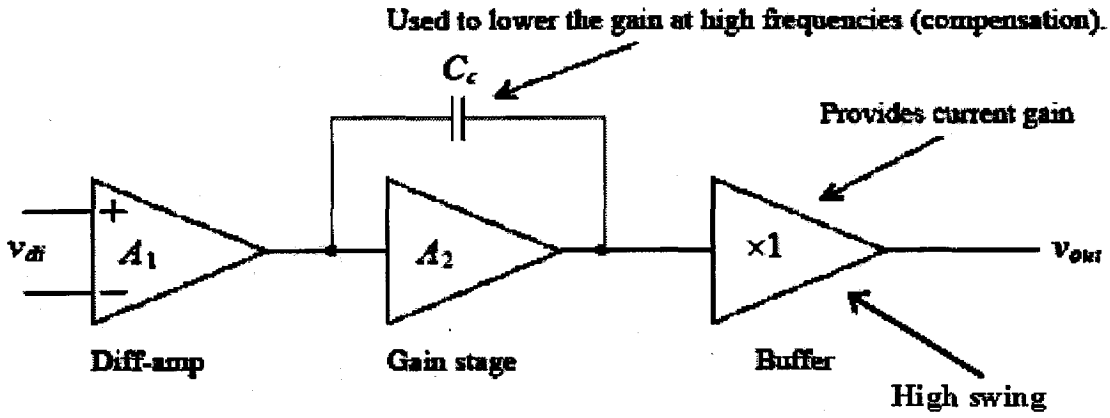



Fig. 4.5 Block Diagram of Two Stage Opamp

**Compensating the opamp**

Since opamps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability.

To ensure stability

$$|A_{OL}\beta| = 1 \tag{4.2}$$

must drop to unity before

$$\angle A_{OL}\beta = -180^0 \tag{4.3}$$

where $A_{OL}$ is openloop gain and $\beta$ is feedback gain.

The open-loop transfer function must be modified such that the closed-loop circuit is stable and the time response is well-behaved.

The simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor across the high-gain stage. However, due to an unintentional feed-forward path through the Miller capacitor, a right-half-plane (RHP) zero is also created and the phase margin is degraded. Such a zero, however, can be removed if a proper nullifying resistor is inserted in series with the Miller capacitor [17].

In designing an opamp, numerous electrical characteristics, e.g., gain-bandwidth, slew rate, common-mode range, output swing, offset, all have to be taken into consideration. Unfortunately, in order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an opamp that meets all specifications needs a good compensation strategy and design methodology.

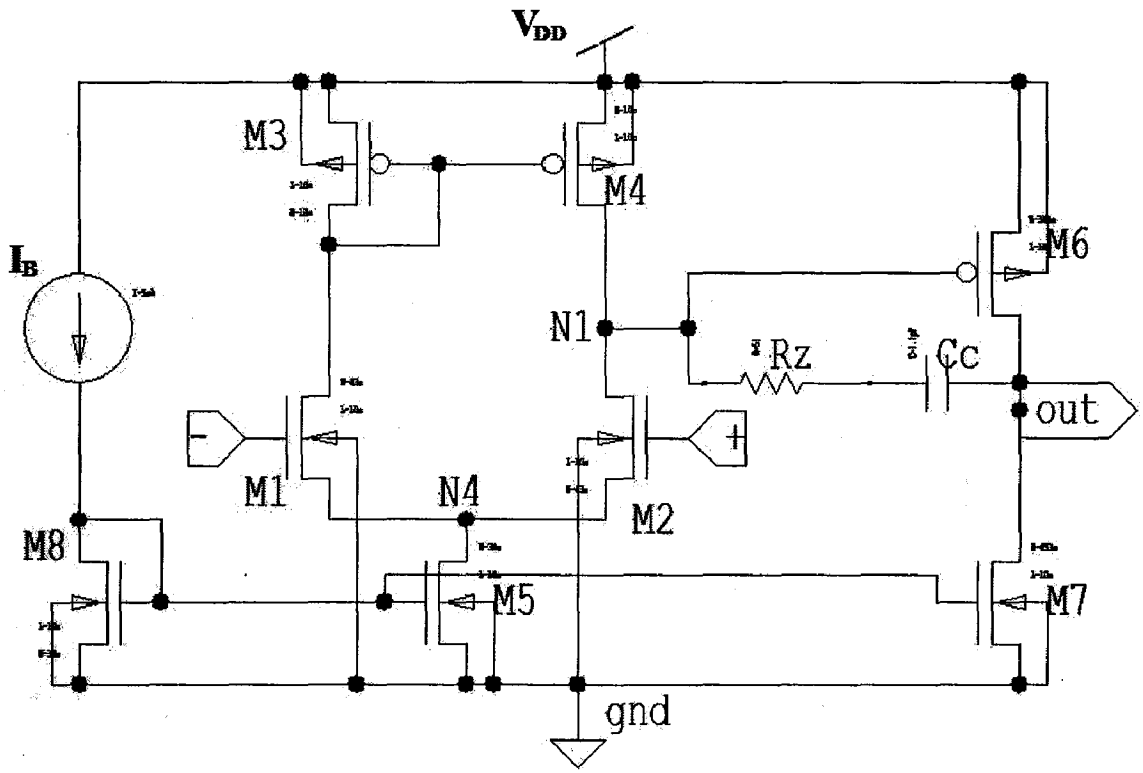



Fig. 4.6 Basic Two Stage CMOS Opamp

## 4.3 COMPARATOR

To reduce power, dynamic latch comparator is used which removes the need for pre-amplifying stage. [18] The 'Lewis-Gray' dynamic comparator shown in Fig. 4.7 was introduced by [19].

The operation of the comparator is as follows. When the clock signal is low, the transistors M9 and M12 are conducting and M7 and M8 are cutoff, which forces both differential outputs to $V_{DD}$ and no current path exists between the supply voltages.

Simultaneously M10 and M11 are cutoff and the transistors M5 and M6 conduct. This implies that M7 and M8 have a voltage of $V_{DD}$ over them. When the comparator is latched, the control signal goes up (clock=$V_{DD}$), which turns M7 and M8 on. Immediately after the switching moment, the gates of the transistors M5 and M6 are still at $V_{DD}$ and they enter saturation. The imbalance of the conductances of the left and right input branches formed by M1, M2, M5 and M3, M4, M6 determines which of the outputs goes to $V_{DD}$ and which to 0 V. After a static situation is reached when clock= $V_{DD}$, both branches are cutoff and the outputs preserve their values until the comparator is reseted again by switching latch to 0 V.

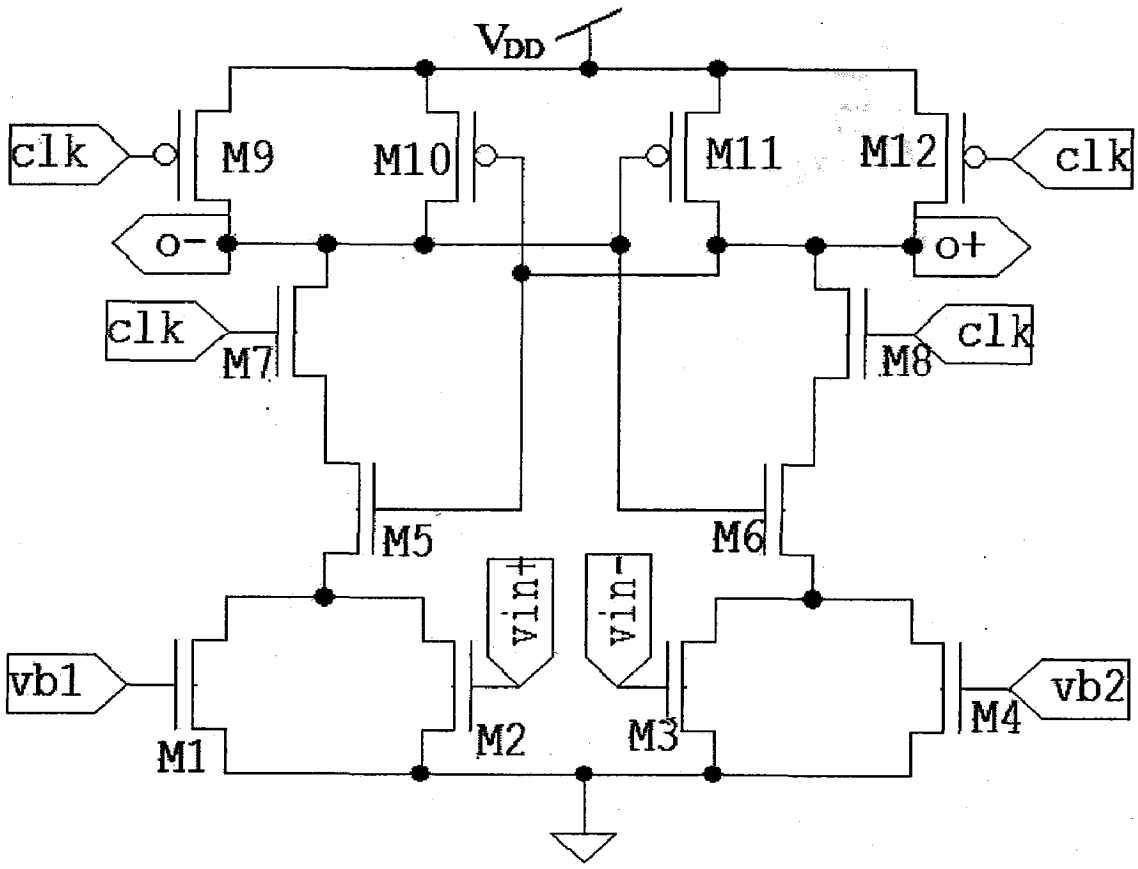



Fig. 4.7 Dynamic Latch Comparator

The transistors connected to the input and reference M1-M4 are in the triode region and act like voltage controlled resistors. If no mismatch is present, the comparator changes its output when the conductances of the left and right input branches are equal. By denoting $W_A = W_1 = W_3$ and $W_B = W_2 = W_4$ the input voltages when the comparator changes the state is given below

$$V_{+in} - V_{-in} = \frac{W_B}{W_A}(V_{+ref} - V_{-ref}) \quad (4.4)$$

By dimensioning of the transistors width $W_A$ and $W_B$, the threshold of the comparator can be adjusted to the desired level.

The comparator produces output of $V_{DD}$ when it is in reset mode. But in order to hold the previous value during reset phase an SR latch, shown in Fig. 4.8.

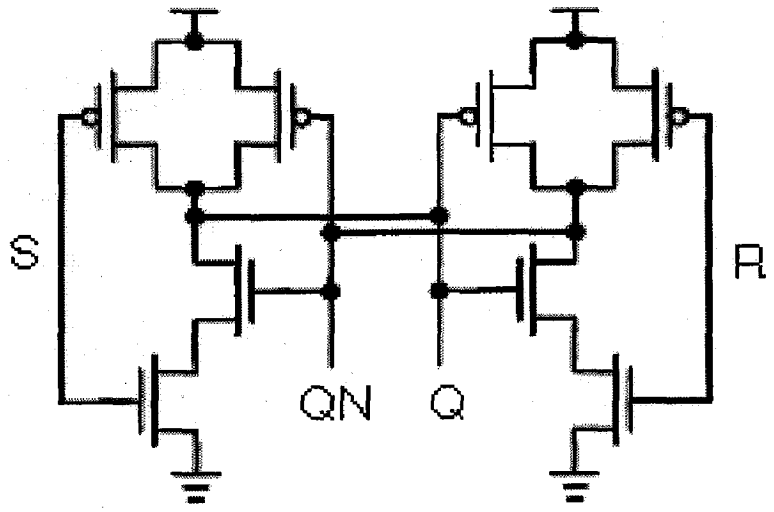



Fig. 4.8 NAND based SR Latch

Thus comparator output produces digital output in bits according to the input waveform when in comparing mode and holds its previous output when in reset mode.

## 4.4 1-bit DAC and SUMMER IMPLEMENTATION

The output obtained at comparator is in bits. This digital output must be converted to analog signal using DAC, to use it as feedback signal. As comparator is nothing but a 1-bit ADC, the digital output is in '0's and '1's. The corresponding 1-bit DAC circuit output will be '$-V_{ref}$' and '$+V_{ref}$' respectively. Therefore, corresponding to output 0/1, the voltages $\mp V_{ref}$ is used as feedback. This DAC output feedback to the integrator input must be subtracted from the input signal. Thus there is need for a summer which performs this action.

The output of SC integrator having two inputs $V_{in1}$ and $V_{in2}$, then the output is integral of $V_{in1}+V_{in2}$, if both the inputs are realised to give noninverting output. The same applies to

the AZI circuitry. To feedback the DAC output to integrator we implement two input AZI as shown in Fig. 4.9, where one input is the input signal and second input is feedback signal. The switches $S_1$, $S_3$, $S_5$ conduct in phase P2 while the switches $S_2$, $S_4$, $S_6$ in phase P1. The voltage at input 'in' and 'ref' terminals result in noninverting integrated output. $+V_{ref}$ is applied as feedback through switch if the output bit is '0' and –Vref if digital output is '1' to get the result as integration of $V_{in} \mp V_{ref}$ if digital output is '1' and '0' respectively. Thus, the output is integration of signal at 'in' plus integration of signal at 'ref'. Thus the summer circuit is seen to be implemented by use of two input integrator with proper clocking of the switches to function one input as inverting and the other as noniverting integrator.

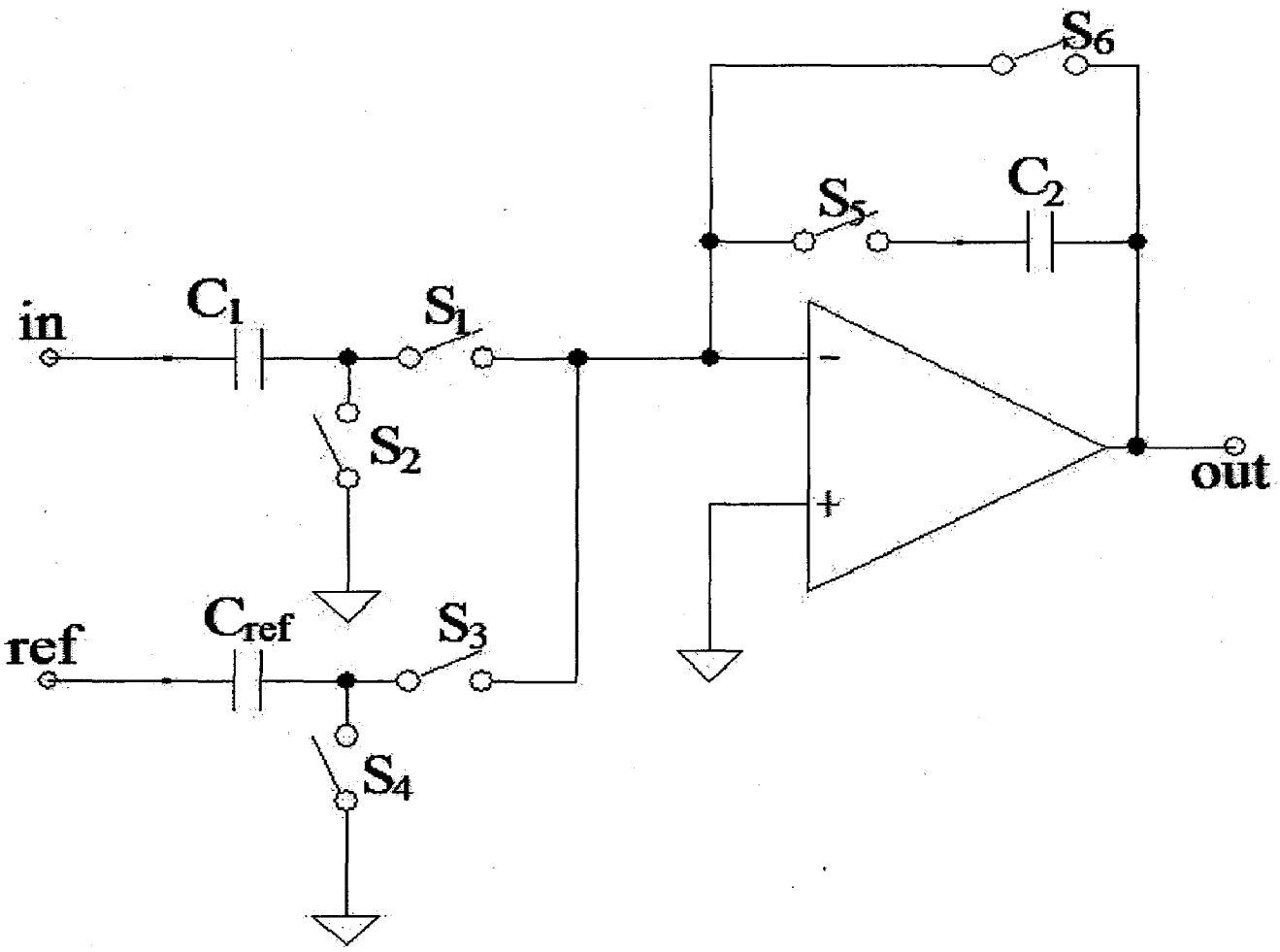



Fig. 4.9 First Order SD Modulator

## 4.5 COMPLETE CIRCUIT DIAGRAM OF SECOND ORDER SDM

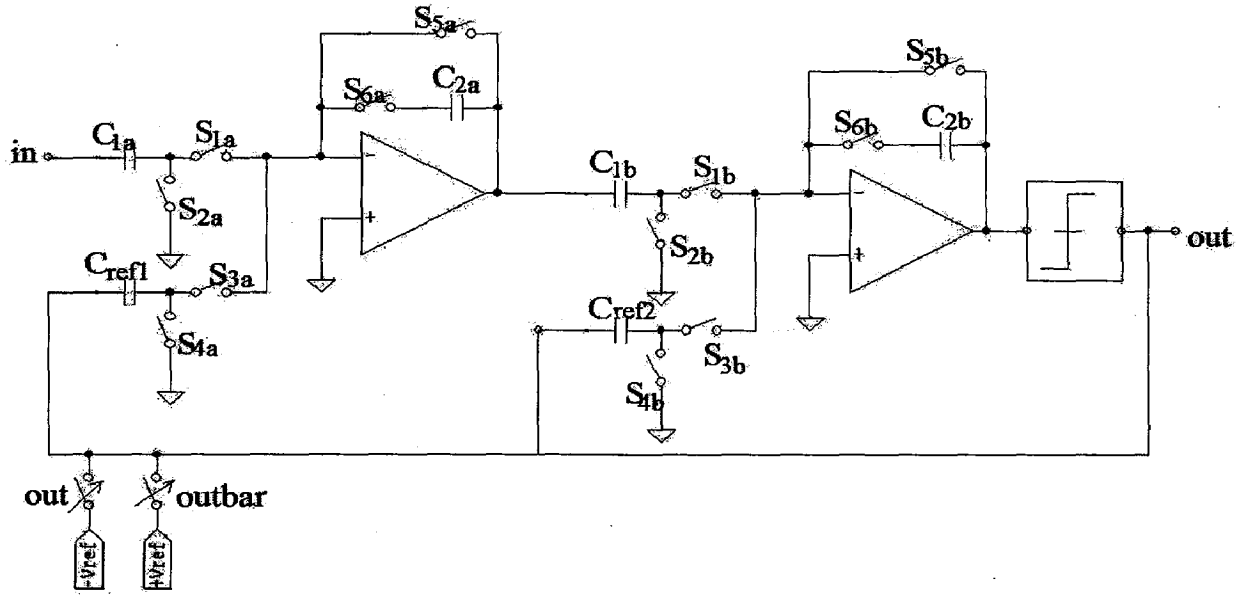



Fig. 4.10 Second Order SDM using AZI

In an AZI, the charge is transferred by switching the integrating capacitor of the previous integrator, not by switching the opamp as in a switched-opamp integrator. Fig. 4.10 shows the complete second order ΣΔM.

The switches $S_{1a}$, $S_{3a}$, $S_{6a}$, $S_{2b}$, $S_{4a}$, $S_{5a}$ conduct in phase P2 while the switches $S_{2a}$, $S_{4a}$, $S_{5a}$, $S_{1b}$, $S_{3a}$, $S_{6a}$ in phase P1. $C_{1b}$ is charged to by Integrator I after $S_{6a}$ is closed in phase P2. At the same time, Integrator II is in the reset phase since $S_{5b}$ is closed, but the charge stored in $C_{2b}$ is not lost because $S_{6b}$ is open. In phase P1, $S_{6a}$ is turned off and the output of Integrator I is reset to zero. As a result, the charge in C1b is dumped to $C_{2b}$ in Integrator II. The stored charge in $C_{1a}$ is not lost during the reset phase of integrator I. Consequently, the charge is transferred from Integrator I to Integrator II.

During clock phase P1 the first integrator will be in reset mode while integrator II in integrating mode. During the clock phase P2, the first integrator is in integrating mode and the second one is in reset mode. Now the comparator output is sensed at the beginning of the clock and latched. The output of comparator is used to provide feedback by applying $+V_{ref}$ to second input of integrators, if output 'out' is low and $-V_{ref}$, if 'out' is high using switches.

# Chapter 5

# DESIGN OF ΣΔM BUILDING BLOCKS

The second order modulator is designed in standard 0.18-μm CMOS technology for a supply voltage of 1V.

The main process parameters for 180nm technology are process transconductance ($K_N$, $K_P$), LAMBDA, threshold voltage of NMOS and PMOS devices ($V_{Tn}$, $V_{Tp}$). The values of these process parameters taken from the technology model file for 0.18μm are listed in Table 5.1.

Table 5.1 Process Parameters for 0.18 μm CMOS Technology

| PARAMETER | VALUE |
|---|---|
| $T_{ox}$ | 4.1 nm |
| $\mu_n$ | 258.9 $cm^2/Vs$ |
| $\mu_p$ | 106.5 $cm^2/Vs$ |
| $V_{Tn}$ | 0.3999 V |
| $V_{Tp}$ | -0.42 V |

From the above parameters process transconductance of NMOS and PMOS can be calculated as,

$\varepsilon_0 = 8.85\ 10^{-14}$ F/cm, where $\varepsilon_0$ is the permittivity of the free space

$C_{ox} = \varepsilon_0 / T_{ox} = (8.85 * 10^{-14}$ F/cm * 3.9) / (4.1 nm) = 0.86 μF/ $cm^2$

$K_N$ and $K_P$ are calculated using $K_N = \mu_n C_{ox}$ and $K_P = \mu_p C_{ox}$ to be 110.9 $\mu A/V^2$ and 45.64 $\mu A/V^2$ respectively.

In estimating the gain of analog circuits, LAMBDA values are used which can be found out from the graph of $I_D$ Vs $V_{DS}$ of the MOS transistor. The inverse of the slope of this graph in saturation region will give the value of lambda. From the graph of drain current vs. drain voltage the values of $LAMBDA_N$ ($\lambda_N$) and $LAMBDA_P$ ($\lambda_P$) for 180nm CMOS

process can be found out. $\lambda_N$ is less than $\lambda_P$, i.e., the slope of the current characteristics in saturation region is higher for PMOS when compared to that of NMOS. It is due to the fact that the drain resistance, due to the short channel effects in deep submicron technologies is dominant for PMOS when compared to that of NMOS.
Among the various architectures for ADC conversion sigma-delta modulator was chosen mainly due to two principal elements of this modulator. Firstly, it is based on oversampling and secondly based on its principal of noise shaping. Consequently, most of the noise power is shifted out of the signal band.

Second order modulator with 1-bit quantizer was chosen as the combination of high order loop filter (>2*nd* order) and high level nonlinear quantizer may lead to a system instability. Table 5.2 summarizes ADC specification for Biomedical Application [20].

Table 5.2 ADC Specification for Biomedical Applications

| PARAMETER | VALUE |
|---|---|
| Bandwidth (BW) | 4 kHz |
| Sampling Frequency ($F_s$) | 0.5 MHz |
| Over Sampling Ratio (OSR) | 64 |
| SNR | about 70 dB |

## 5.1 BEHAVIORAL MODELLING RESULTS

The simulink model of the nonideal second order SDM is shown in Fig. 3.5. This model was simulated with MATLAB/SIMULINK with the nonidealities tabulated in Table 5.3. These values of the nonideal parameters of the modulator given below were used for design of modulator at circuit-level.

In the behavioral modeling of the modulator, the opamp specifications and integrators'

gain coefficients are optimised to achieve SNR of about 70 dB for input signal frequency of 4 kHz and OSR 64.

Table 5.3 Values of Nonidealities [11]

| SC INTEGRATOR NONIDEALITY | VALUE |
|---|---|
| Sampling Jitter | $\Delta\tau = 8$ ns |
| Switched $(kT/C)$ noise | $C_f = 5$ pF |
| Input referred opamp noise | $V_n = 50\ \mu V_{rms}$ |
| Finite DC gain | $H_0 = 1000$ dB |
| Finite Bandwidth | GBW = 10 MHz |
| Slew-rate | SR = 17 V/μs |
| Saturation voltage | $V_{max} = 0.6$ V |

The specifications of OTA for the integrator are

Gain Bandwidth (GBW) =15MHz

Gain ($A_v$) = 57 dB

Phase Margin = 90 deg

As the opamp used in feedback loop requires a phase margin of 60 deg. to keep the closed loop system stable [16].

Integrators' gain coefficients (b1 and b2) which are necessary due to saturation value of the opamp block in SC integrator. These are optimised for high SNR are, 0.4 and 0.5 respectively.

## 5.2 OTA DESIGN & TRANSISTOR SIZING

The aim was to design a two stage operational amplifier that would satisfy the above given specifications.

The opamp design is based on the following main parameters: noise, phase margin (PM), gain-bandwidth product ( $f_{GBW}$), load capacitance ($C_L$ ), slew rate (SR), input common mode range (CMR), output swing (OS), and input offset voltage (due to systematic errors). The parameters such as dc gain, CMRR and PSRR, are not used during the design steps since they depend on the output resistance of MOS transistors and greatly depend on the amplifier topology (typical dc gain and CMRR in a two-stage OTA are in the ranges of 60–80 dB and 70–90 dB, respectively) and can only be predicted by simulation using accurate transistor models.

## OTA TRANSISTOR SIZING

STEP 1: The design procedure begins by choosing a device length to be used. This value will determine the value of the channel length modulation parameter $\lambda$, which is a necessary parameter in the calculation of amplifier gain. For 180nm technology the minimum channel length is 0.18 μm. For all the devices used in the entire circuits minimum channel length is taken as device length, to minimize the capacitance and also resistive effect thereby achieving improvement in terms of speed.

$$L = 0.18\ \mu m$$

STEP 2: Setting the minimum value for the compensation capacitor $C_C$. Placing the output pole $P_2$ 2.2 times higher than the GBW permits a 60° phase margin. A phase margin of 60° is sufficient for keeping the ringing effect in the output signal, in a closed loop system, to an acceptable level. Such pole placement results in the following requirement for the minimum value for $C_C$:

$$C_C > (2.2/10)\, C_L \qquad (5.1)$$

$$\Rightarrow \quad C_C > (2.2/10)\, 2pF = 1\ pF$$

$$\Rightarrow \quad 1\ pF \text{ value is considered for } C_C$$

STEP 3: Determine the minimum value for the tail current $I_5$, based on slew rate requirement.

The slew rate performance of the amplifier depends on the slews on both the output node of the differential stage and the output node of the second stage, which are referred to as

internal and external slew rate, respectively. These slew rate terms are related to the quiescent currents $I_{D1,2}$ and $I_{D8}$ according to

$$SR_{INT} = \frac{2I_{d1,2}}{C_C} \tag{5.2a}$$

$$SR_{EXT} = \frac{I_{D8} - 2I_{D1,2}}{C_L} \tag{5.2b}$$

To satisfy slew rate performance, set the internal and external slew rate not lower than the target value SR. In a first design step we can set $SR_{INT} = SR_{EXT} = SR$ and get

$$I_{D1,2} = \frac{SR}{2} C_C \tag{5.3}$$

$$I_5 = SR\ (C_C) \tag{5.4}$$

$$\Rightarrow \quad I_5 = (10\ V/\mu s)(1\ pF) = 10\ \mu A$$

STEP 4: The aspect ratio of M3 ($S_3$) is determined by the positive input common mode range (ICMR).

$$S_3 = (W/L)_3 = I_5 \{ (K_3) [V_{DD} - Vin(max) - |V_{T3}| + V_{T1}]^2 \}^{-1} \quad \text{(Eq. 23)}$$

where $K_3$ $V_{T3}$ $V_{T1}$=are the process transconductance of M3 and threshold voltages of M3, M1 respectively.

$$\Rightarrow \quad S_3 = 1.45$$

$$\Rightarrow \quad \text{Since, } S_3 = S_4,\ S_4 = 1.45$$

If the values of S3, S4 are less than 1, it is increased to a value that minimizes the product of W and L to minimize the area of the gate region, which in turn reduces the gate capacitance. This gate capacitance contributes to the mirror pole which may cause degradation in phase margin.

STEP 5: Mirror pole P3 has to be greater than 10GBW for all the formulation under consideration to be valid.

$$P3 \approx -g_{m3} (2\ C_{GS3})^{-1} = -\sqrt{2}\ K_3\ S_3\ I_3\ (2\ W_3\ L_3\ C_{ox})^{-1} \tag{5.5}$$

$$\Rightarrow \quad P_3 >> 10*30\ MHz$$

Therefore, mirror pole and zero can be unconsidered in this design.

STEP 6: Requirements for the transconductance of the input transistors can be determined from knowledge of $C_C$ and gain-bandwidth (GBW). The tranconductance $g_{m1}$ is calculated using the following equation

$$g_{m1} = GBW\ (C_C) \tag{5.6}$$

$$\Rightarrow \quad g_{m1} = 2 * \pi * 30MHz * (1pF) = 188\ \mu S$$

The aspect ratios of M1, M2 are given by,

$$S_1 = (W/L)_1 = g_{m1}^2 / (K_1\ I_5) \tag{5.7}$$

$$\Rightarrow \quad S_1 = (W/L)_1 = 32$$

$$\Rightarrow \quad S_1 = S_2 = 32, \text{ considering symmetry of the circuit.}$$

STEP 7: Using the negative ICMR equation $V_{DS5}$, the saturation voltage of M5 is calculated as below:

$$V_{DS5} = Vin(min) - V_{SS} - (I_5 / \beta_1)^{1/2} - V_{T1} \tag{5.8}$$

$$\Rightarrow \quad \beta_1 = S_1 * K_1$$

$$\Rightarrow \quad V_{DS5} = -0.3 + 1 - (10\ \mu / 32 * 110\ \mu)^{1/2} - 0.369 = 0.278\ V$$

$S_5$ is then given by,

$$S_5 = 2\ I_5\ (K_5\ V_{DS5}^2) \tag{5.9}$$

$$\Rightarrow \quad S_5 = 2*10\ \mu\ (110\mu * 0.278^2)$$

$$\Rightarrow \quad S_5 = 1.335$$

STEP 8: For a phase margin of 60° the location of the output pole is assumed to be at 2.2 times GBW. Based on this assumption the transconductance $g_{m6}$ is determined using the following relationship

$$g_{m6} = 2.2\ (g_{m2})\ (C_L / C_C) \tag{5.10}$$

STEP 9: From the values of $g_{m6}$, $S_6$ current through M6 is calculated and then the $V_{DS}$ drop across M6. $I_6$ plays a major role in determining the power dissipation of the opamp.

$$I_6 = g_{m6}^2\ \{2\ K_6\ S_6\}^{-1} \tag{5.11}$$

$$V_{DSsat6} = \sqrt{(2\ I_6 / S_6\ K_6)} \tag{5.12}$$

⇨ $I_6 = (66.6\ \mu)^2 \{2 * 45.64\mu * 66.6\}^{-1} = 112.5\ \mu A$

⇨ $V_{DSsat6} = \sqrt{(2 * 112.5\ \mu / 66.6 * 45.64\mu)} = 0.074\ V$

⇨ Therefore, Vout(max) = 1- 0.165 = 0.926 V

STEP 10: $S_7$ is designed to achieve the desired current ratios between $I_5$ and $I_6$.

$$S_7 = (I_6 / I_5)\ S_5 \tag{5.13}$$

⇨ $S_7 = (112.5\mu / 10\mu) * 2.335 = 26.25$

⇨ $V_{DSsat7} = \sqrt{(2\ I_7 / S_7\ K_7)} = 0.0635V$

⇨ Therefore, Vout(min) = -1 + 0.00635 = -0.9364V

Now the opamp is designed with the given specifications.

STEP 11: Now the power dissipation can be calculated and if it is not in the specified limits bias currents $I_5$, $I_6$ are reduced and the aspect ratios of all the transistors are redesigned.

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|) \tag{5.14}$$

⇨ $P_{diss} = (10\mu + 56.3\mu)(1 + 1) = 132.6\ \mu w$

From the above fig., it is observed that there is a trade-off between noise and power. If we wish to design an opamp with less power then it consumes more power and this happens with increase in $C_c$. Thus to decrease power consumption, Cc value can be increased which in turn increases the noise.

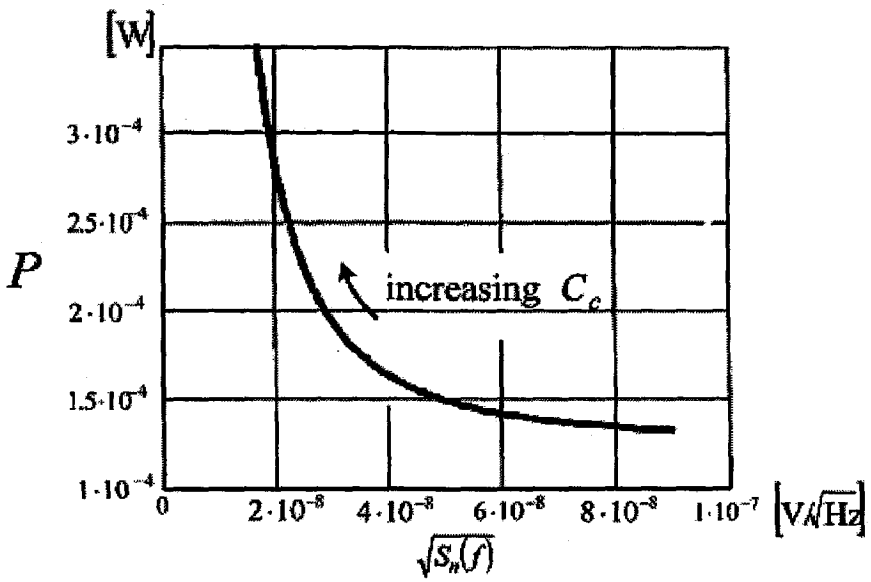



Fig. 5.1 Noise Spectral Density vs. Power Consumption [21]

TABLE 5.4 Opamp Transistor Sizes

| TRANSISTOR | W/L | TRANSISTOR | W/L |
|---|---|---|---|
| M1 | 32 | M5 | 2.335 |
| M2 | 32 | M6 | 66.6 |
| M3 | 1.45 | M7 | 26.28 |
| M4 | 1.45 | M8 | 2.335 |

The transistor sizes for the above design are given in Table 5.4. The circuit is simulated using these aspect ratios and if the any of the specifications is non-satisfactory redesign has to be done in order to achieve the required specifications.
For reduction of noise at low frequencies, increase the channel length and proportionally the channel width of M1 and M2.

Gain can be increased by increasing $(W/L)_{1,2,5}$ and$L_{3,4,8}$ ; $I_7$ and $I_8$ decreased. Slew rate can be increased by increasing $I_7$ and/or decreasing $C_c$. GBW can be increased by increasing $I_7$ and $(W/L)_{1,2}$ ; decreasing $C_c$.

If we design the opamp with the values obtained, the DC gain in open loop configuration is found to be about 51 dB. In order to increase the gain of the opamp, $(W/L)_{1,2}$ is increased and it is found that gain is about 55 dB by doubling length and width.
By doubling the width in $(W/L)_{3,4}$ gain is increased to 56 dB.
$(W/L)_7$ is also doubled which resulted in gain of 59 dB. $(W/L)_6$ is also doubled. Then gain is found to be around 64 dB which seems satisfactory. All the other parameters such as GBW and SR were checked in every step to be within specified value. To increase phase margin and GBW, $I_7$ can be increased but this in turn results in a decreased gain.

Analog design involves lot of tradeoffs, increasing or decreasing one parameter to meet one specifications result in a change in the other specification. After some variations to meet the required specifications keeping in mind the power consumption to be low, the values of transistor aspect ratios, bias current, compensation capacitor and nulling resistor determined are shown in Table 2.

Table 5.5 Transistor Sizes of Opamp used for Design of Integrator

| PARAMETER | VALUE |
|---|---|
| $I_B$ | 10μA |
| M1 M2 | 11.52 μm/0.36 μm |
| M1 M2 | 11.52 μm/0.36 μm |
| M4 | 1.45 |
| M5 | 0.42 μm/0.18μm |
| M6 | 23.976 μm /0.36 μm |
| M7 | 9.46 μm /0.36 μm |
| M8 | 0.42 μm /0.18μm |
| $C_C$ | 0.5 pF |

## 5.3 SWICTHED CAPACITOR INTEGRATOR DESIGN

### Sizing of Capacitors

The sizing of capacitors is the first step to be able to realize a fully functional circuit realization of a SDM, due to the fact that too small capacitors will introduce unwanted

thermal noise at the output of the SDM, which might decrease the SNR, and too large capacitors will result in increased requirements on the OTA's due to the larger load. Thus there is need to choose the capacitors to be as small as possible in order to let the OTA's drive the smallest load possible, and to still make the capacitors large enough so that the desired SNR is still fulfilled.

The switches connected to ground or virtual ground is realized using nmos switch to reduce the charge-injection effects [16].

Before calculating the different capacitor sizes, an estimation of the total amount of noise power which is allowed at the output of the modulator due to thermal noise is necessary. This can be determined according to the eq. (5.17)

$$\sqrt{\frac{kT}{C_1}} < \frac{LSB}{2} \tag{5.15}$$

where LSB = least significant bit

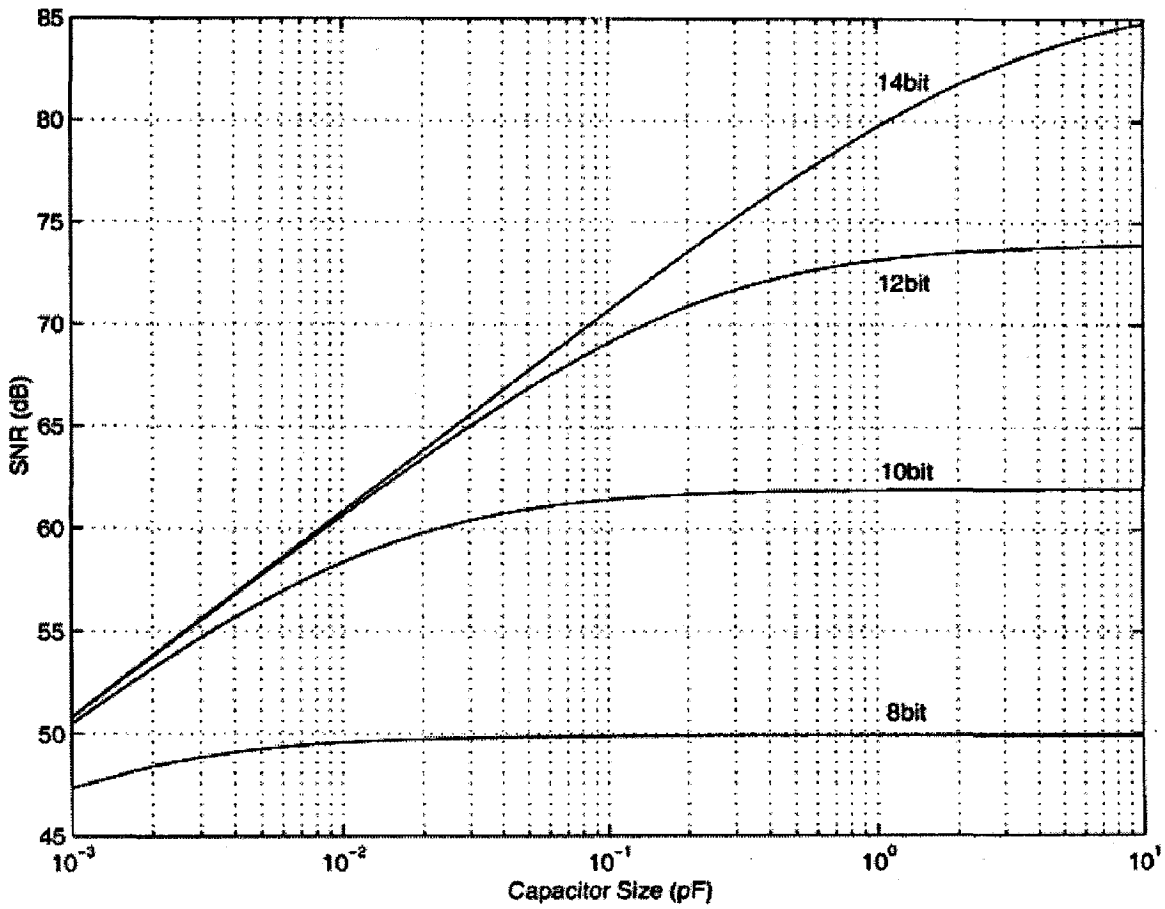



Fig. 5.2 SNR vs. Different Sampling Capacitance [22]

In Figure 3.11, the maximum SNR versus different sampling capacitor values is plotted. In practice, minimum size capacitors for a given noise requirement should be chosen to reduce power consumptions [22].

The sizing of capacitors should not be too small as they will introduce unwanted thermal noise at the output of the SDM, which might decrease the SNR, and too large capacitors will result in increased requirements on the OTA due to the larger load and also increase the area occupied by the SDM.
Depending on the gain coefficient needed for the integrator the values of $C_1$ and $C_2$ are determined.

For 1st integrator to realise b1=0.5,
$C_{ref} = C_1 = 1$ pF and $C_2 = 2$ pF

For 2nd integrator to realise b2=0.4,
$C_{ref} = C_1 = 1$ pF and $C_2 = 0.25$ pF

## 5.4 COMPARATOR DESIGN

Transistors M4, M7, M10, M11 constitute the cross-coupled inverter pair structure which forms the main regenerative loop for the latch.
The cross coupled inverter pair was first separately designed. Each inverter follows the typical rule of CMOS inverter transistor sizing i.e. the size of PMOS is almost equal to two times size of NMOS. Then the sizes of these transistors were optimized so that the DC biasing is kept a little bit more than the mid point of supply voltage. Also the widths of the transistors were kept minimum size i.e. 0.18 μm to cater for speed as a digital design and their sizes for length and width are kept minimum for least capacitive effects. Sizes are further optimized to set the metastable trip point of the inverter to half of the supply voltage.
Transistors M2, M5, M6, M8 are sized so as to obtain threshold voltage of inveter to be midpoint of supply voltage i.e. 0.9 V. The remaining transistors are sized to work as switch with high resistance when off and low on resistance and at the same time designed

to keep intrinsic capacitances low. The thus designed comparator's transistors sizes are tabled in Table 5.6.

Table 5.6 Sizes of the Transistors for Dynamic Latched Comparator

| **PARAMETERS** | **VALUE** |
|---|---|
| M1, M3, M4, M7 | 2μm/0.18μm |
| M2, M5, M6, M8 | 0.2μm/0.18μm |
| M9 – M12 | 4μm/0.18μm |
| v1, v2 | 0.38 V |

The NAND based SR latch designed has the transistors all with $W/L$ = 8.8. This is designed to obtain a propagation delay of about 200 ps.

$t_{PHL}= t_{PLH}=0.7R_{eff}C_L$ is the equation for propagation delays where Reqn= 12.5 kΩ/□.

Thus, all the building blocks topology was chosen to reduce distortion and the designed for 1 V supply voltage. These blocks are used in the design of second order SDM.

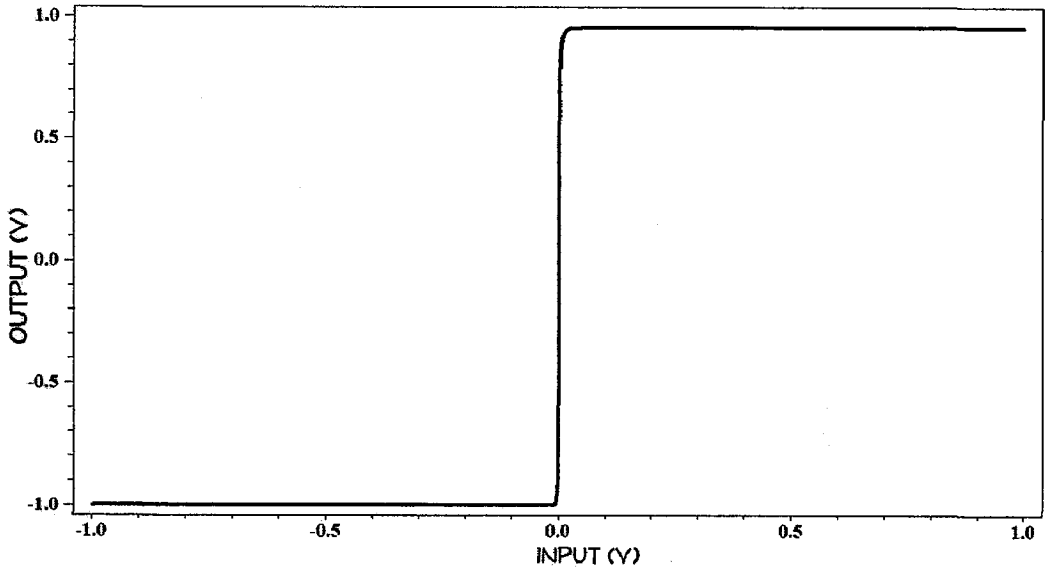
# Chapter 6

# RESULTS & DISCUSSIONS

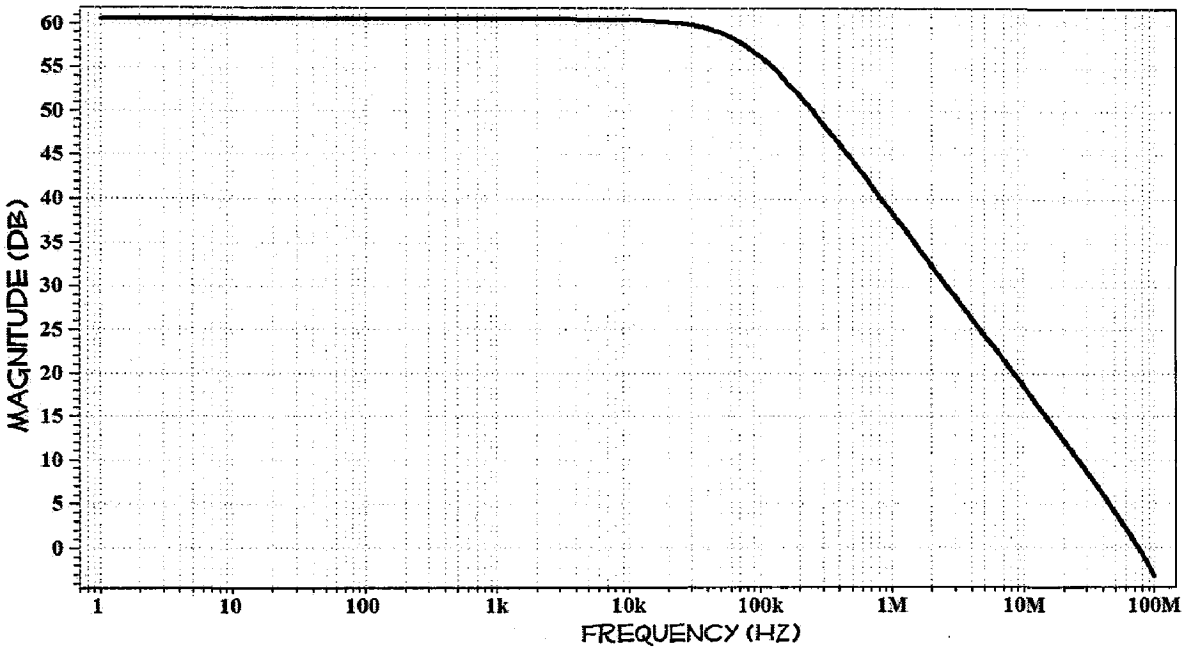
In this section all the simulated waveforms of the opamp, integrator, comparator, designed are presented. The simulations were carried out in T-Spice at 180nm technology node with a power supply of 1V

**OPAMP**

**TRANSFER CHARACTERISTICS OF OPAMP**




**MAGNITUDE RESPONSE OF OPAMP**

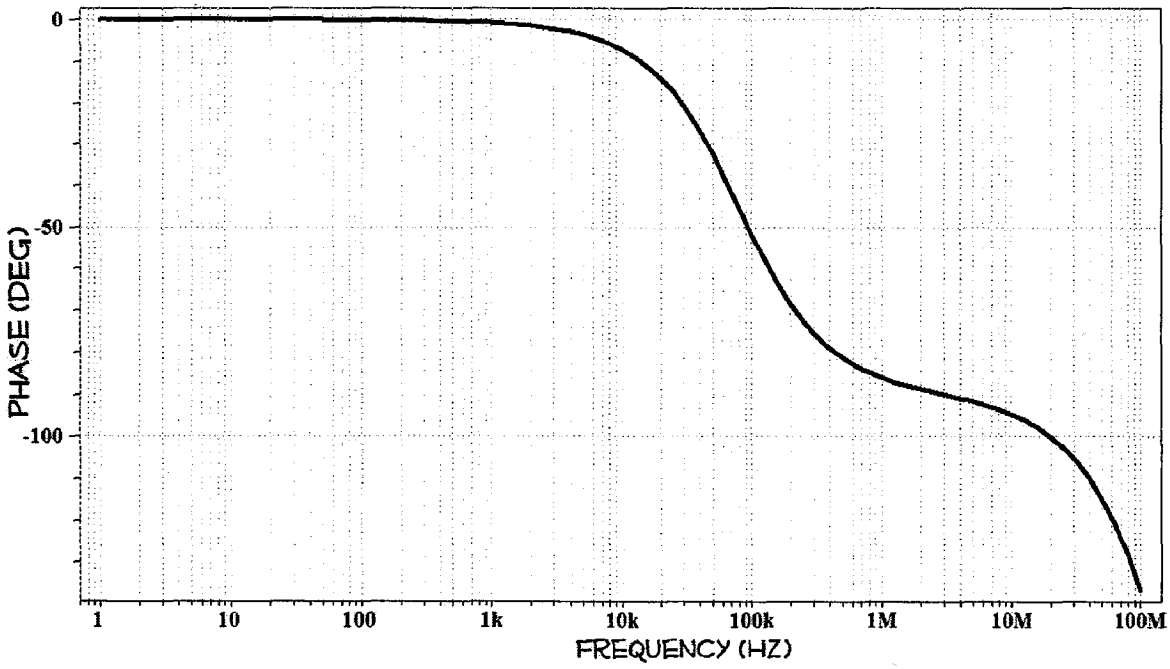



From the magnitude response the DC gain and the unity gain bandwidth are measured.

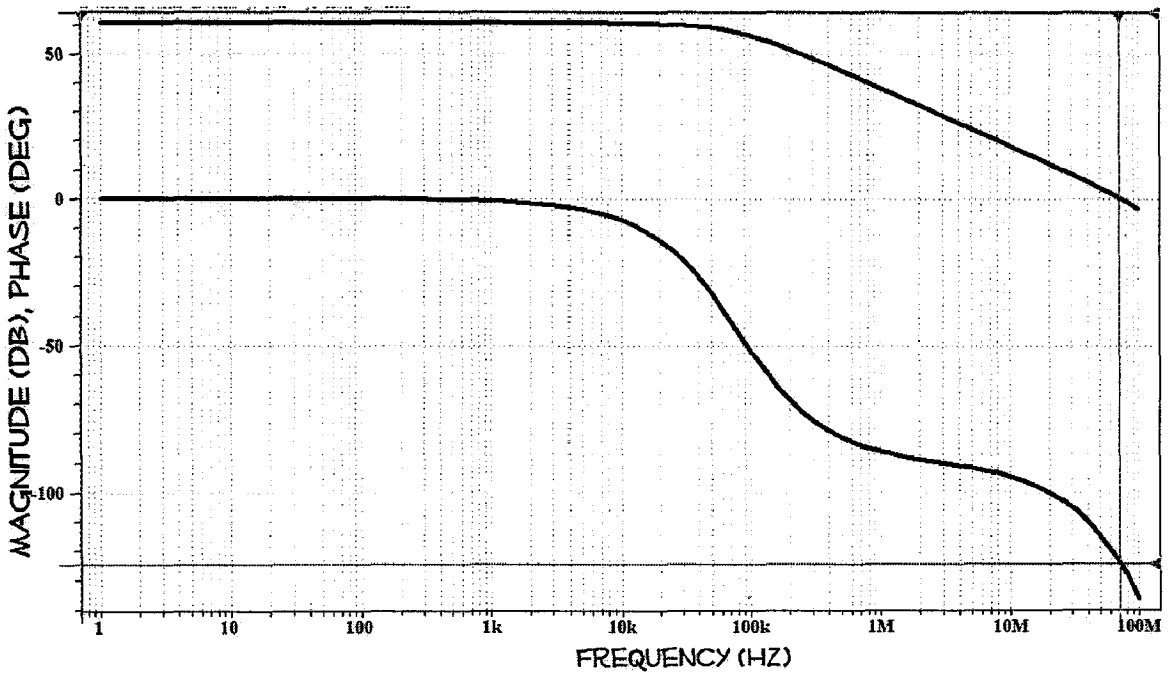
Gain of the OPAMP is thus 64 dB

Unity gain bandwidth = 70 MHz

**PHASE RESPONSE OF OPAMP**




**MAGNITUDE & PHASE VS. FREQUENCY**




From the phase characteristics, phase margin of the open loop system (Opamp) is measured. A phase margin of $60^{o}$ is necessary to avoid ringing at the output in a closed loop system i.e., when this opamp is used in any closed loop configuration [16].

Phase Margin is given as,

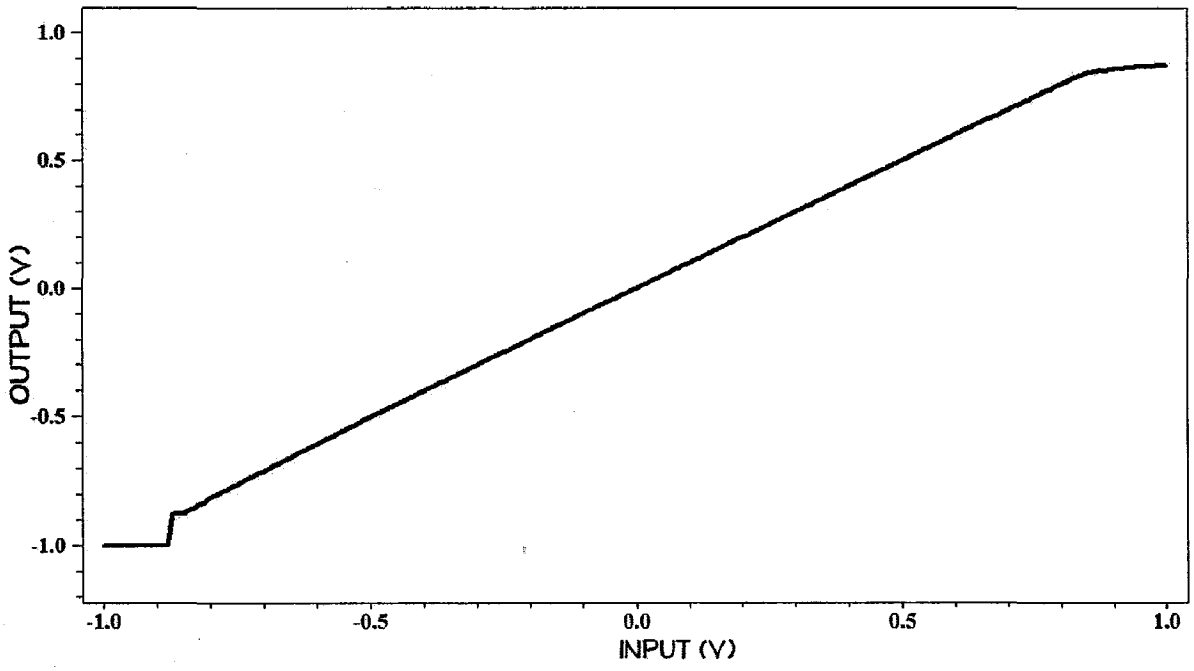
$$PM = 180^{o} + \theta \qquad \text{(Eq. 41)}$$

where $\theta$ is the angle corresponding to the frequency at which the gain of the opamp is 0 dB.

At gain cross over frequency the phase angle is $-120^{o}$

Therefore, Phase Margin = $180^{o} - 120^{o} = 60^{o}$

**FOR MEASUREMENT OF INPUT COMMON MODE RANGE**




$CMR^{-} = -0.85$ V

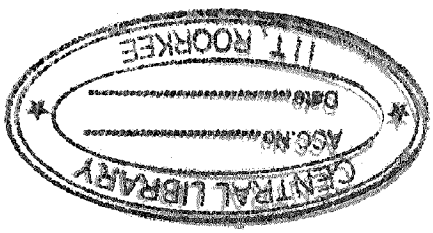
G14333

$CMR^{+} = +0.85$ V

Thus, input common mode range = 1.7 V.

The input and output waveforms for an opamp operated as a voltage buffer can be used to measure CMRR and SR.

The common mode voltage gain is found to be equal to 100KdB from the frequency response graph shown below.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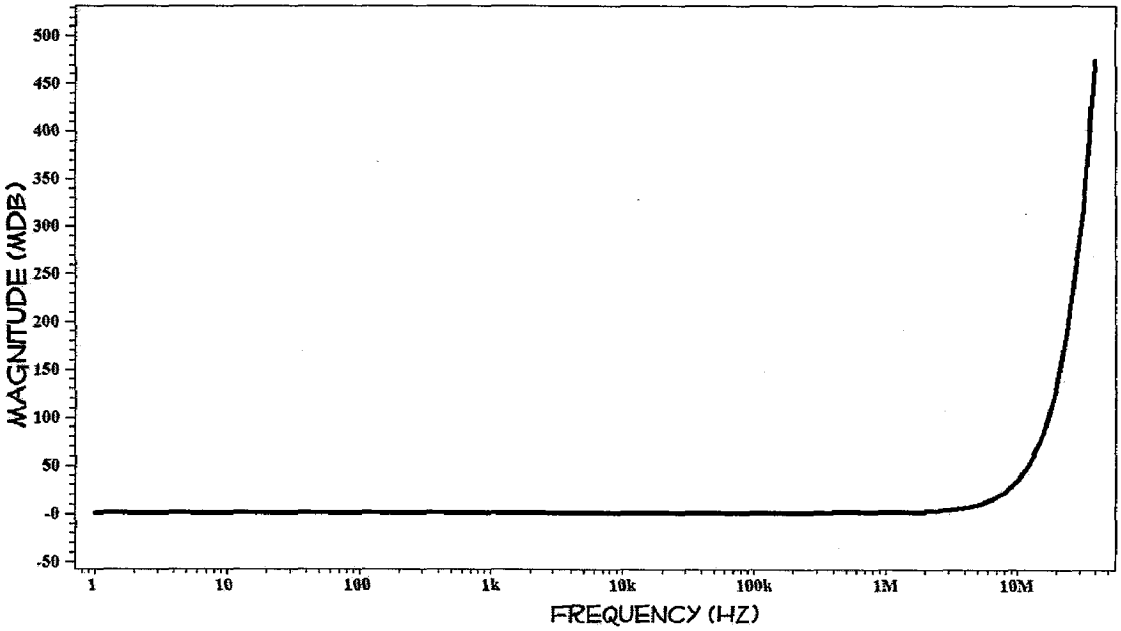
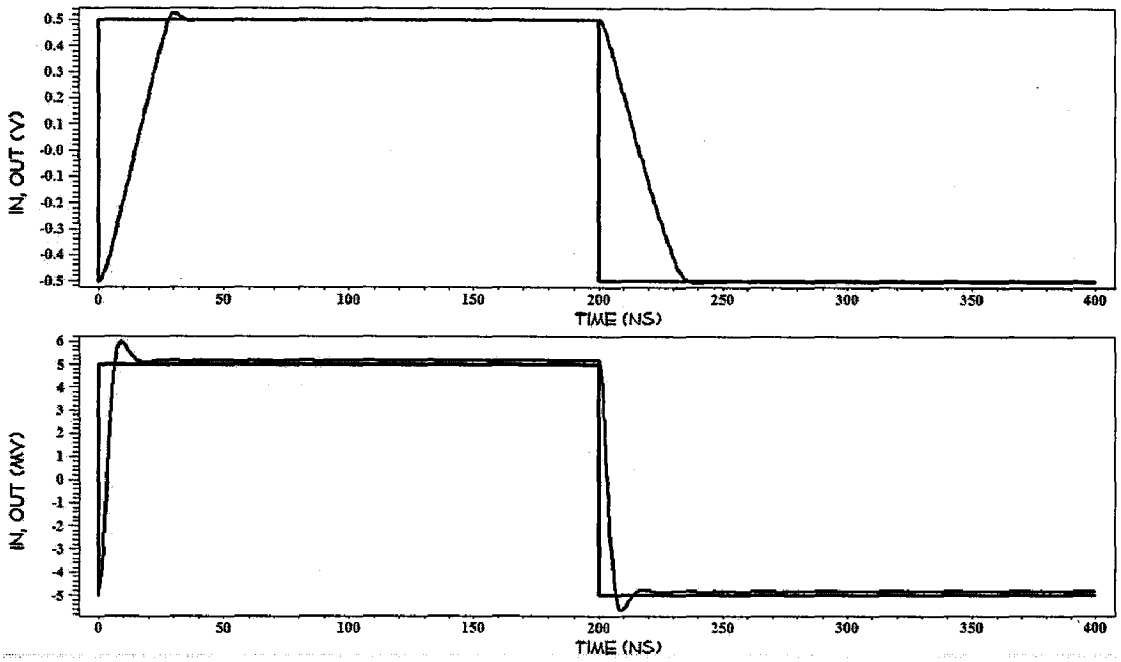
**COMMON MODE FREQUENCY RESPONSE**




**OUTPUT FOR INPUT PULSE WITH AMPLITUDE= 0.5 V & 5 mV**




Slew rate of the opamp determines the speed with which the switched opamp can be switched. The slew rate mainly depends on the load capacitor and the compensation capacitor. To achieve higher slew rates driver transistor current capacity has to be increased, in this design the current through the driver transistor M1 and M2 has to be increased in order to achieve higher slew rate.

From the output pulsed wave form slew rate is calculated as,

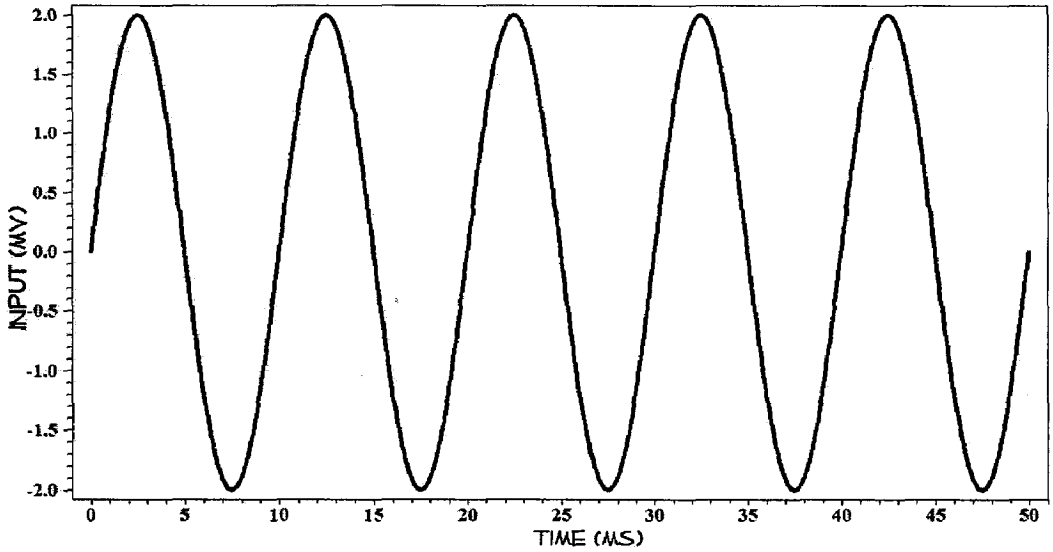
Positive Slew Rate = 13.4 V/μs

Negative Slew Rate = 11.9 V/μs

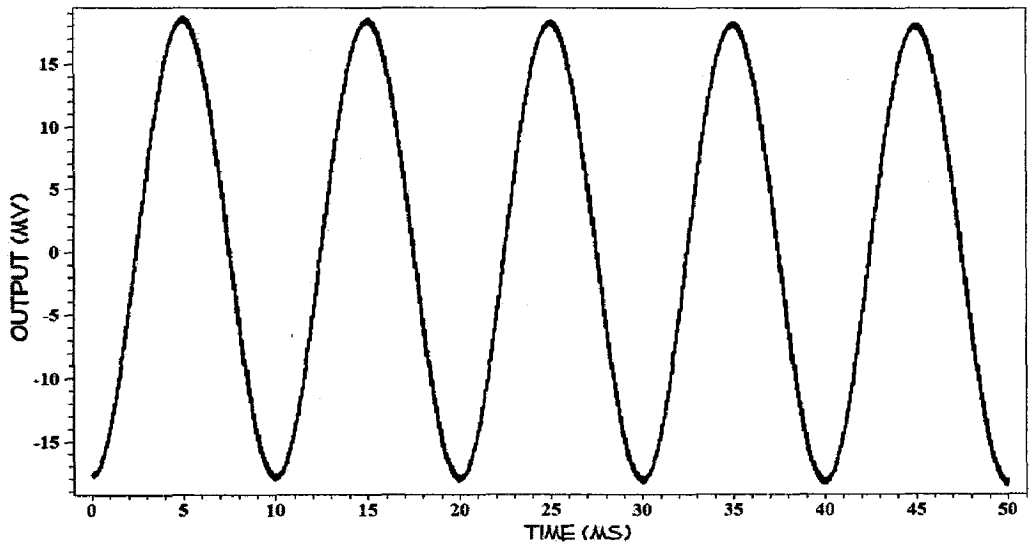
SR = 12 V/μs

**INTEGRATOR**

**INPUT WAVEFORM**




**OUTPUT WAVEFORM**




The opamp designed in the above section is used in SC integrator and feedback capacitor and input capacitors are taken to be 1 pF and 2.5 pF.The input sine wave with 200 Hz frequency and clock with 25 kHz frequency is applied to check the performance of SC

integrator. The integrator gives a cosine wave if input is sine wave and thus integration operation is verified.

The outputs for integrator for

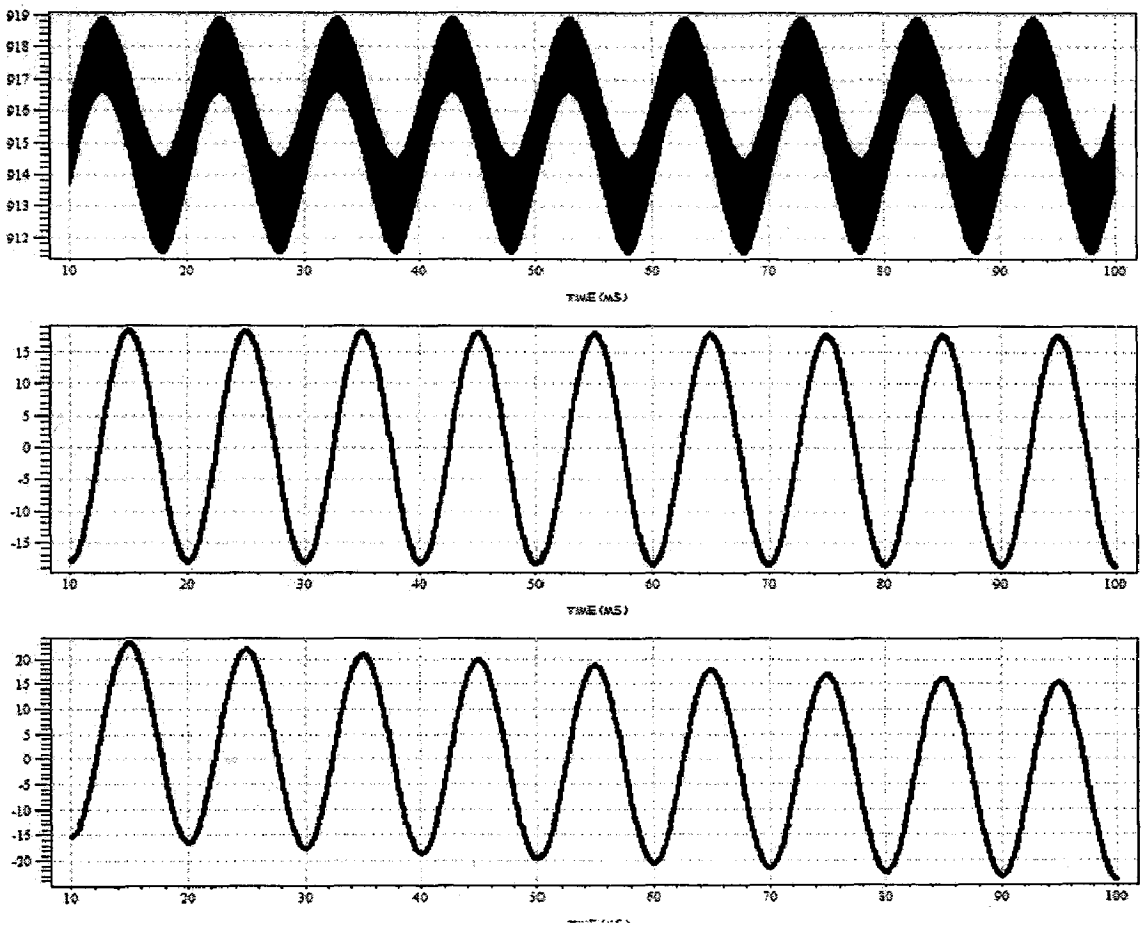
[1] C1/C2 = 0.05 pF/ 0.1 pF

[2] C1/C2 = 1 pF/ 2pF

[3] C1/C2= 5 pF/ 10 pF

It is observed that as the capacitor value goes down, output of integrator becomes noisier. If high value of capacitor is used with thermal noise reduction as aim, it is observed that the opamp designed doesn't allow high values of capacitors of about 3-4 pF due to overloading.

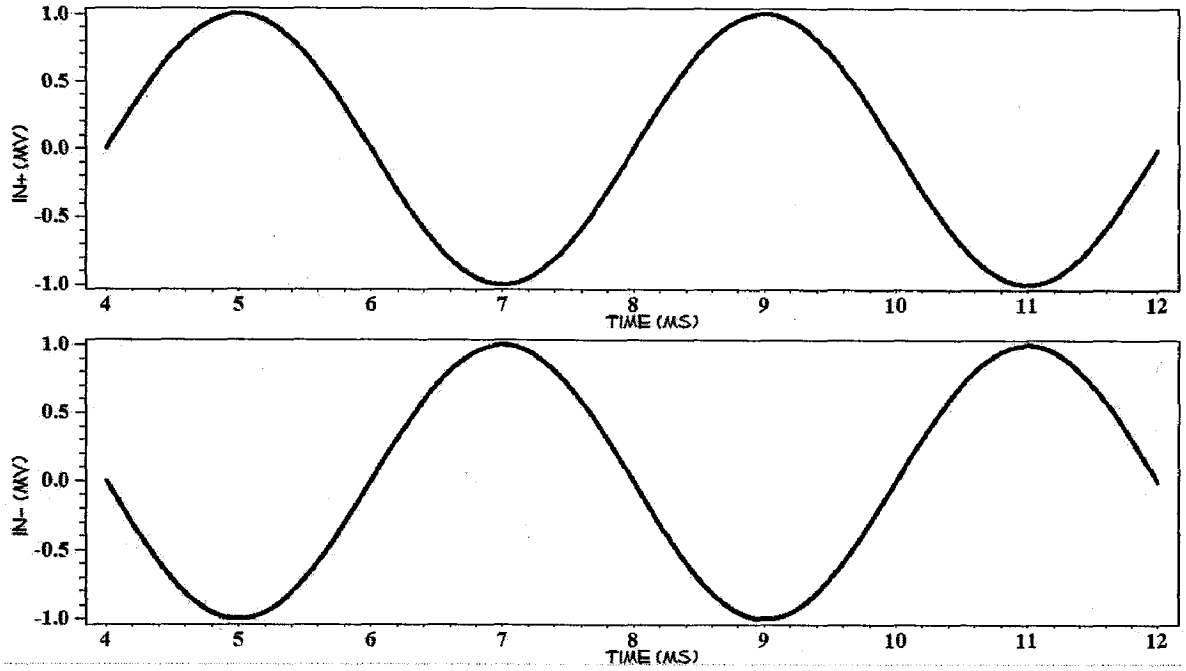
**OUTPUT OF SC INTEGRATOR FOR DIFFERENT SIZE CAPACITORS**



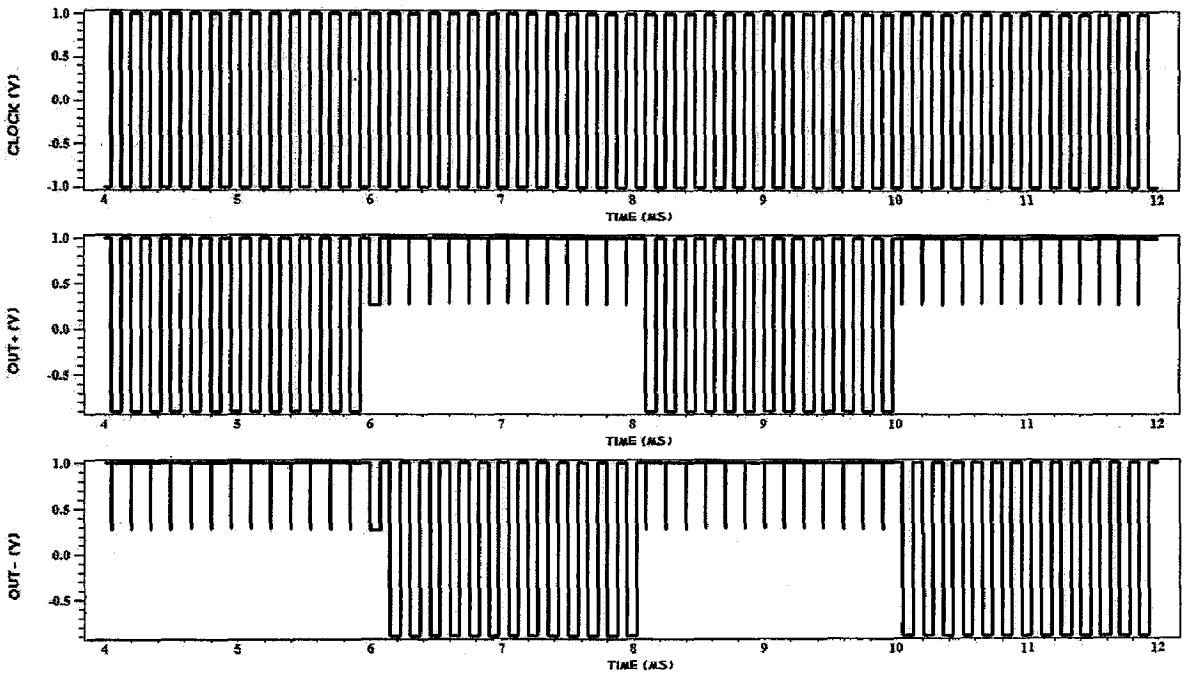
## DYNAMIC COMPARATOR

The dynamics comparator designed was tested with sine and cosine wave given to both differential inputs clock signal and output at nodes o- and o+ are observed wrt clock to see the working of comparator.

**INPUTS FOR COMPARATOR**



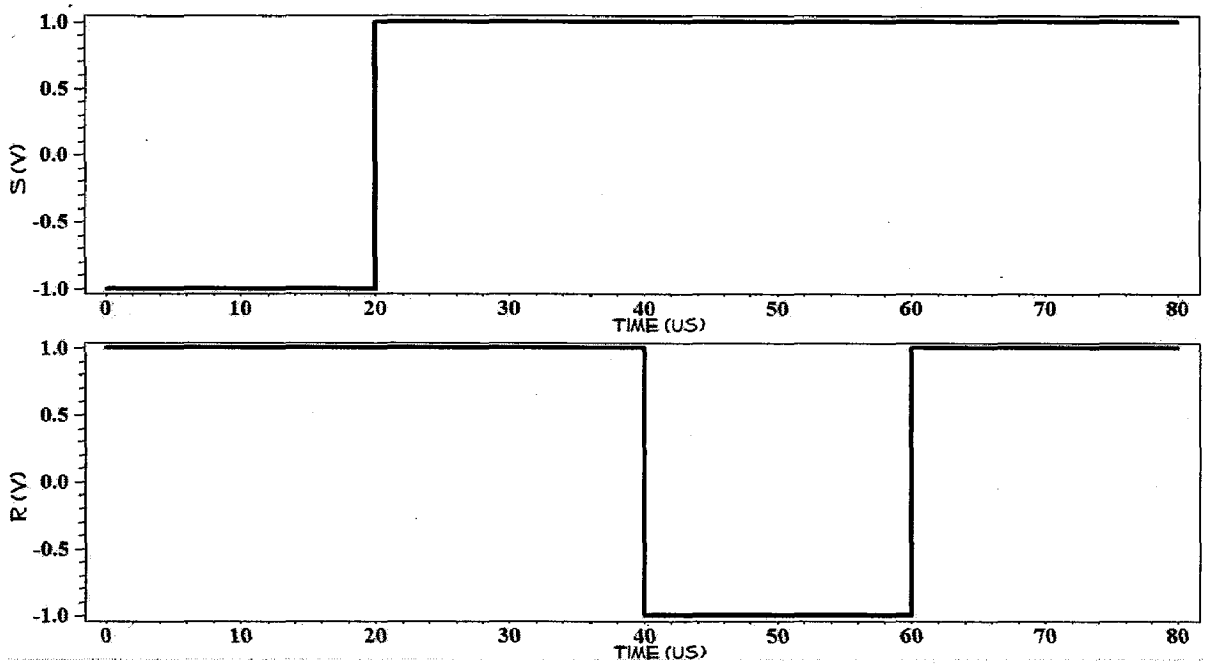

**DIFFERENTIAL OUTPUTS WRT CLCOK**



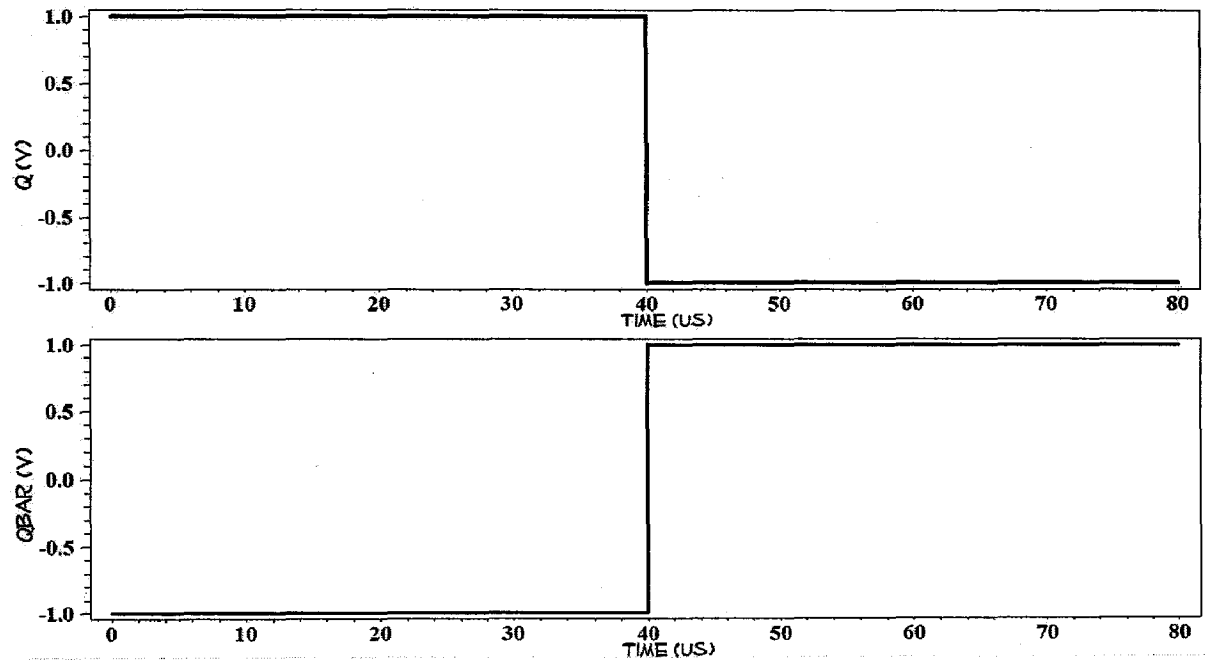
## SR LATCH

The SR latch designed was tested for its operation giving bit vectors S = [ 0 1 1 1 ] and R= [1 1 0 1] to S and R inputs respectively. While S=R=1 it holda its previous value. When S=0 & R=1 output is reset and S=1 & R=0 output is set. Input S=R=0 must be avoided.

**S and R INPUTS**



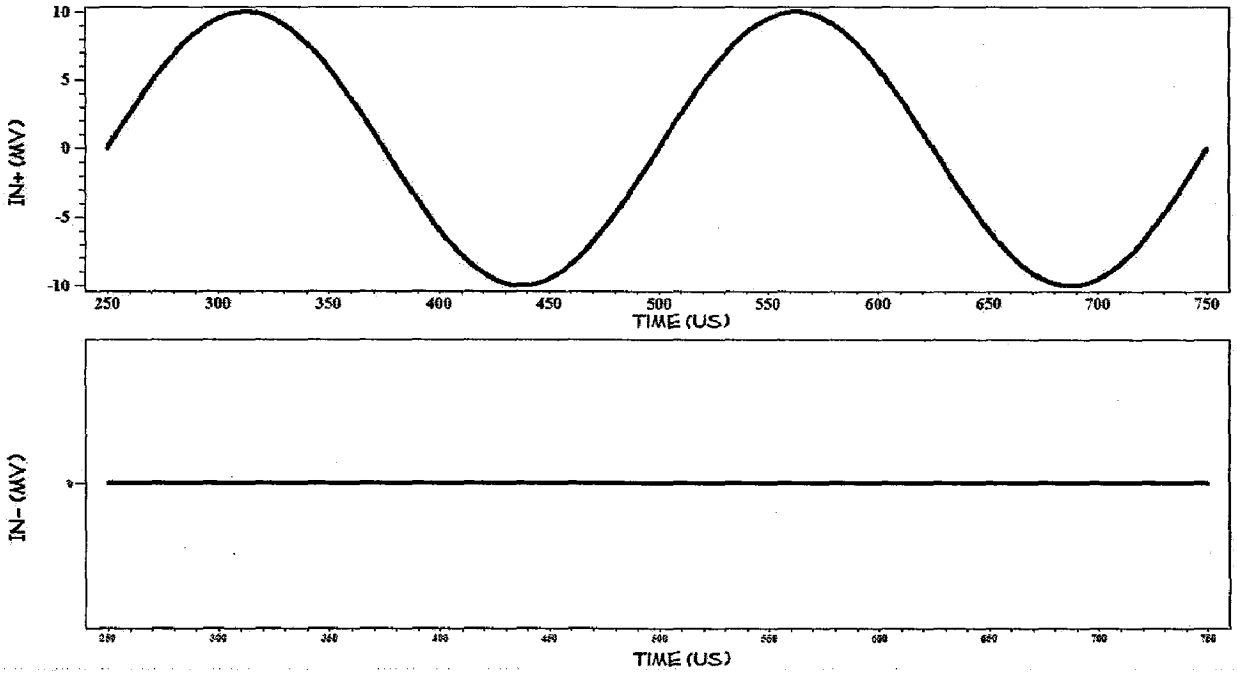

**Q and Qbar OUTPUTS**



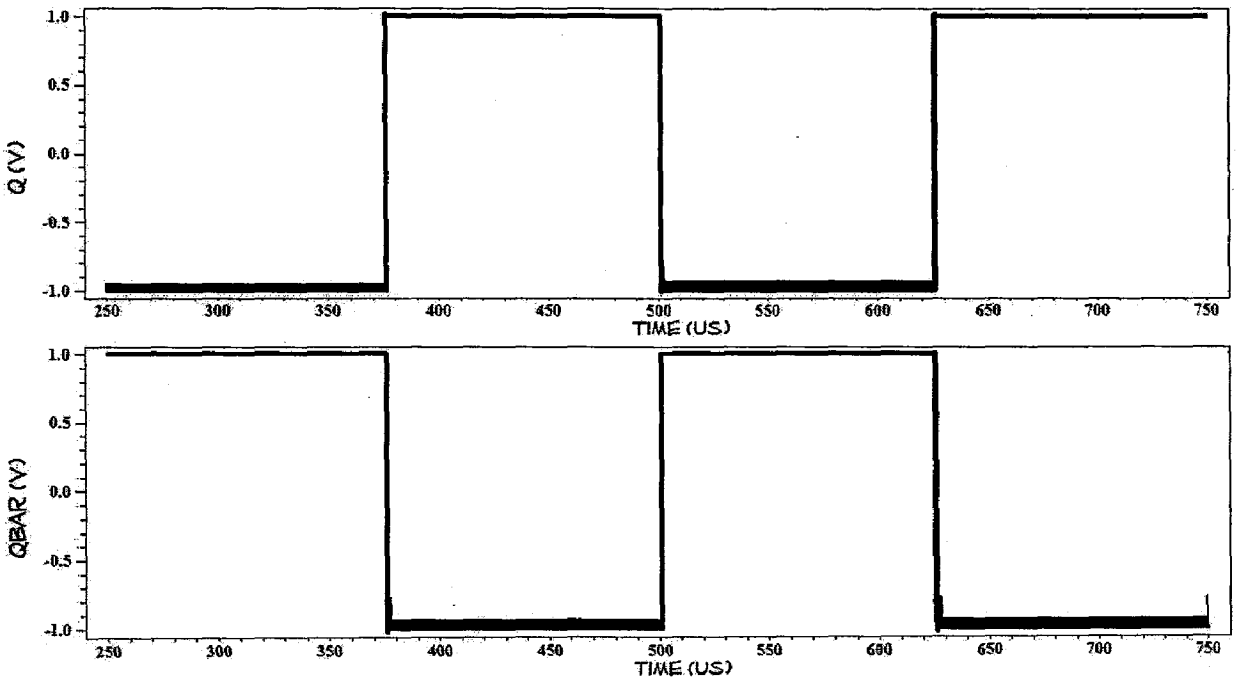
## DYNAMIC LATCHED COMPARATOR

The dynamic comparator is combined with lacth to give output in bits according to its input value. The input sine is of 4 kHz frequency and the comparator is operated with clock frequency of 1 MHz.

**INPUTS TO LATCHED COMPARATOR**



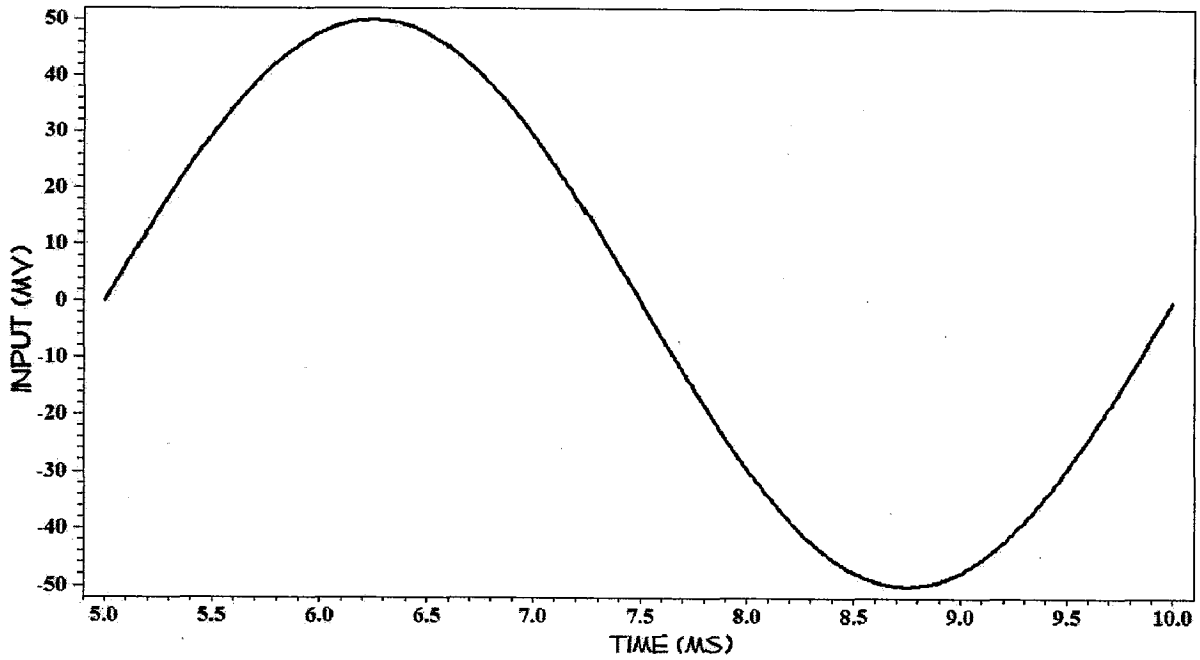

**OUTPUT OF LATECHED COMPARATOR**



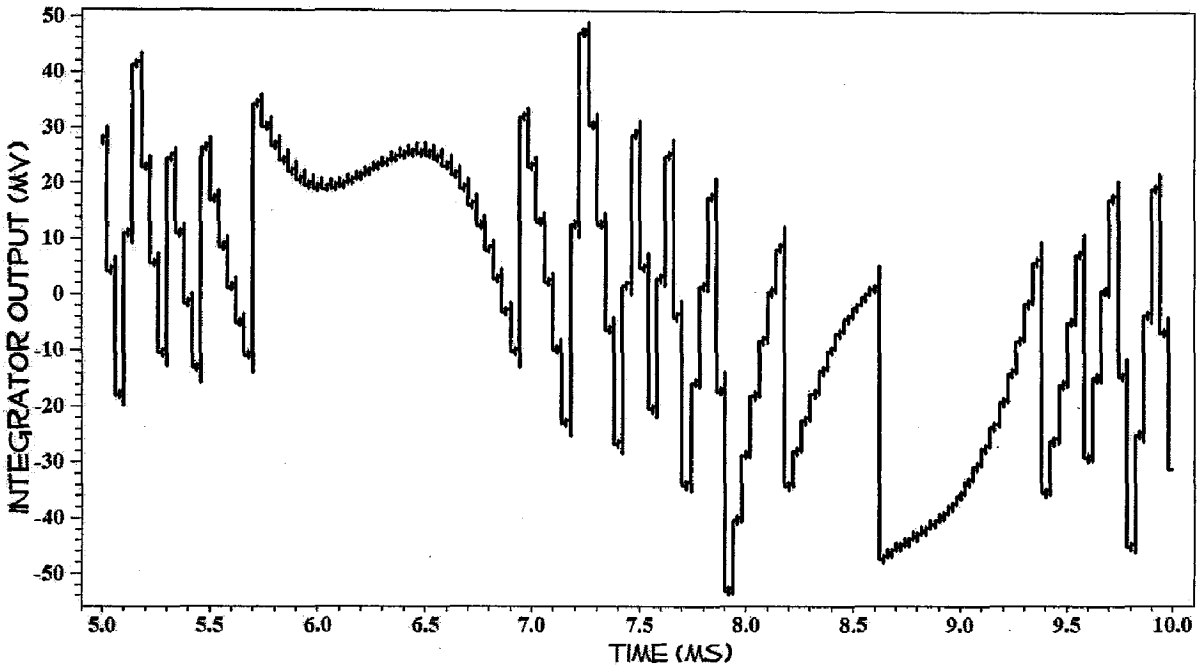
## SIGMA DELTA MODULATOR

The output of 2nd order SC Sigma Delta Modulator for a sine wave of frequency 200 Hz with ac amplitude of 10 mV using sampling frequency of 25 kHz produces the output of integrator and comparator as shown below.

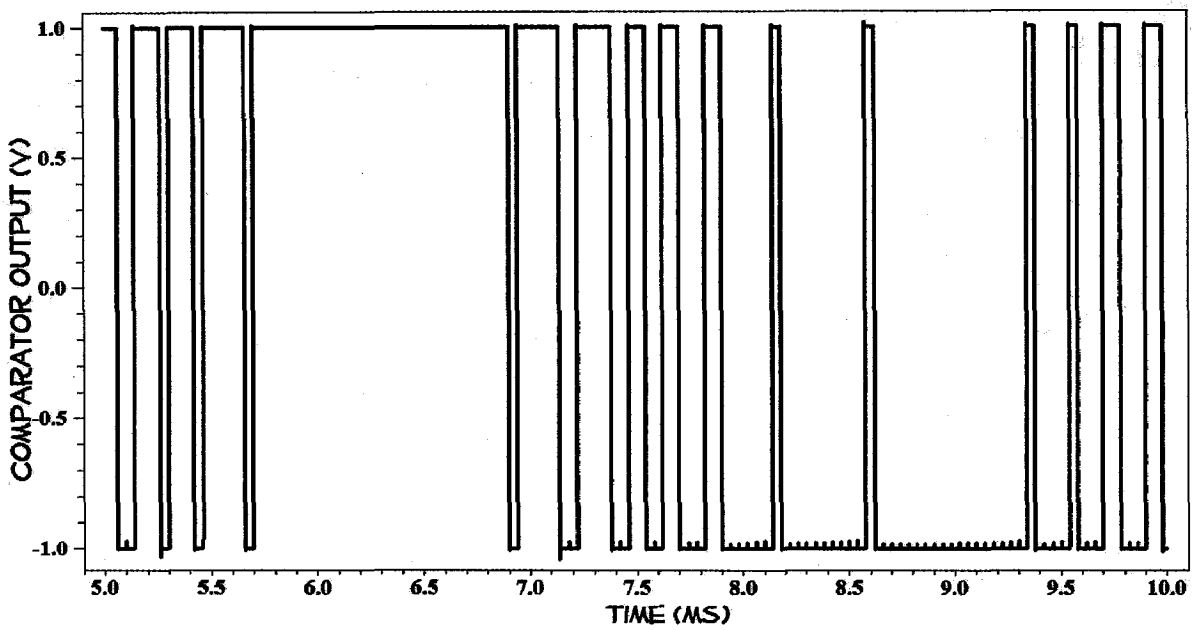
**INPUT TO MODULATOR**



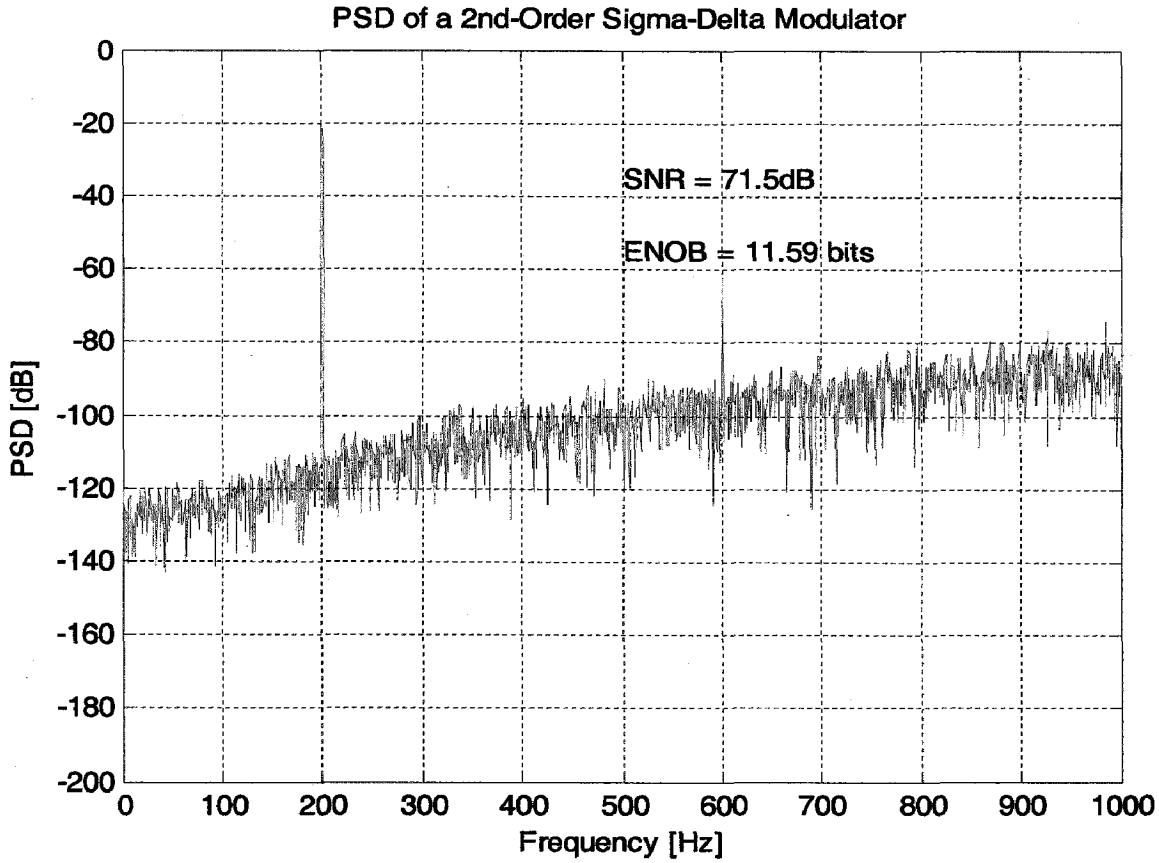

**OUTPUT OF SC INTEGRATOR**



**OUTPUT AT DYNAMIC LATCHED COMPARATOR**




From these output values, the SNR for the SC based SDM is obtained using MATLAB. The SNR was found to be 71.5 dB, which satisfies the resolution of > 10 bits.



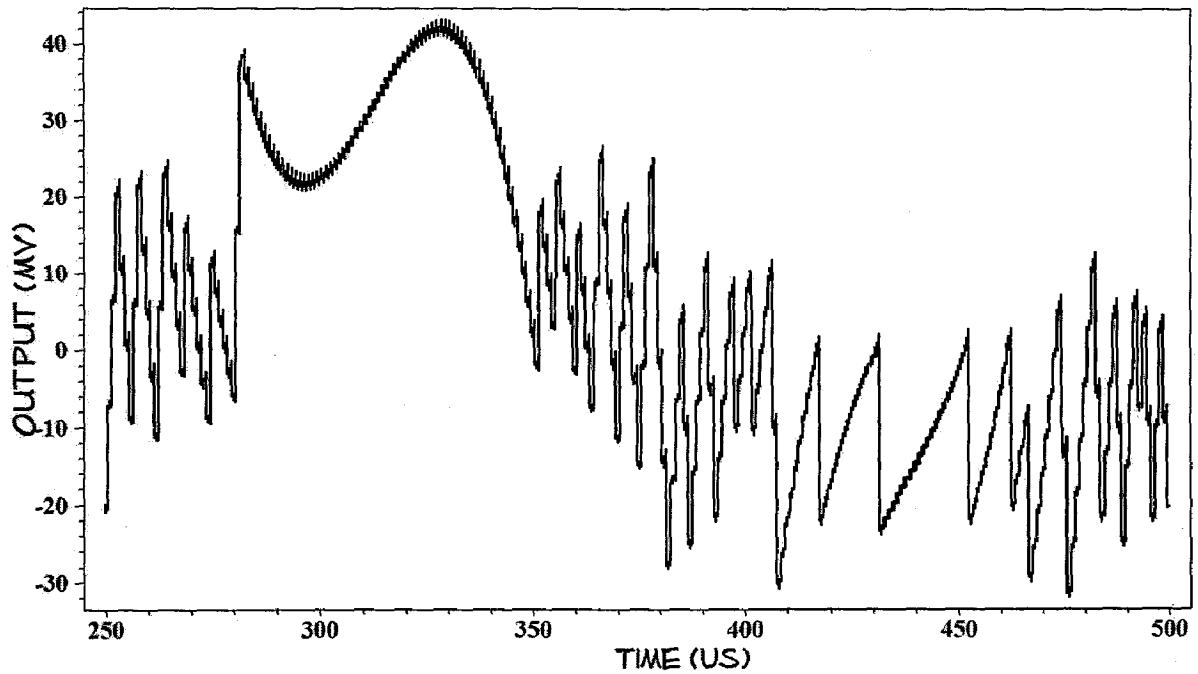
But, for high frequencies at low voltages the operation of SC fails due to the presence of 'critical switches' as discussed earlier. SO is not a good choice for high frequency applications. AZI was implemented in sigma delta modulator to operate with clock frequency 1 MHz.

Now, the sine wave of 4 kHz frequency is applied to the sigma delta modulator using AZI integrator, with sampling frequency of 1 MHz.

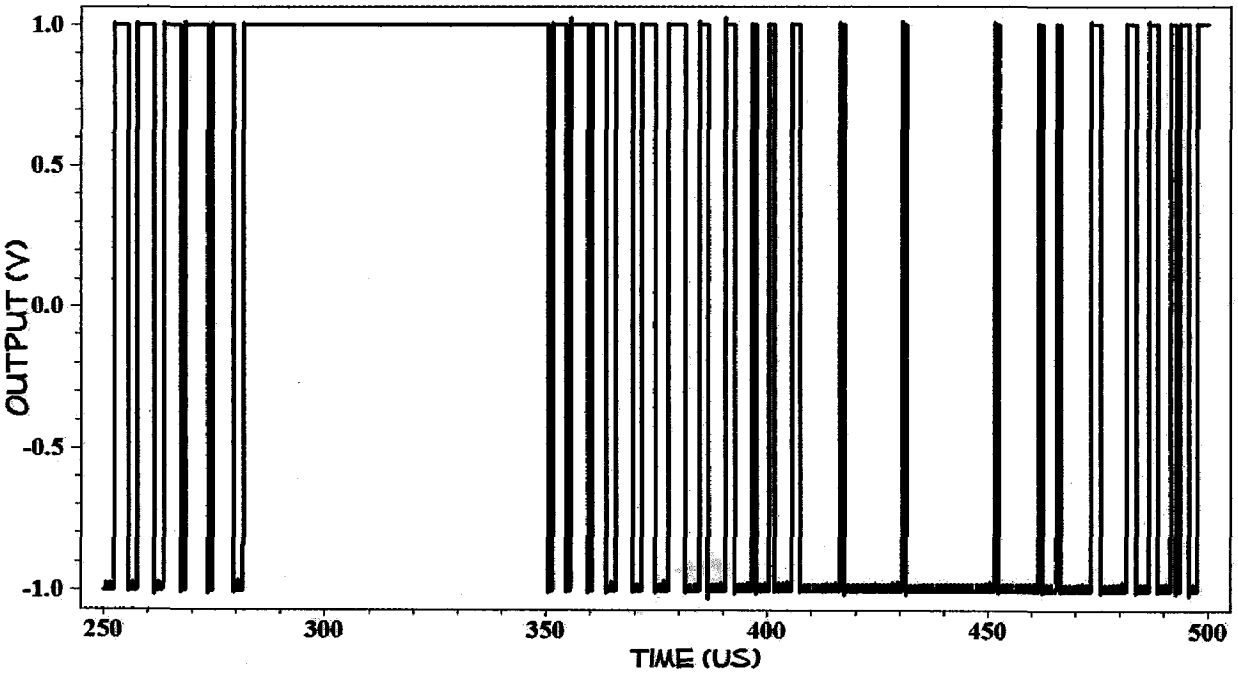
The output digital bits are sampled at clock frequency and these values are used to calculate SNR in MATLAB. The thus calculated SNR obtained was about 69.2 db with SNR plot as shown below.

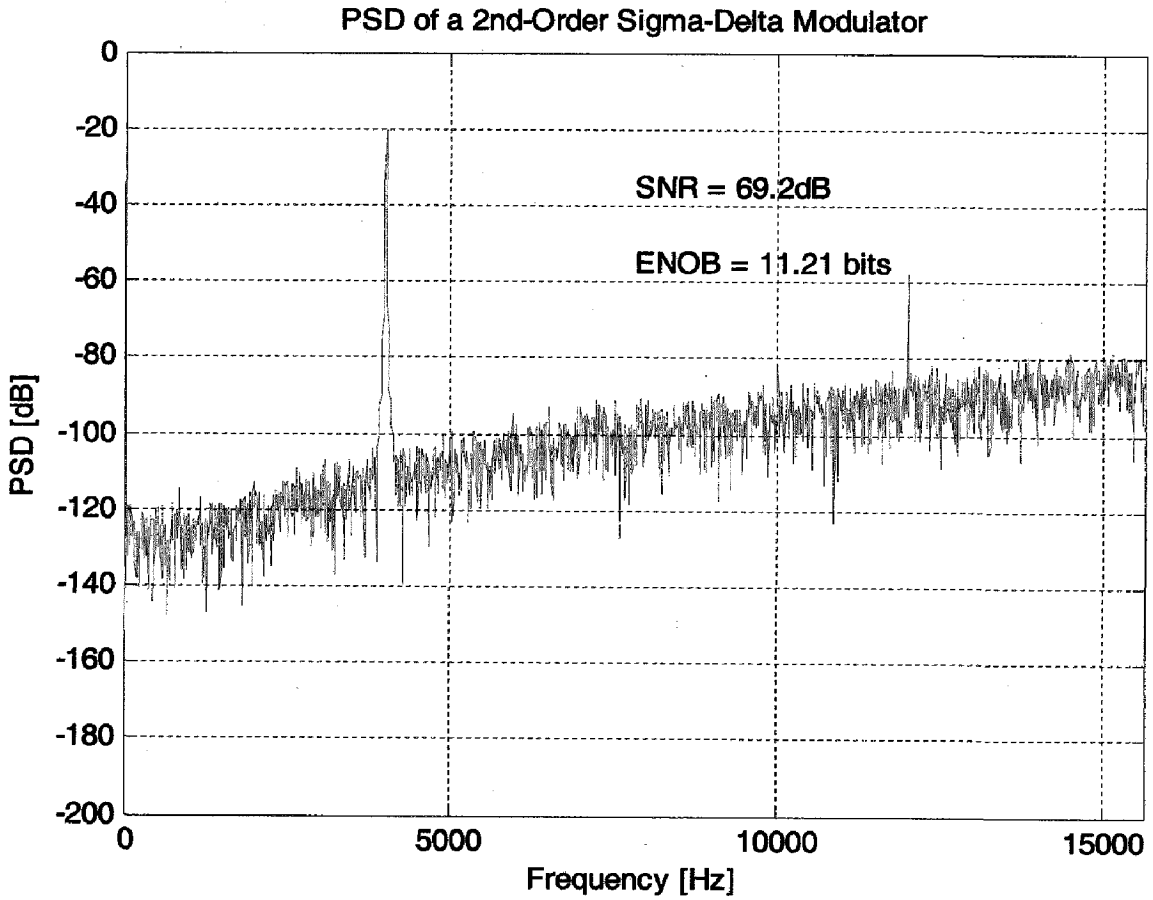
**OUTPUT ACROSS 2$^{ND}$ INTEGRATORS FEEDBACK CAPACITOR**

**( for i/p=4 kHz & clk=0.5 MHz )**



**OUTPUT AT DYNAMIC LATCHED COMPARATOR**



# Chapter 7

# CONCLUSION & FUTURE SCOPE

## CONCLUSION

The Sigma Delta Modulator has been used for ADC conversions to achieve high resolution with less precise components and also to meet low power requirements. To obtain a resolution > 10 bits, which is the resolution needed in biomedical applications, second order ΣΔM has been used with OSR of 64 at 1 V supply voltage.

Second order ΣΔM was behaviorally modelled to obtain optimum values for system level architecture and specifications for individual block requirements. The conventional SC based SDM showed satisfactory results at input bandwidths of around 200 Hz with sampling frequency of 25 MHz. But as the signal bandwidth is increased to 4 kHz the SC integrator's performance degraded slightly due the critical switch. Therefore, AZI was employed instead of conventional SC integrator for these frequency ranges. Thus, a low voltage low pass SC based ΣΔM has been designed with reduced nonidealities, so that dynamic range of > 10 bits is met.

## FUTURE SCOPE

This design of SC SDM can be extended by considering the nonidealities due to noise and clock feedthrough in the design of its building blocks.

This thesis designs the modulator at 1 V power supply with $V_{th} \approx 0.4$ V. The International Technology Roadmap for Semiconductors (ITRS) predicts that the threshold voltage of high-performance logic technology will continue to decrease to sub-0.1 V. The main problem with low Vth transistors is the presence of large subthreshold leakage.

To make analog circuitry compatible with the mainstream scaled digital circuits, modulator can be designed with low voltages of around 0.5 V with low $V_{th}$. For these modulators simple switches need to be replaced by Super Cutoff CMOS (SCCMOS) or Analog T - Switch schemes to reduce subthreshold leakage issues.

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# Appendix

# ADC PERFORMANCE METRICS

- DYNAMIC RANGE is the ratio of the largest to smallest signal that can be measured at one time and is normally reported in the Decibel scale.

- EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD - 1.76)/6.02.

- OSR: Oversampling ratio = $f_s/2f_B$, where $f_s$ is the sampling frequency and $f_B$ the input signal bandwidth.

- RESOLUTION is the smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in N bits, where the number of digital codes is equal to $2^N$.

- SIGNAL TO NOISE RATIO (SNR) (expressed in dB) is the ratio of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

- SNDR (SIGNAL TO NOISE AND DISTORTION RATIO) indicates in dB the ratio between the powers of the converted main signal and the sum of the noise and the generated harmonic spurs