DESIGN OF LOW LEAKAGE HIGH PERFORMANCE MGDG BASED SRAM at 32nm TECHNOLOGY NODE

A DISSERTATION

Submitted in partial fulfillment of the
requirements for the award of the degree
of
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in
ELECTRONICS AND COMMUNICATION ENGINEERING
(With Specialization in Semiconductor Devices and VLSI Technology)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being in this dissertation report, entitled "**Design of Low Leakage High Performance MGDG Based SRAM at 32nm Technology Node**", is being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Semiconductor Devices and VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work, carried out from June 2007 to June 2008, under guidance and supervision of **Dr. R. C. Joshi**, and **Dr. S. Dasgupta**, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not been submitted for the award of any other Degree or Diploma.

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CERTIFICATE

This is to certify that the statement made by the candidate is correct to best of my knowledge and belief.

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ABSTRACT

Logic and memory circuit design in nanoscale regime requires control over leakage currents and process parameter variations. Metal Gate Double Gate (MGDG) MOSFET has been proved to be vital in nanoscale regime for its leakage reduction with appropriate second gate bias and reduced sensitivity to process parameter variations. Unfortunately leakage minimization techniques using body bias forces the design to have increased transition time. We demonstrated that SRAM cell designed with MGDG-MOSFET has the benefit of reduced transition time. We did analytical modeling of the small signal capacitances that affect circuit operation from which glitch voltage at the output has been evaluated and validated through HSPICE simulations and less glitch voltage has been observed for MGDG MOSFET compared to the bulk case. Also, we estimated all leakage currents by considering interconnect effect and used them in finding voltage rise/fall at the critical nodes of SRAM cell. We have emphasized on low leakage, high performance robust cache subarray design with the help of MGDG devices. Suppressing leakage currents and maintaining constant Static Noise Margin (SNM) in ultra low voltage operation is crucial for circuit designers. We did SNM analysis of SRAM designed using our gate work function Engineered MGDG MOSFET and it is confirmed through HSPICE simulations that the cell is able to maintain constant SNM at ultra low voltage operation and more robust to process variations.

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Chapter 1

Introduction

1.1 Introduction

A closer look in recent technology nodes reveals that early signs of scaling limits were seen in high-performance devices. To obtain the projected performance gain of 30% per technology generation, device designers have been forced to relax the device subthreshold leakage continuously. Consequently, passive power density is now a significant portion of the power budget of a high-speed microprocessor.

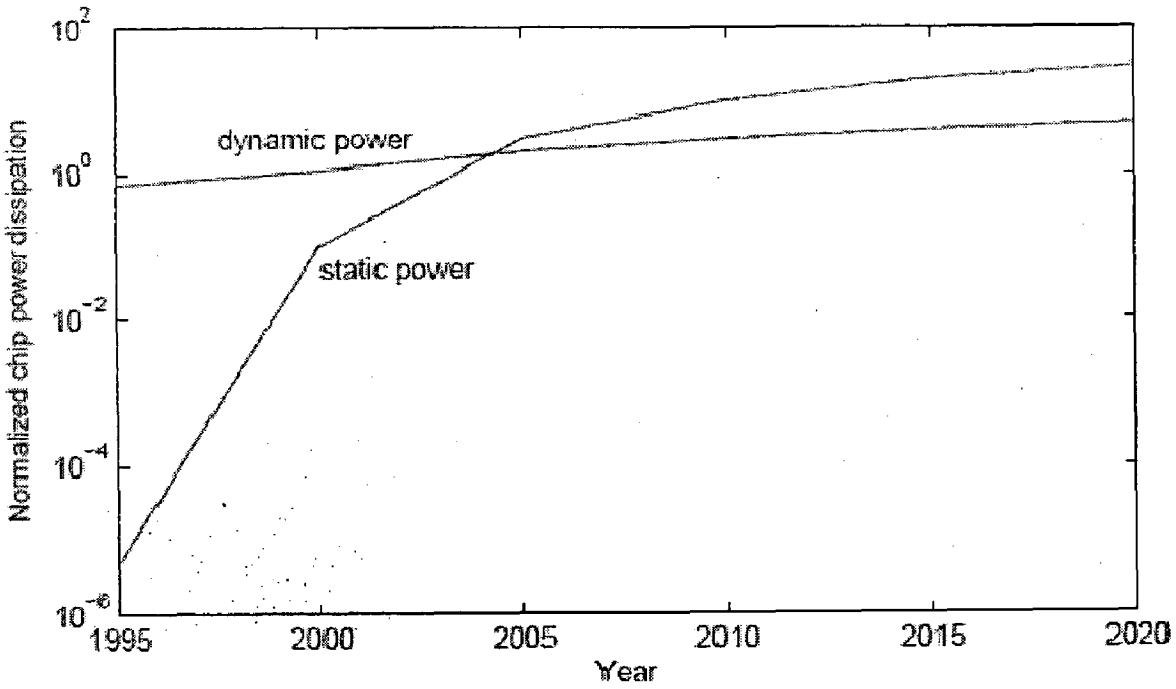


Figure 1.1 Power trends according to ITRS-2007 roadmap [1].

The increased variation of process parameters of nanoscale devices not only results in higher average leakage power (mean) but also in a larger spread of leakage power (standard variation). Some low leakage chips with too slow speed and some other faster chips with too high leakage have to be discarded. As a result, both power yield and timing yield are seriously affected by the process variations. Process variations are basically separated into inter-die and intra-die variation [2]. Inter-die variation or global variation refers to variations from wafer to wafer, or die to die on a same wafer while

intra-die variation or local variation occurs across an individual die that means on same chip devices at different locations may have different process parameters. Since inter-die variation affects all the devices on a chip in the same way, it has a stronger effect on circuit power and performance.

According to ITRS predictions, by 2014 memory is going to occupy 94% of chip area, so power consumption, performance and reliability of total system is determined by memory. Also, many high performance processors dedicate large fraction of their area to caches which are designed using SRAM. Proper attention is needed for standby power estimation, robust high performance subarray design of nanometer cache and its associated timing. Also, in sensor network nodes burst of activity occurs in response to an input event, and the system is otherwise idle for most of the time. Hence one should be able to operate at ultra low voltages [3].

1.2 Motivation

Design of nanoscale device providing high performance and reduced leakage currents with reduced sensitivity to process parameter variations is challenging at nanoscale dimensions. Estimation of small signal capacitances and leakages helps to estimate glitch voltage present at output and gives idea on robustness and performance of the circuit which reduces design time at higher levels of abstraction [4]. Also, leakage current determination using interconnection effect gives better insight into reliability of the circuit. At lower voltages ratio of on current ratio with backgate voltage of V_{dd} and 0V is more for MGDG MOSFET and this feature can be used for obtaining superior ultra low voltage characteristics than bulk MOSFET which will be more useful in sensor network nodes and improves battery lifetime.

1.3 Problem Description

Leakage and process variation are two major problems faced by the semiconductor nanometer technologies [2], [5], [6]. Designers have been forced to relax limits on subthreshold leakage to have 30% performance increase with each technology generation [1]. In addition aggressive scaling of gate dielectric causes catastrophic gate leakage [7] in nanometer regime. Further, as the silicon industry is moving towards the possible end of the roadmap, controlling the variation in device parameters during fabrication becomes a great challenge. Variations in process parameters such as oxide

thickness, channel length, channel thickness and dopant placement result in large variations in threshold voltage which subsequently threatens the yield of nanoscale circuits/memories [8]. Further the leakage minimization schemes involve additional transition time and lot of complexity in row decoder design.

In circuits operating at nanoscale regime voltage rise or fall at output node during signal transitioning events creates timing, noise and glitch related problems. So, to perform early power and timing estimates, one needs an efficient method to estimate the small signal capacitances of the selected device structure and leakage currents at respective nodes in the circuit using interconnection effect. Leakage currents also determines the potential rise or fall, so leakage current estimation using interconnection effect and solution of nodal current equations at different nodes of circuit gives better insight into the robustness of the circuit. Also, transition time and energy overhead required for the backgate biasing schemes needs to be considered for high performance and low leakage which can be estimated by finding semiconductor capacitance at optimum biasing point. Due to increased composition of memory in today's high performance processors power consumption, performance and reliability of total system is determined by Memory. Stand by Power can be minimized by reducing the supply voltage to a limit called data retention voltage (DRV) [9], [10] at which memory cell can just retain the data stored while reducing all leakage currents. Data retention voltage is further influenced by process variations of minimum geometry transistors used in present day technology. Maintaining almost constant Static Noise Margin (SNM) [2], [11], [12] across different process corners in ultralow voltage operation is still challenging.

1.4 Dissertation Organization

The dissertation organization is as follows:

Chapter 1 deals with introduction portion of the thesis.

Chapter 2 deals with review of design problems present in nanoscale bulk CMOS and introduce MGDG MOSFET as its solution. It reviews high performance low leakage circuit design in nanometer regime and leakage reduction methods of SRAM cell and their performance.

Chapter 3 deals with work function engineered MGDG MOSFET as its solution. It also describes leakage current estimation techniques of MGDG MOSFET.

Chapter 4 describes transition time and optimum biasing configuration and method to reduce the transition time. It also presents different types of failures present in conventional SRAM.

Chapter 5 deals with Small signal capacitance and glitch voltage modeling and estimation of leakage currents using interconnection effect and voltage rise/fall at critical nodes of SRAM cell and its validation through **HSPICE Simulations**.

Chapter 6 deals with ultra low voltage operation of SRAM cell designed using MGDG MOSFET. It also shows SNM variation across different process corners.

Chapter 7 gives conclusion and future scope of the work.

Review of Design Problems in Nanometer Cache Memories

2.1 Design Problems in Nanometer Bulk CMOS Technologies

Main Problems faced by CMOS Nanometer technologies are

- Maintaining a Good on to off current ratio.
- Exponential increase in leakage current.
- Process parameter variations.

In addition to above poly-depletion causes severe transconductance degradation as shown below.

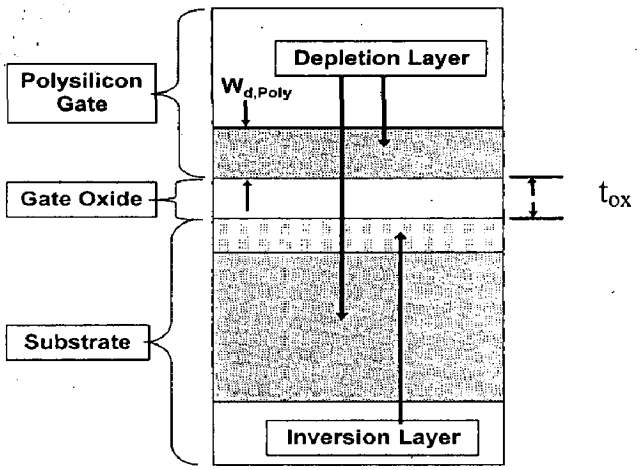


Figure 2.1 Poly-Depletion Effect [1].

Due to poly depletion effective oxide thickness will increase to [13],

$$t_{ox,electric} = t_{ox} + (K_{ox}/K_{si})^* (W_{d,Poly}) ; \quad \text{where } K_{ox} = 3.9 \text{ for } SiO_2,\ K_{si} = 11.9 \qquad (2.1)$$

From ITRS specifications Poly-doping is limited and its depletion become more critical with insulator thickness scaling, leading to severe transconductance degradation. Performance and robustness of the design decreases due to degraded transconductance. Unfortunately scalability of bulk devices is limited by process variations and severe short channel effects there by forcing the designers to search for new channel materials, unconventional devices. Double gate MOSFET is one such promising device which can extend the scaling limit to sub20nm [14]. A special class of DGMOSFET called MGDG MOSFET was reported in [15], which reduces sensitivity of leakage currents to process

parameter variations and also it eliminates poly-depletion effect. It has been proposed in [16] that midgap gates reduce performance of the design. Hence one should go for dual metal gate processes as reported in [17] for improved performance.

2.2 High Performance Low Leakage Circuit Design in Nanoscale Regime

High performance low power Nanoscale circuit design requires estimation and reduction of standby leakage power [4]-[6], [18]-[19]. A. Agrawal *et. al* [4] has reported leakage estimation procedure but it is limited to bulk MOSFET's. Circuit level technique of 'stacking' has been proposed in [18] as a way to reduce leakage currents and estimation of leakage currents in stacking has been reported in [20]-[21]. Stack effect is more effective in scaled devices due to increased stack factor and if MGDGMOSFET is used then due to reduced short channel effects there is not much benefit of stacking, also reduced driving capability limits the benefits of stacking in Double gate devices [15]. So, only option left for either improving performance in critical paths or reducing leakage in noncritical paths is backgate biasing. Backgate biasing fails if the channel is left almost intrinsic [22]. In case of DG devices one can finely tune threshold voltage with back gate biasing [23], [24] to achieve required leakage reduction as well as improved performance. Timing analysis of problems caused by backgate bias is required for estimating timing requirements of design. For MGDG MOSFET's timing analysis reported in [25] is not applicable since it does not give estimation of semiconductor film capacitance. A method of estimating semiconductor capacitance has been reported in [26]. Also, small signal capacitances present in the device causes voltage rise/fall in output levels and causes reliability problems [8], [27]. Moldovan *et. al* [28] have obtained small signal capacitances of intrinsic channel double gate device from explicit expression for mobile charge sheet density/unit area but, they have not given measure of glitch voltage present at the output of the circuit due to small signal capacitances. Modeling and analysis of various failure mechanisms present in the circuit is essential for finding reliability of the total system [8] [29]. Failure probability estimation in [8] does not include effect of leakage currents determined using interconnection effects and glitch voltage at the data storing nodes of the cell. Reduction of leakage currents and operation at subthreshold regime based on application demands [30]-[34] helps to reduce most of leakage currents to minimum. SRAM's uses minimum geometry transistors and they can be better used for characterizing the performance of nanoscale devices.

2.3 Conventional Leakage Reduction Methods of SRAM and Their Performance

The selection of leakage reduction scheme is governed by percentage leakage reduction and delay overhead caused by the scheme [25] as shown in figure 2.2. Study of effect on the read/write delay by each low leakage technique is required to estimate the circuit performance. The popular Device/Circuit co-designing schemes of low power SRAM cell are given in **Table 2.1**. Here sub: double down arrow indicates large reduction of subthreshold leakage If only one arrow is there only marginal reduction is available. Similarly Gate: double down arrow indicates large reduction of gate leakage and the same applies for BTBT.

Table 2.1 Selection of Co-design Scheme

Scheme	Source Biasing	Fwd/Reverse Biasing BG	Dynamic V_{dd}	Floating BL	Negative WL
Leakage reduction	Sub: ↓↓ Gate: ↓↓	Sub: ↓↓ BTBT:↑(RBB)	Sub, gate: ↓ Bitline leakage	Sub: ↓ Gate: ↓	Sub: ↓ Gate: ↑
Delay	Increases	No Increase	No Increase	No Increase	No Increase
Transition overhead	Low	Large	Large	Precharge latency	Low charge pump efficiency

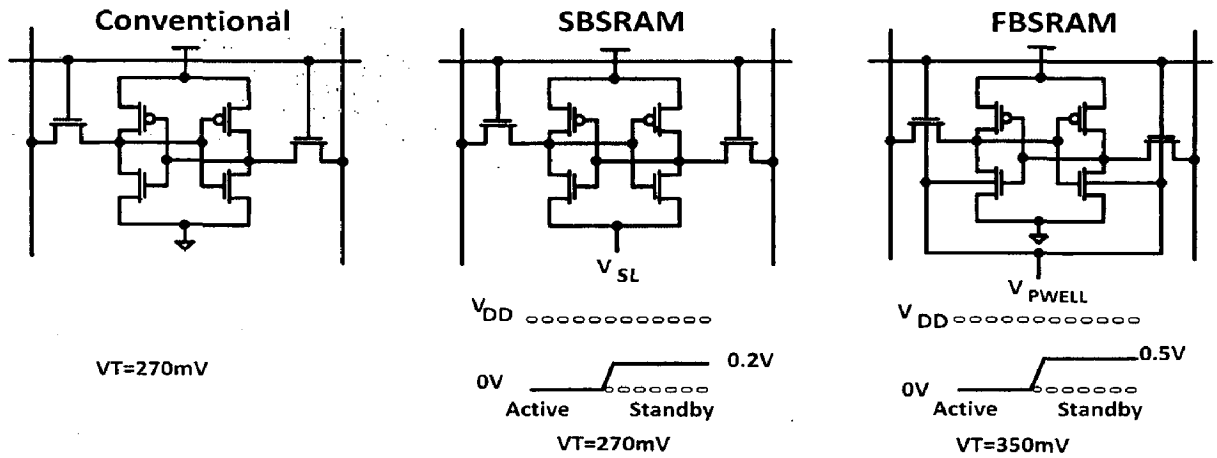


Figure 2.2 Biasing Schemes of SRAM Cell

Most commonly used methods of reducing leakage power are,

A. Self-Reverse Bias

Self reverse biasing schemes raise the source voltage of MOSFET thereby increase threshold voltage. The effect of transistor stacking on circuit topology was first proposed for subthreshold Current. In transistors connected serially, gate-to-source voltage is

more negative, when the transistor is top of the stack. Threshold voltage of the transistors at top of the stack is increased because of body effect. Hence, "OFF" transistors at stack have lower subthreshold current than individual transistors. Stacking has secondary effect of Drain induced barrier lowering (DIBL) and slight increase of V_{th}.

B. Back Gate Biasing for Leakage Reduction

Back gate biasing schemes focus on varying backgate bias for tuning front channel threshold voltage. All the leakage currents from both front and back gate have been calculated in above section. Leakage currents can be reduced by negative backgate bias and performance can be improved by positive backgate bias. This scheme introduces transition time as well as energy overhead and complicates row decoder design.

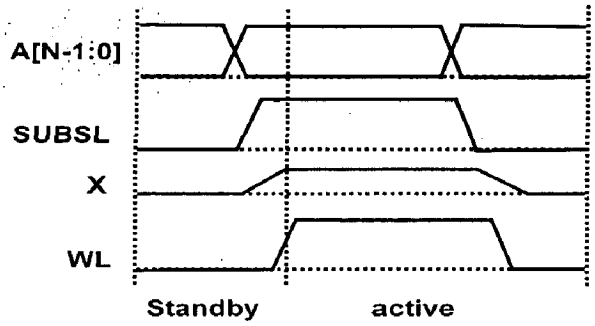


Figure 2.3 Wake up of Subarray in backgate biased SRAM [3]

2.4 Reliability Issues of an SRAM Cell

Read Failure: Flipping of cell state due to increase in the '0' storage node above the trip voltage of the other inverter during a read operation is regarded as read failure.

Write Failure: '1' Storage node may not be reduced below the trip point of the other inverter before WL is discharged.

Access Time Violation: The cell access time (T_{ACCESS}) is defined as the time required to produce a prespecified voltage difference ($\Delta_{MIN} \approx 0.1V_{DD}$) between two bit-lines. If due to V_{th} variation, the access time of the cell is longer than the maximum tolerable limit (T_{MAX}), an access time failure is said to have occurred [8]. Access failure is caused by the reduction in the strength of the access and the pull-down transistors. Thus, access failure limits the reduction in the size of the access transistor (required to reduce V_{READ}). An increase in the V_{th} of the access transistor and the pull-down NMOS (caused by the

process variation) can significantly increase the access time from its nominal value thereby resulting in an access failure. Thus, both intra-die and inter-die variation in process parameters increase the access failure.

Hold Failure: In the stand-by mode, the V_{dd} of the cell is reduced to reduce the leakage power consumption. As the supply voltage of the cell is lowered, the voltage at the node storing "1" also gets reduced. Moreover, for a low supply voltage leakage of the pull-down NMOS reduces the voltage at its drain node below the supply voltage applied to the cell. If it falls below the trip-point of opposite inverter, then flipping occurs and the data is lost in the hold mode. The supply voltage to be applied in the hold mode is chosen to ensure the holding of the data under nominal condition. However, variation in the process parameter can result in the device mismatch causing hold failures.

Leakage Current Estimation of MGDG MOSFET

3.1 Proposed Gate Workfunction Engineered MGDG MOSFET

Poly-depletion effect can be eliminated with use of metal gates. Midgap metal gates are easier from fabrication perspective but reduces the performance [16] hence dual metal gates are required for improved performance. An integrable Dual Metal Gate CMOS process using an ultra thin Aluminum Nitride (AlN_x) buffer layer in [17] can be used with Haffinium (Hf) as gate metal to achieve dual workfunctions for PMOS and NMOS thereby improving performance in our proposed gate work function engineered MGDG MOSFET.

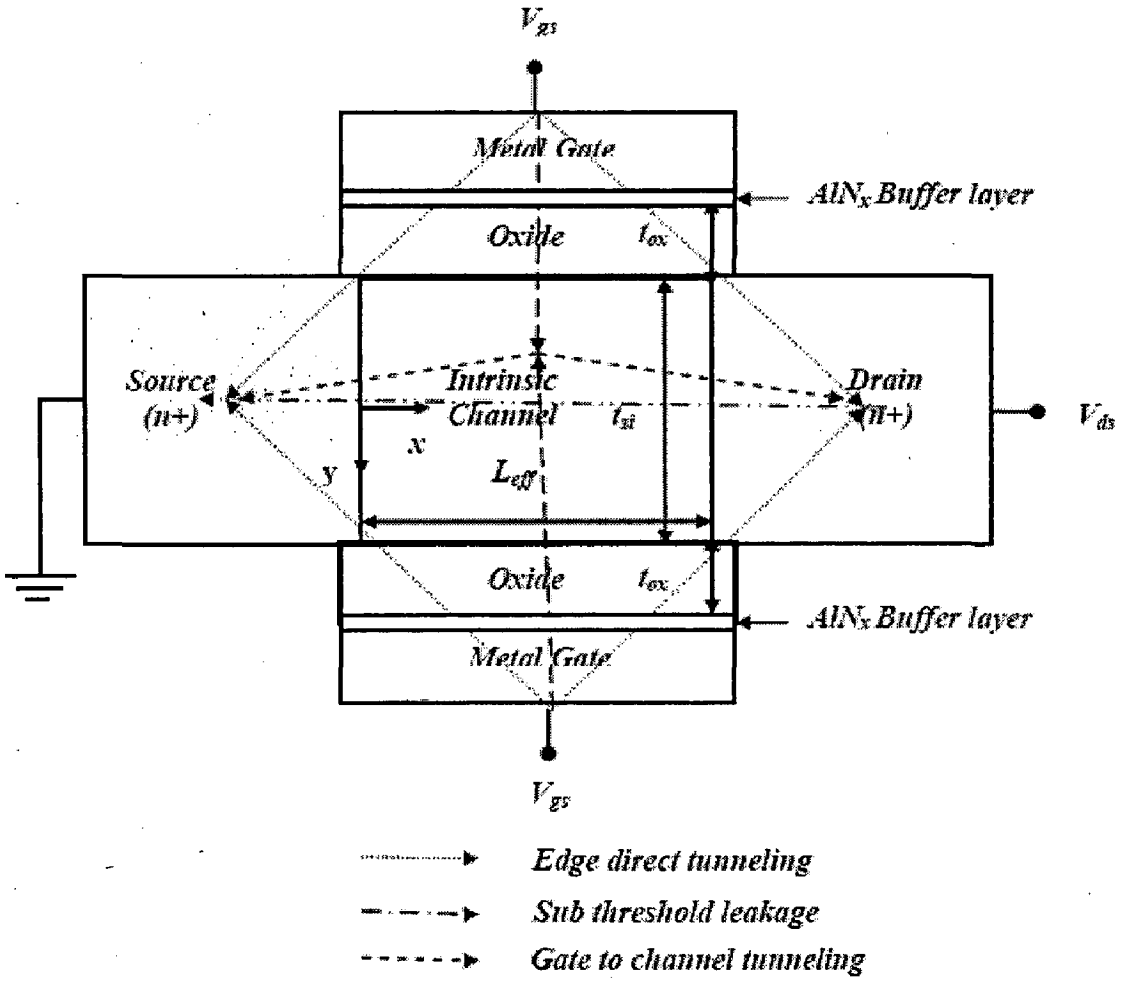


Figure 3.1 Metal Gate Double Gate MOSFET and associated leakage current components.

Using Hf/AlNx we achieve 4.4eV work function, which is ideal for MGDG-NMOSFET and use different metal with workfunction of 4.9eV which gives optimum threshold voltage for MGDG-PMOSFET so that performance of digital designs will be improved. The cross-sectional diagram of the Gate work function engineered Metal Gate Double Gate (MGDG) MOSFET with the associated leakage current components is shown in Figure 3.1.

Advantages of proposed device are,

- Metal gate Eliminates poly depletion effect and eliminates threshold voltage fluctuations.
- Subthreshold current reduces due to less DIBL of 19mV/V and reduced short channel effects.
- Absence of bulk charge and hence negligible surface electric field causes lesser gate to channel leakage.
- Intrinsic body doping eliminates random dopant fluctuation and electric field at the edges as well as interface hence Edge Direct Tunneling Current reduces.
- Stacking effect of series connected transistors in SRAM cell architecture is minimum due to lower short channel effect.

3.2 Modeling of Leakage Currents in MGDG MOSFET

The cross-sectional diagram of the Metal Gate Double Gate (MGDG) MOSFET with the associated leakage current components is shown in **figure 3.1**. Leakage current estimation requires estimation of electron energies available for tunneling and calculation of electric field in the oxide region (E_{ox}). In DG devices using ultra thin silicon body electron energies are quantized into different subbands due to structure as well as field present in the body. In our analysis we have considered first two sub bands of first valley and first sub band of second valley as they will contain most of carriers [35]. Electron energy $E_{(j,i)}$ associated with j^{th} subband of the i^{th} valley (both longitudinal and transverse) is given as [36]

$$E_{(j,i)} = \frac{j^2 (2\pi\hbar)^2}{8m_i^* t_{Si}^2} + \left[\frac{3hq\varepsilon_{ins}E_{ox}}{4\varepsilon_{Si}\sqrt{2m_i^*}} \left(j + \frac{3}{4} \right) \right]^{2/3} \tag{3.1}$$

Where q is electron charge, m_i^* is the electron effective mass in i^{th} valley ($m_1^* = 0.916m_o$, $m_2^* = 0.19m_o$), m_o is free space electron mass, ε_{ox} is the permittivity of the oxide layer, ε_{Si} is the permittivity of the silicon layer and t_{si} is silicon film thickness. The first term in equation (3.1) is due to structural quantization and second term is due to field quantization.

3.2.1 Modeling of Threshold Voltage for MGDG MOSFET

Threshold voltage of DG device considering the Short channel effects and quantum-mechanical (QM) effects is given by [36]-[40]

$$V_{th} = \frac{E_g}{2q} + \frac{1}{1+r}\left[\Phi_{Gfs} + r\Phi_{Gbs}\right] - \left(\frac{\varepsilon_{Si}t_{Si}t_{ox}V_{ds}}{\varepsilon_{ox}\alpha L_{eff}^2} + \frac{\varepsilon_{Si}t_{Si}t_{ox}E_g}{2\varepsilon_{ox}\gamma L_{eff}^2}\right) + \frac{E_g}{2q} - \frac{kT}{q}\ln\left(\frac{Q_{inv}^{QM}(E_F = 0)}{n_i t_{Si}}\right) \tag{3.2}$$

where, $r = 3t_{ox}/(3t_{ox} + t_{Si})$ is the sensitivity of threshold voltage to the back gate bias, t_{ox} is insulator layer thickness, E_g is silicon bandgap and L_{eff} is the effective channel length. We have neglected the bulk charge in metal gate devices with intrinsic body doping. For ultra thin channel thickness t_{si} due to volume inversion back gate bias can impact threshold voltage even after inversion so equation (3.2) is valid in all regions of operation [40]. Here, Φ_{Gfs} and Φ_{Gbs} are the work-function differences for the front and back gates, α and γ are the structure and doping dependent empirical factors. From equation (3.2) the threshold voltage for Hf/AlN_x is evaluated to be 0.31V.

3.2.2 Modeling of Subthreshold Current

Subthreshold current is modeled as [26]

$$I_{sub} = 2\mu_o C_g \frac{W}{L_{eff}} V_T^2 \exp\left(\frac{V_{gs} - V_{th}}{mV_T}\right) \cdot \left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{3.4}$$

where μ_o is mobility of intrinsic silicon channel, W is the gate width and V_T is thermal voltage. The parameter m is called ideality factor which is defined as the ratio of ideal subthreshold swing to that of analytically determined value of the same. Subthreshold swing S [41] [42] has been analytically calculated to be 59.5mV/dec. We have estimated DIBL using our MGDGMOSFET to be 19mV/V.

3.2.3 Effect of Channel Thickness Variation on Subthreshold Current

Threshold voltage control is limited by channel thickness control. Assuming particle in potential box model given by [43] threshold voltage variation can be modeled as,

$$\Delta V_t = -\frac{\hbar^2 \pi^2}{q m^* t_{si}^2} \frac{\Delta t_{si}}{t_{si}} \tag{3.5}$$

Assuming t_{si}=5nm and channel thickness control of 20% threshold voltage variation can be controlled to 28mV with the present device which is much lower than supply voltage under worst case variation there by guaranteeing high performance operation in nanoscale regime. As the silicon film thickness varies the inversion charge sheet move away from interface there by reducing gate leakage. Leakage currents can be kept to bare minimum if High-K dielectric is used in combination with metal gate.

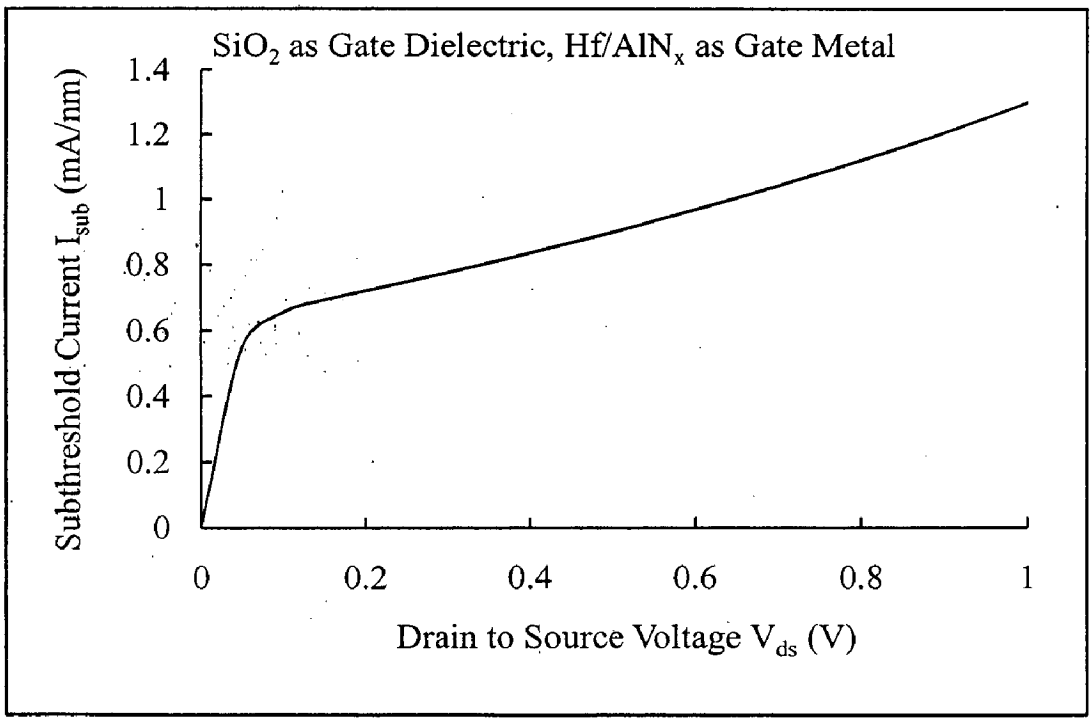


Figure 3.2 Variation of subthreshold current with drain bias

Figure 3.2 shows the variation of subthreshold current with drain bias at channel thicknesses of 5 nm for oxide thicknesses of 1 nm with SiO_2 as a gate dielectric and Hf/AlN_x as a gate metal. Subthreshold current increases with supply voltage due to DIBL effect.

3.2.4 Gate to Channel Current

For ultra thin dielectrics it has been reported in [44] that electrons no longer enter the insulator conduction band, but tunnel directly through the insulator. In state-of-the-art CMOS technologies, direct tunneling is the dominant current conduction mechanism at operating voltage for insulator thickness less than 3 nm. The different physical mechanisms for gate leakage are: conduction band electron tunneling (CBET), valence band electron tunneling (VBET), and valence band hole tunneling (VBHT). In DG devices due to strong quantum confinement, tunneling occurs from quasi-bound states (QBS) and at the interface electron eigen function is no longer nonzero in the metal gate region. Gate to channel leakage is primarily due to tunneling of electrons from inverted surface channel to gate (CBET) [23] and can be modeled as [45],

$$I_{gc} = WL_{eff} \sum_{j} \sum_{i} Q_{(j,i)} f_{(j,i)} T_{(j,i)} \tag{3.5}$$

where $Q_{(j,i)}$ is the inversion charge associated with $(j,i)^{th}$ state , $f_{(j,i)}$ is the impact frequency of electron, $T_{(j,i)}$ is the transmission probability from the $(j,i)^{th}$ state estimated using [36]. Inversion charge associated with $(j, i)^{th}$ state $Q_{(j,i)}$ is estimated as in [46]-[47].

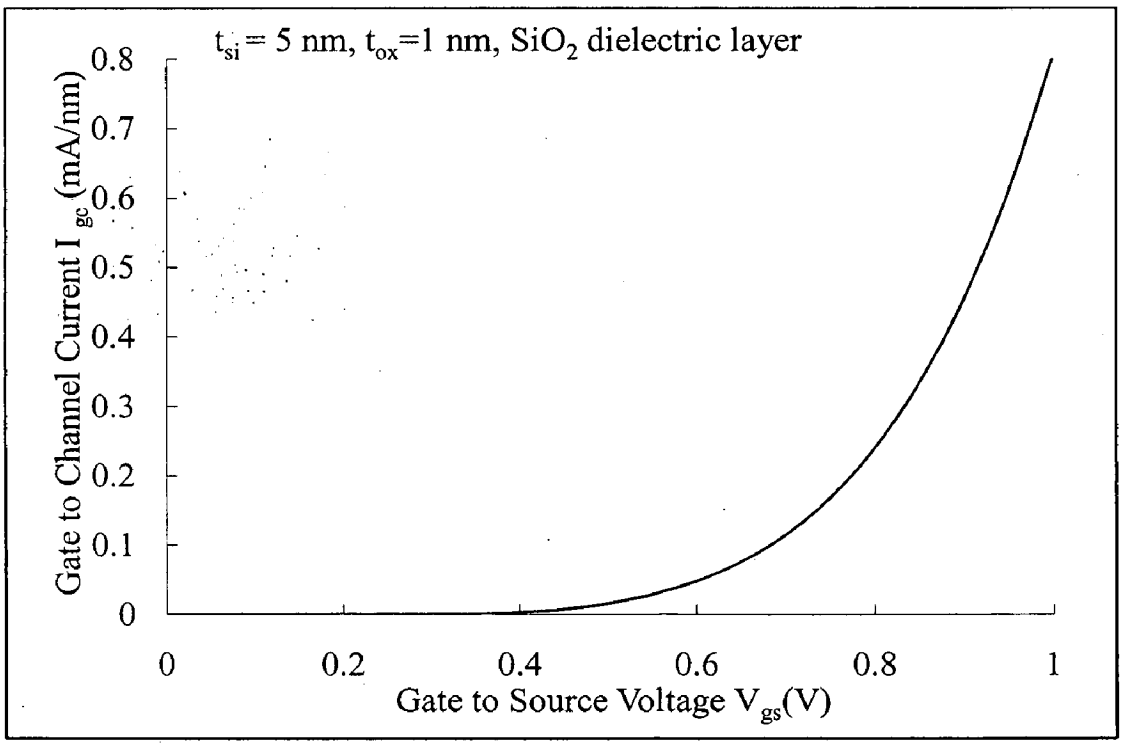


Figure 3.3 Variation of gate to channel current with gate bias.

Figure 3.3 shows the variation of gate to channel current with gate to source voltage at channel thickness of 5 nm and for oxide thicknesses of 1 nm with SiO_2 as gate dielectric and Hf/AlN_x as gate metal. As gate voltage increases due to increased tunneling probability as well as inversion charge gate to channel current increases. Figure 3.4 shows variation of gate to channel current with oxide thickness. Clearly it can be seen that leakage current variation is with in 100times its original value with in standard variation of oxide thickness from ITRS specifications. Variaiton is less basically due to logarithmic movement of inversion layer into silicon volume due to reduced oxide thickness.

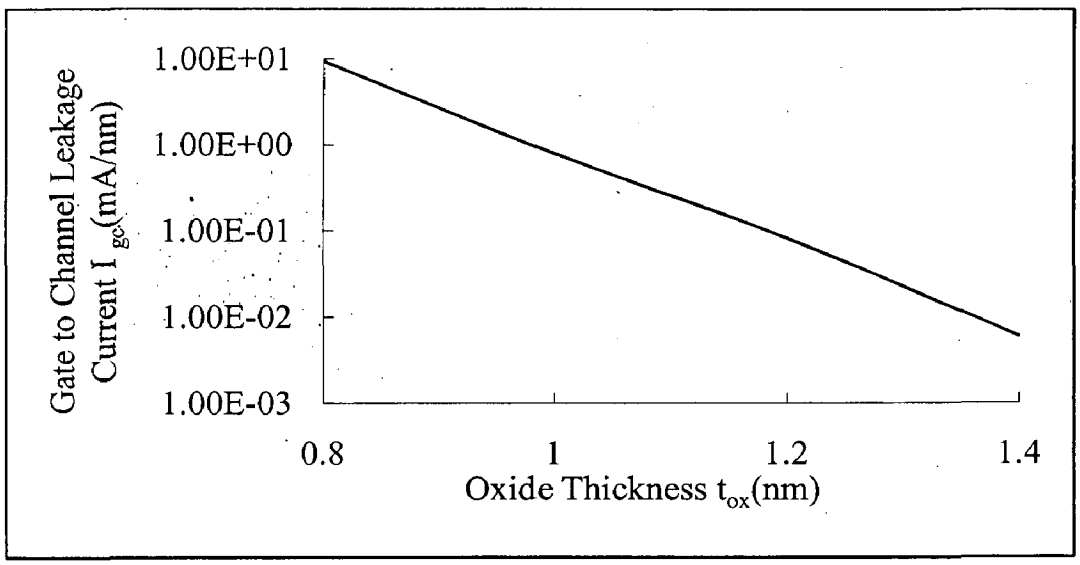


Figure 3.4 Variation of gate to channel current oxide thickness.

3.2.5 Edge Direct Tunneling Current (EDT)

Tunneling through source/drain extension region and gate occurs both in 'on' and 'off' state. In the 'on' state electron tunnels from S/D region to gate, while in 'off' state tunneling of electron occurs in opposite direction. Electric field in the oxide region E_{ox} across the 1-D gate-dielectric-drain extension structure depends on the voltage drop across drain extension (V_{DE}) given by [48],

$$V_{DE} + E_{ox} t_{ox} - (V_{DG} - V_{fb}) = 0 \tag{3.6}$$

where V_{DG} is drain gate voltage. The voltage drop across drain extension region can be evaluated as in [16]. V_{DE} can be obtained from [15]. Substituting this E_{ox} in transmission probability equation given in [45] and it can be used in evaluating EDT in 'on' state (which is basically CBET) from equation (3.5). In "off" state of MGDG structure,

electrons from the free states below the fermi level in metal constitute EDT. 'Off' state EDT density can be expressed as in [49],

$$J_{EDT} = \frac{4\pi q m^* kT}{h^3} \times \int_{E_{min}}^{E_{max}} T(E) \ln\left[\frac{1+\exp\{q(\Phi_D - V_{GD} - E_{av})/kT\}}{1+\exp\{q(\Phi_D - E_{av})/kT\}}\right] \tag{3.7}$$

$$E_{max} = \phi_m;\ E_{min} = E_C(n^+ drain);\ E_{av} = (E_{max} + E_{min})/2 \tag{3.8}$$

Where transmission probability is evaluated at average energy E_{av} and ϕ_m is gate work function. The function in integral determines 'off' state EDT density. Figure 3.5 compares variation of edge direct tunneling current with gate to drain bias. In off state due to more window available for tunneling from metal to free states we observe more leakage current than in 'on' state where EDT is primarily due to conduction band electron tunneling.

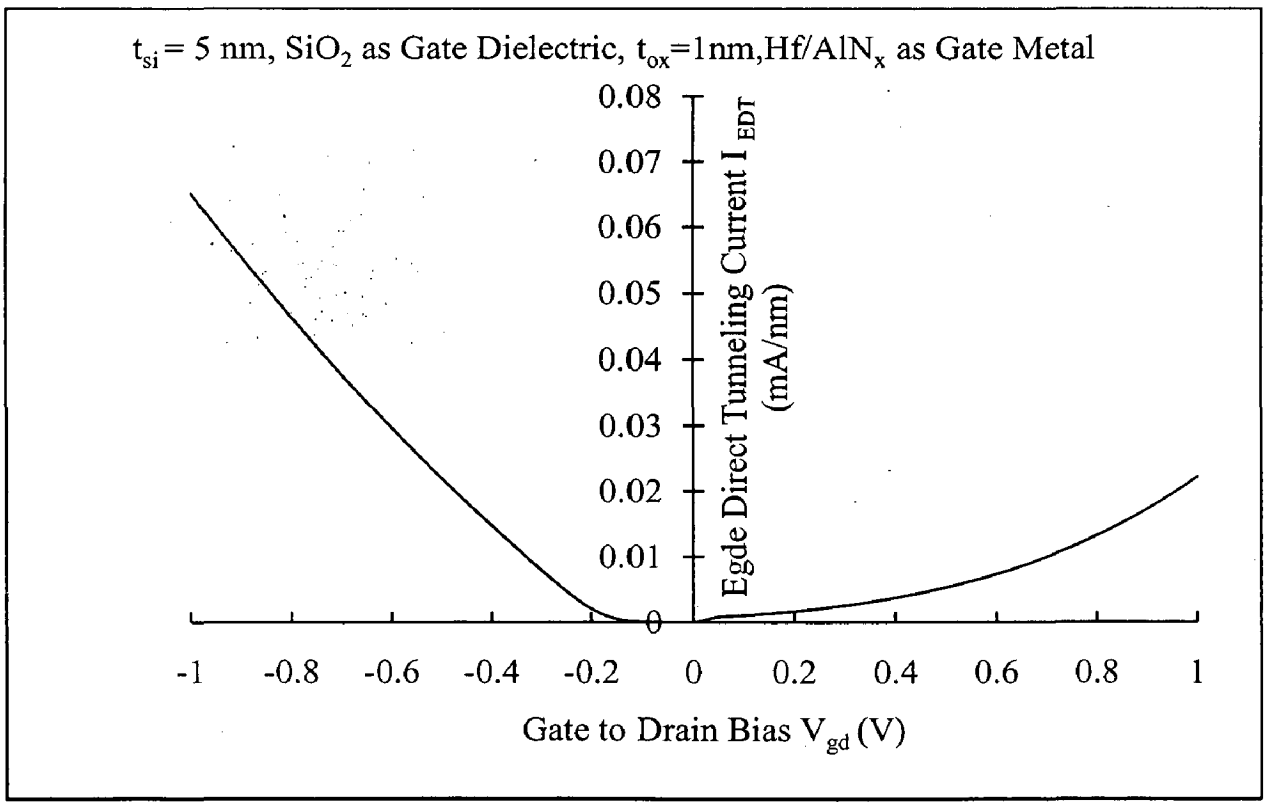


Figure 3.5 Variation of edge direct tunneling current with gate to drain bias.

3.2.6 Band-to-Band Tunneling Current (BTBT)

Band-to-band tunneling across reverse biased p-n junction occurs from p-side valence band to n-side conduction band, becomes increasingly important with continued device scaling into nanometer regime and increasing electric fields in the channel. At positive

drain bias and/or, negative bias, potential across drain-to-body region can exceed the band-gap voltage, especially at the interface causing BTBT between drain and body. I_{BTBT} is a function of the local electron-hole pair generation rate, given by [50]

$$G_{BTBT} = \frac{q^2 m^{0.5} E^2}{18\pi\hbar^2 E_g^{0.5}} \times \exp\left(-\frac{\pi m^{0.5} E_g^{1.5}}{2\hbar q E}\right) \tag{3.9}$$

Where E is local electric field and E_g is the energy band gap. The units of G_{BTBT} are electron-hole pairs/cm^3-s. Local electric filed is estimated using modeling scheme in [51]. Figure 3.6 shows the variation of band to band tunneling current with gate to source voltage for Hf/AlN$_x$ as gate metal with silicon thickness of 5 nm and for oxide thickness of 1 nm using SiO_2 as a gate dielectric on the log scale. For negative gate biases drain body junction becomes more reverse biased and hence BTBT current increases.

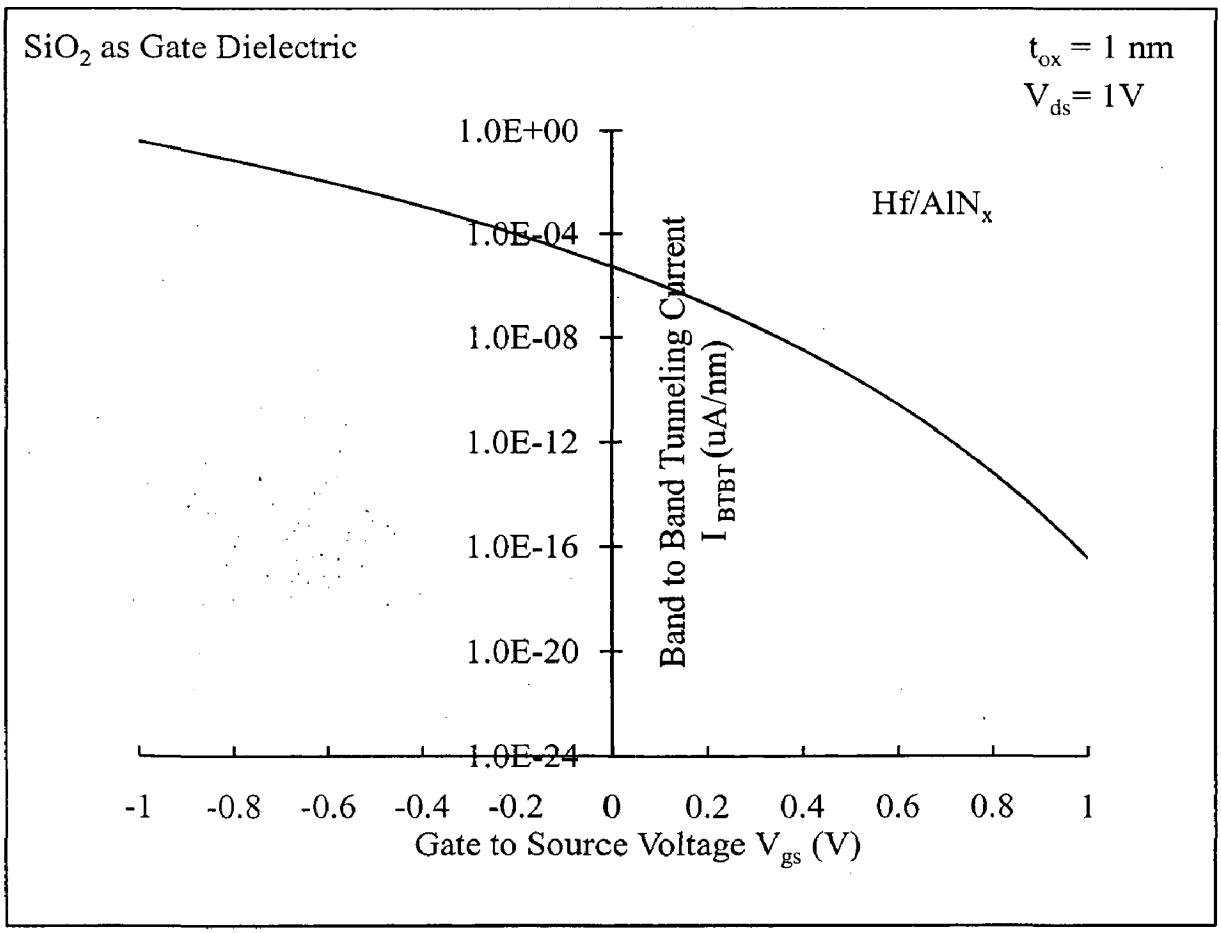


Figure 3.6 Variation of band to band tunneling current with gate to source voltage.

3.3 Stack Effect Analysis of MGDG MOSFET

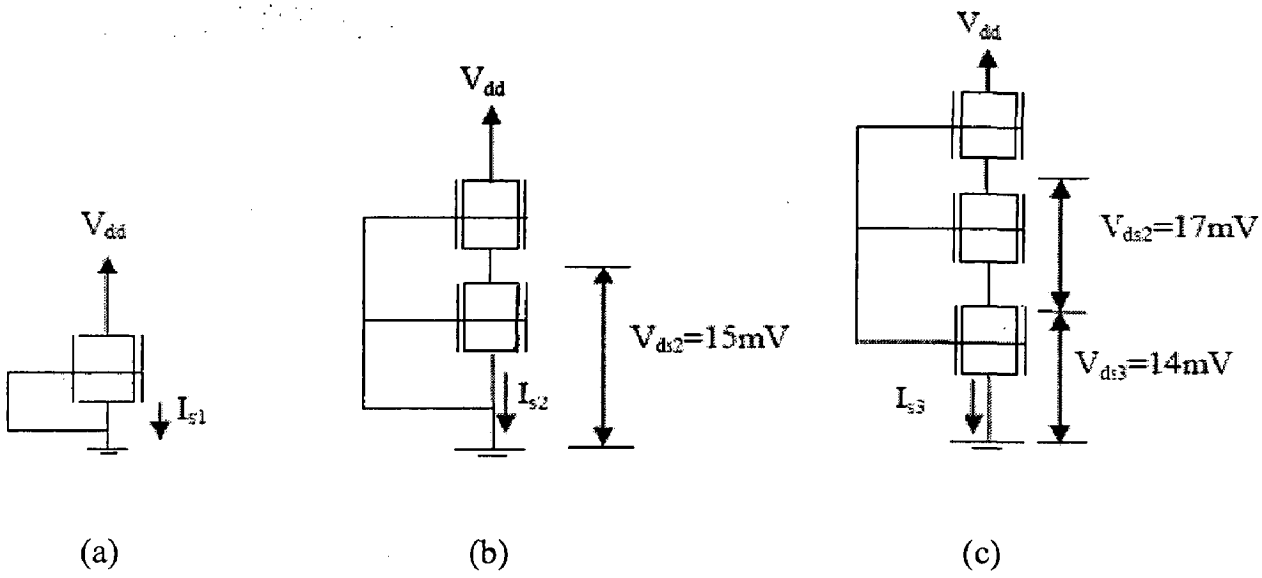


Figure 3.7 Stacked DG-NMOS transistors with V_{gs} = 0.(a) One NMOS, (b) two stacked NMOS transistors, and (c) three stacked NMOS.

Reducing DIBL is crucial for low power applications. In our MGDG MOSFET case DIBL is 19mV/V so leakage current is less and effect of stacking is not much significant. Stack effect analysis for our MGDG MOSFET is presented in Appendix A Stack effect for leakage reduction is more useful only when short channel effects are more prominent and stacking is not much beneficial in MGDG MOSFET and reduces performance.

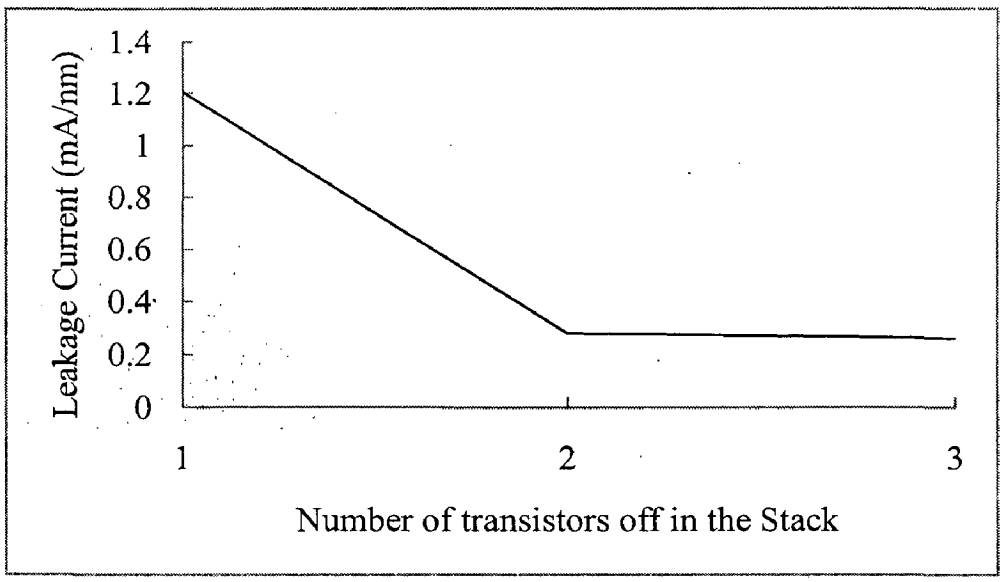


Figure 3.8 Leakage Current reduction with increasing number of off transistors.

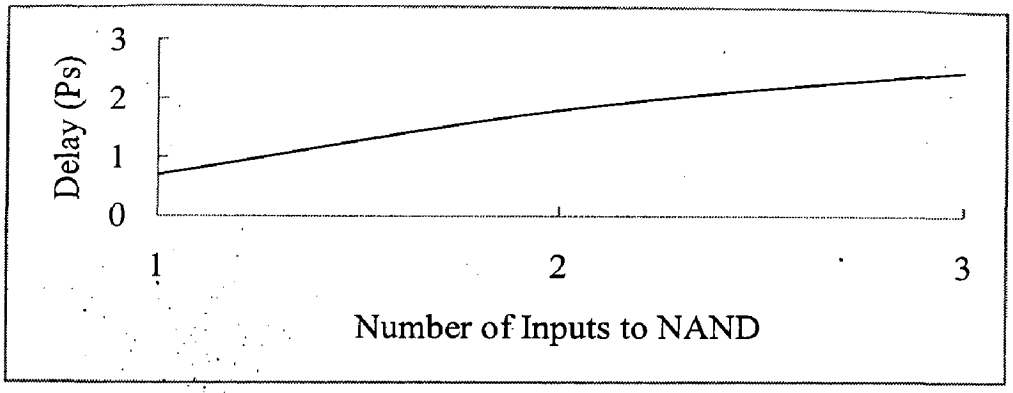


Figure 3.9 Delay increase observed usign Hspice with increasing number of inputs.

It is observed from figure that self reverse bias failed for MGDGMOSFET. Only backgate biasing is efficient scheme to reduce leakages as well as to improve performance in nanoscale circuits/Memories designed using DGMOSFET.

3.4 Effect of Back Gate Bias on Leakage Currents

Effect of back gate bias on front channel electrical properties is modeled through variation in front channel threshold voltage V_{thf} [44], [45], [46] as given by,

$$V_{thf} = V_{thfo} - \left(rV_{gbx}\right)$$

$$V_{gbx} = \begin{cases} V_{gb} & V_{gb} < V_{thb}; \\ V_{thb} & V_{gb} > V_{thb}; \end{cases} \tag{3.10}$$

where V_{thfo} the front gate threshold voltage at zero gate bias, V_{thb} is the back gate threshold voltage and V_{gb} is back gate bias. All the leakage currents from both front and back gate have been calculated with the incorporation of equation (3.10) and it has been found that at a backgate bias of -0.4V all the leakage currents are minimum and at backgate bias of 0.3V performance of MGDG will be improved due to reduced threshold voltage. Subthreshold current variation with the incorporation of backgate bias is as shown in figure 3.10. Figure 3.10 shows the variation of subthreshold current with back gate bias (V_{gs2}) using Hf/AlN$_x$ as gate metal, at channel thickness of 5 nm and oxide thickness of 1 nm with SiO_2 as gate dielectric on log scale. It can be observed that when back gate is in depletion condition ($V_{gb} < V_{thb}$) subthreshold currents starts to decrease with decreasing back gate voltage due to reduced level of inversion at the front interface.

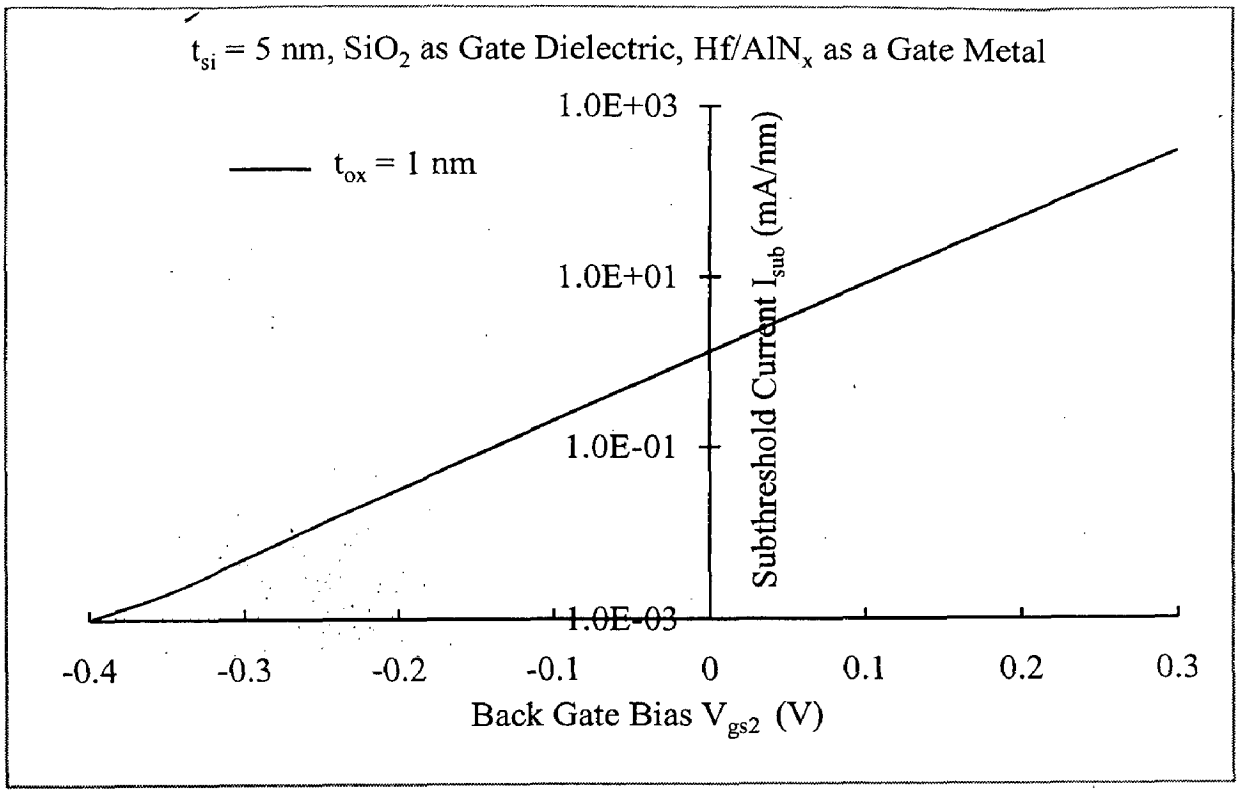


Figure 3.10 Variation of subthreshold current with Back Gate Bias.

Beyond certain negative back gate bias gate-gate coupling effect will be eliminated. In our modeling scheme we are restricting V_{gs2} to - 0.4V in negative direction by considering power dissipation characteristics. There is no exact value of V_{gs2} in negative direction reported in literature beyond which threshold voltage is insensitive to it, since for ultrathin films the possibility of accumulating the back interface is very less and according to Zhang and Roy [44], [45] front gate threshold voltage depends on back gate bias as long as back gate is depleted, where as in positive direction it is limited by the threshold voltage of back gate. Here only BTBT current increases slightly with negative back gate bias except that all leakage currents shows increasing trend with increasing back gate bias from -0.4V to 0.4Vsimilar to that in figure 3.10. Thus for transistors in off state leakage can be reduced to a larger extent by applying suitable negative bias (about -0.4V) to the back gate of these transistors during store '0' operation. The main leakage currents in on state N-transistor are 'on' state EDT and gate to channel leakage. As EDT is much small compared to Gate to Channel current (I_{gc}) our main objective is to reduce I_{gc}. At a back gate bias of 0.3V threshold voltage of the device gets reduced, so we will observe improved performance for transistors in 'on' state with a back gate bias of 0.3V at the cost of increased leakage by approximately three times.

Leakages and Nanometer Cache Design Using MGDG MOSFET

4.1 Leakage Currents Present in MGDG SRAM

Leakage currents present in typical SRAM cell designed using MGDG MOSFET during idle mode are shown in Figure 4.1.

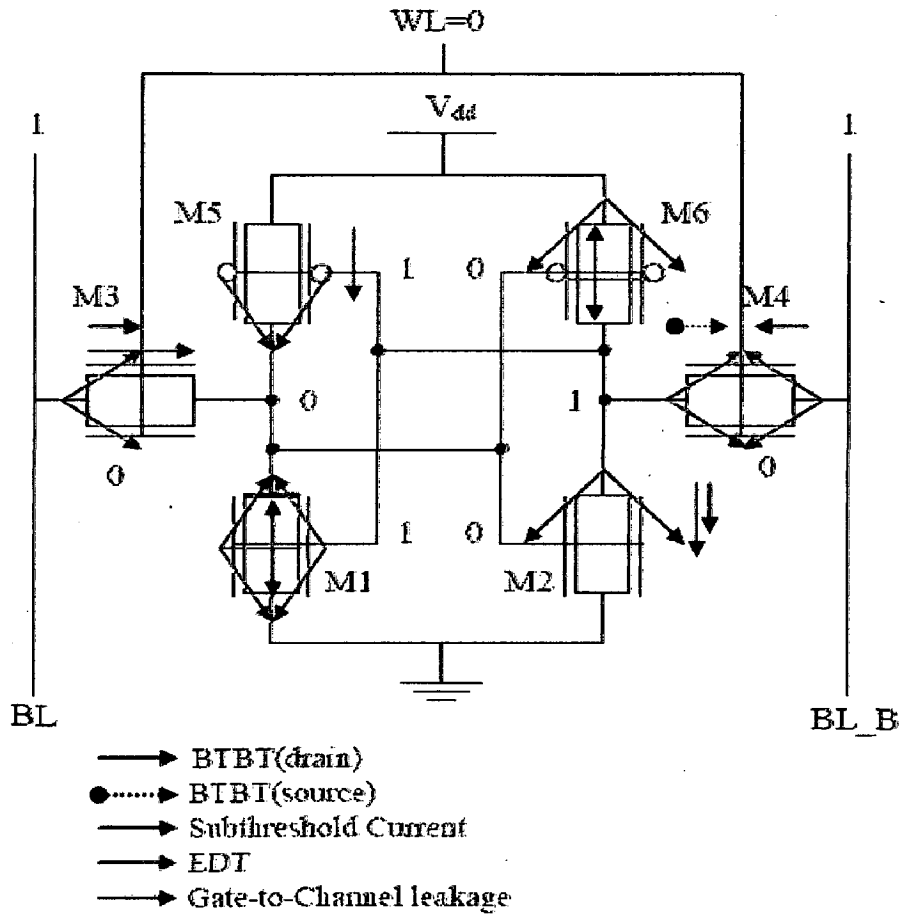
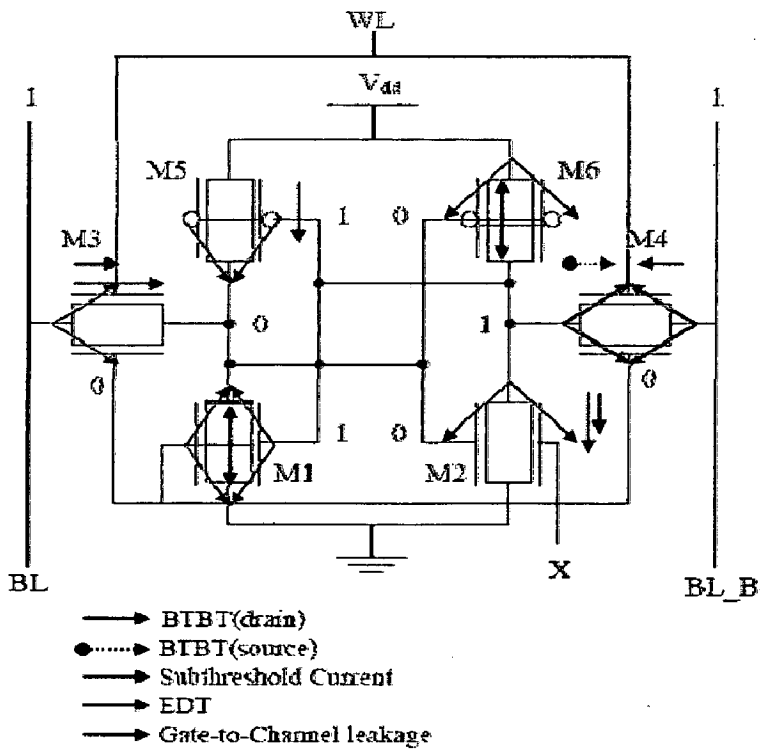


Figure 4.1 Leakage components in MGDG SRAM cell during idle mode.

Where BL is bitline, BL_B is complementary bitline and WL indicates wordline activation for accessing the cell. In idle mode when the wordline is not asserted we observe subthereshold leakage in access FET on '0' side and driver FET on '1' side. Mostly we observe gate leakage at all other nodes since terminals are at different potentials. It is clearly observed that when the nodes are at different potentials we observe either Gate-to-Channel current or EDT. If gate potential is zero based on drain source potential Subthreshold Current flows.

4.2 Proposed Backgate Biasing Scheme using MGDG MOSFET

Dual threshold voltage schemes utilize the timing slack of noncritical paths to reduce leakage power by using high threshold voltage devices in noncritical path and low threshold voltage devices in critical path. Making tradeoff between leakage power and performance leads to a significant reduction in the leakage power while sacrificing only some or none of circuit performance. Such a tradeoff is made in Dual Threshold designs [6]. In our design we typically use forward biased back gate devices in critical path during active operation to improve performance and we switch to negative back gate bias during standby mode to reduce leakage. From Chapter 3 it has been found that at a back gate bias of -0.4V all the leakage currents are minimum and at backgate bias of 0.3V performance of MGDG will be improved due to reduced threshold voltage. So, except BTBT current all leakage currents will increase monotonically with increasing back gate voltage from -0.4V to 0.3V.Back gate biasing introduces transition time as well as energy overhead. Each subarray has Subarray select signal (SUBSL) which is generated by row decoder. X line is body biasing signal for subarray and can be routed using an upper layer metal.



Where X is back gate biasing signal generated from body bias drivers.

Figure 4.2 Proposed leakage reduction scheme using MGDG MOSFET.

In SRAM NMOS access transistor and pull down transistor are critical for read, write operations. So, they are fed with forward bias of 0.3V in 'on' state to get improved performance and with -0.4V back gate bias in 'off' state for reduced leakage. Schematic of the proposed latency minimized cache subarray is shown in figure 4.2.

4.3 Estimation of Semiconductor Capacitance and transition time

But transition time and energy overhead is introduced by back gate bias which in turn depends on parasitic body capacitances and semiconductor capacitance.

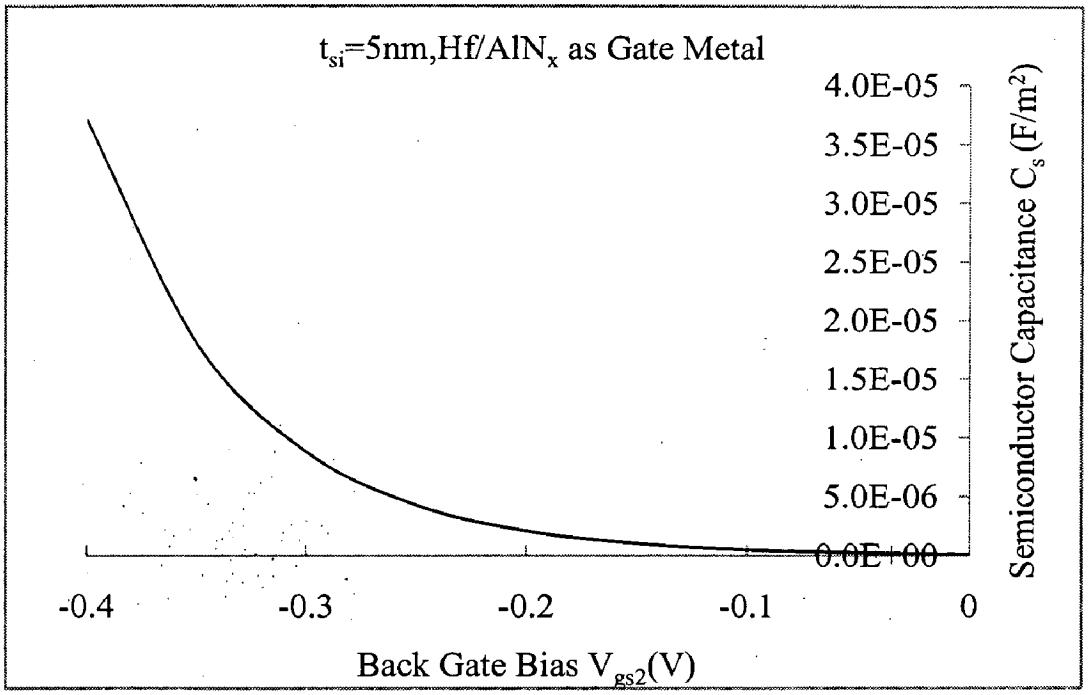


Figure 4.3 Semiconductor capacitance variation with back gate bias

Figure 4.3 shows the semiconductor film capacitance variation with back gate bias from - 0.4V to 0V with unbiased front gate. Assuming film resistance of .1Ω-m and with given device dimensions and FBB=0.3V and RBB= -0.4V latency time can be calculated to be 0.69RC=1.021ps. It is clearly observed that transition overhead is very less and facilitating easier design of decoder circuitry without compromising much on performance with application of leakage reduction technique. With this configuration back gate selection signal need not be generated since back gate activation time is very less with present configuration using MGDG MOSFET.

Since MGDG uses fully depleted silicon film, substrate parasitic capacitances are eliminated. Drain to gate capacitance is less in Double gate devices due to increased control of gate on channel. In body biased cache subarray architectures each subarray

has a subarray select signal (SUBSL) which is generated by the row decoder circuit [9]. SUBSL selects the subarray ahead of time which is needed for transition from forward back gate bias (FBB) to reverse back gate bias (RBB). The 0.3V FBB and -0.4V for RBB can be generated by a high-efficiency DC–DC switched capacitor converter. For facilitating easier design of switched capacitor converter one can prefer -0.3V and 0.3V as RBB and FBB respectively. Switching between FBB and RBB requires additional transition delay and energy overhead. Four NMOS MGDG's in each SRAM cell yield four gate–body capacitances to charge and discharge in every body transition event. This introduces transition latency and energy overhead. But, the transition overhead is minimum in MGDG devices due to the use of intrinsic body and reduced parasitic substrate capacitance. Parameter variations causes congestion of design margins [10]. MGDG MOSFET is less sensitive to parameter variations and parameter variations reduce considerably if negative backgate bias is applied hence SRAM cell designed by it is more robust.

Chapter 5

Small Signal Capacitance and Glitch Voltage Estimation

5.1 Causes of Potential Rise at Output

In circuits operating at nanoscale regime potential rise at output node during signal transitioning events creates timing, noise and glitch related problems. Glitches at output are result of gate-drain capacitance of MOSFET. So, to perform early power and timing estimates, one needs an efficient method to estimate the small signal capacitances of the selected device structure. Leakage currents also determines the potential rise or fall at critical nodes, so leakage current estimation using interconnection effect and solution of nodal current equations at different nodes of circuit gives better insight into the robustness of the circuit. We have obtained independent small signal capacitances and used them in the glitch voltage estimation of circuits designed with the proposed device. A very good agreement is reached between the DESSIS-ISE Simulations presented in [28] and our analytical modeling. We have evaluated potential rise at output node during signal transitioning events for inverter designed with our MGDG MOSFET both analytically and through **HSPICE Simulations**. Due to reduced gate-drain capacitance the steady state charge injected into the body is less and hence noise power will be reduced.

We did leakage current estimation of SRAM cell using interconnection effect and estimated the potential rise/fall at the '0' and '1' storing nodes. Further the read/write failure probability is reduced since during word line assertion less potential rise is observed due to the reduced gate-drain capacitance.

5.2 Modeling of Small Signal Capacitances of MGDG MOSFET

Explicit charge based expressions are required for evaluating gate-drain capacitances. We have considered explicit charge based expression for mobile charge sheet density/unit area [28],

$$Q = 2C_{ox}\left(-\frac{2C_{ox}V_T^{\,2}}{Q_o}+\sqrt{\left(\frac{2C_{ox}V_T^{\,2}}{Q_o}\right)^2+4V_T^{\,2}\log^2\left[1+\exp\left(\frac{V_{gs}-V_{th}-V}{2V_T}\right)\right]}+\frac{E_{11}}{q}\right) \qquad (5.1)$$

where C_{ox} is the oxide capacitance/unit area, q is electron charge, $V_T = kT/q$ is thermal voltage, $Q_o = 4V_T C_{si}$, V_{gs} is gate bias, V_{th} is threshold voltage modeling as in section A , V is electron quasi-Fermi potential which depends on V_{ds} and E_{11} is the energy of first subband of first valley in which most of the carriers are populated and it models the quantum correction for mobile charge density both due to structural and field quantization. The terminal charges and associated capacitances are essential for AC and transient analysis of MGDG MOSFET. In above the source and drain charge densities can be obtained by substituting 0 and V_{ds} respectively in equation (5.1) in place of electron quasi-Fermi potential. The drain and source charges at non zero V_{ds} can be obtained from [28]. Charge conservation requires that all the capacitances be computed in terms of terminal charges given by,

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \tag{5.2}$$

Where i and j are terminals of MGDG-MOSFET. C_{gd} can be evaluated from equation (5.1) and (5.2) since it is of most interest in circuit applications and it is the independent capacitance from which others can be evaluated. The expression for C_{gd} is given by,

$$\frac{C_{gd}}{2WLC_{ox}} = \frac{2V_T \log\left[1+\exp\left(\frac{V_{gs}-V_{th}-V}{2V_T}\right)\right] * \exp\left(\frac{V_{gs}-V_{th}-V}{2V_T}\right)}{\sqrt{\left(\frac{2C_{ox}V_T^2}{Q_o}\right)^2 + 4V_T^2 \log^2\left[1+\exp\left(\frac{V_{gs}-V_{th}-V}{2V_T}\right)\right] * \left[1+\exp\left(\frac{V_{gs}-V_{th}-V}{2V_T}\right)\right]}} \tag{5.3}$$

while plotting the graphs we normalize all the capacitances with the factor $2WLC_{ox}$

Figure 5.1 compares the variation of normalized gate-to-drain capacitance with drain to source voltage for our case of MGDG-MOSFET and that of DESSIS simulations from [28] with L=1um, W=1um, t_{ins}=2nm, t_{si}=20nm. As can be observed from the figure both results agree at very low values of drain to source voltage but as drain to source voltage increases we observe a very small decrement of gate-to drain capacitance in our case due to more rigid gate control of channel in our case and also we will observe performance improvement.

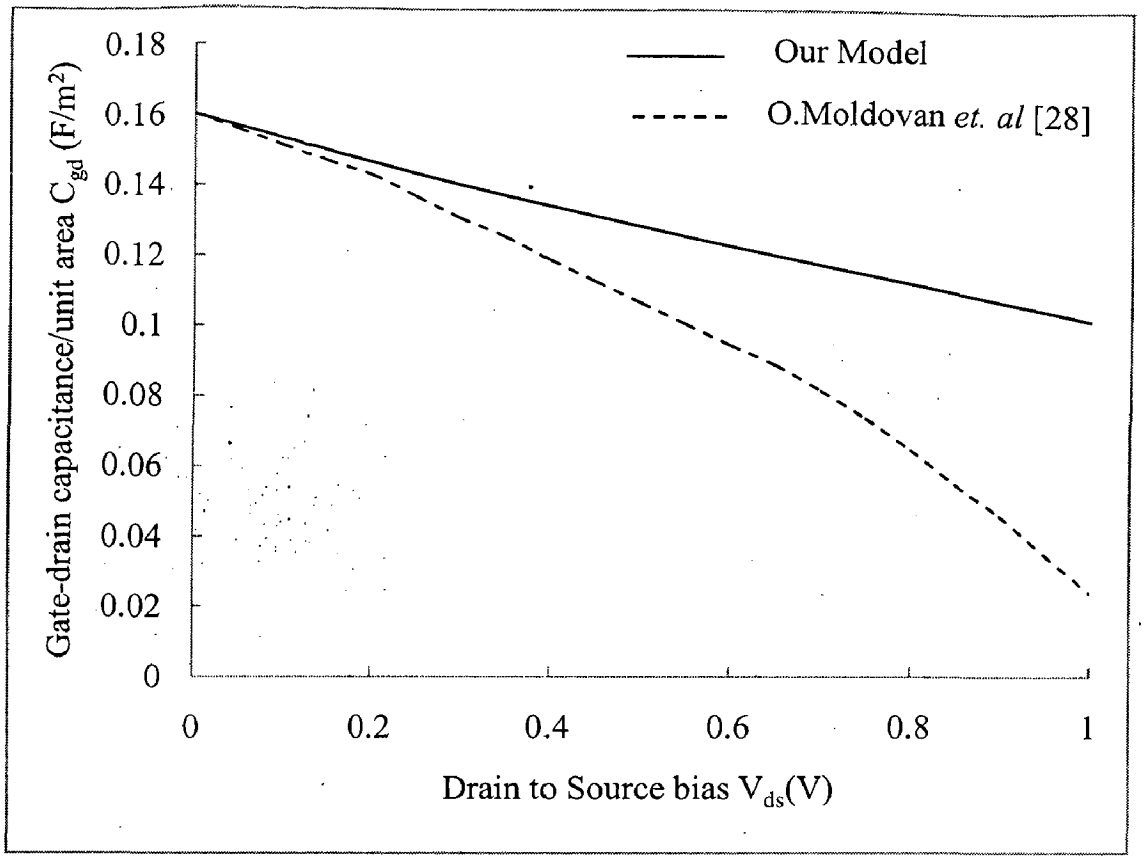


Figure 5.1 Gate-Drain capacitance variation with drain potential from analytical modeling of MGDG –MOSFET vs DESIS-ISE simulation from [28].

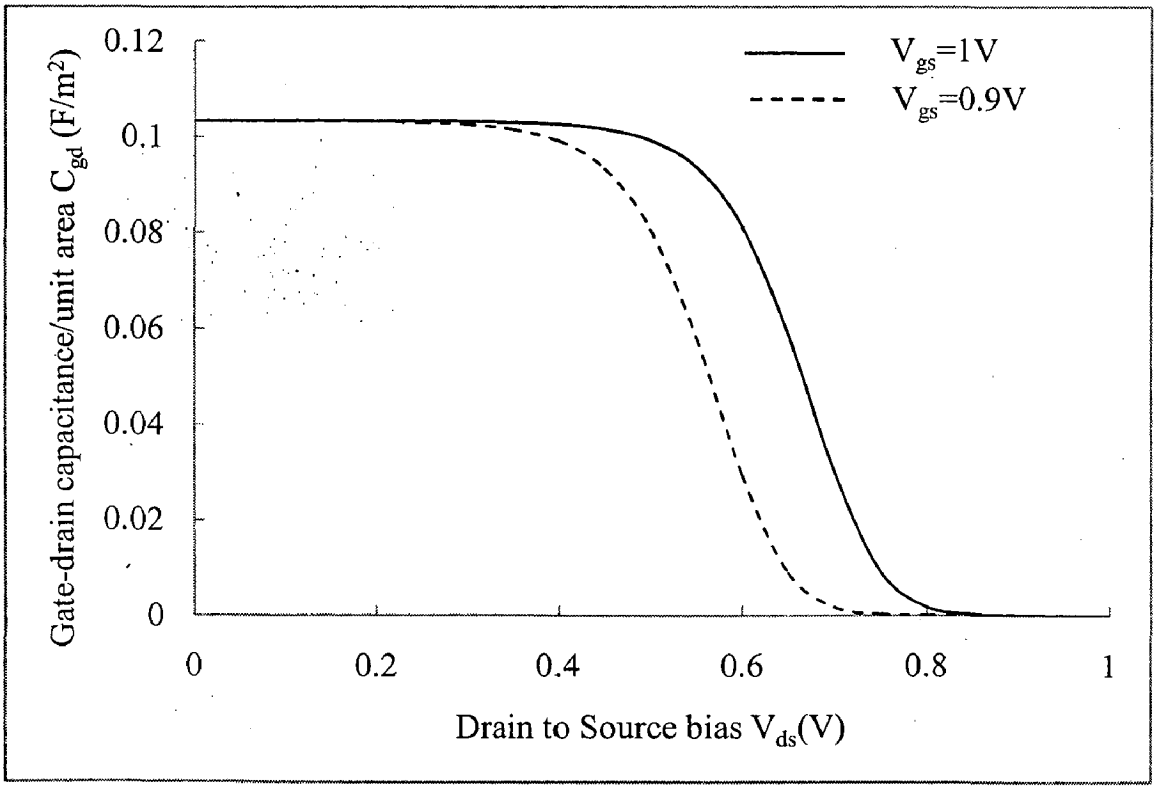


Figure 5.2 Normalized Gate-Drain capacitance variation with drain potential from analytical modeling of MGDG-MOSFET.

Figure 5.2 shows the variation of normalized gate to drain capacitance with drain to source voltage for two values of gate voltages 1V and 0.9V using L_{eff}=20nm, t_{ox}=1nm, t_{si}=5nm, W=30nm with Hf/AlN_x as gate metal. As can be observed from the figure at lower values of gate potentials the fall in gate drain capacitance is more drastic due to reduced inversion charge. The normalized gate to drain capacitance at V_{ds}=0V for conventional bulk MOSFET with same device parameters as MGDG MOSFET is found to be 0.61, which shows the superiority of MGDG MOSFET during signal transitioning events and improves reliability of Memory circuits designed with it. Gate to drain capacitance, gate to source capacitance and drain to gate capacitance shows the same variation with respect to gate voltage for V_{ds}=0V. For non zero V_{ds} they show little deviation as shown in [28].

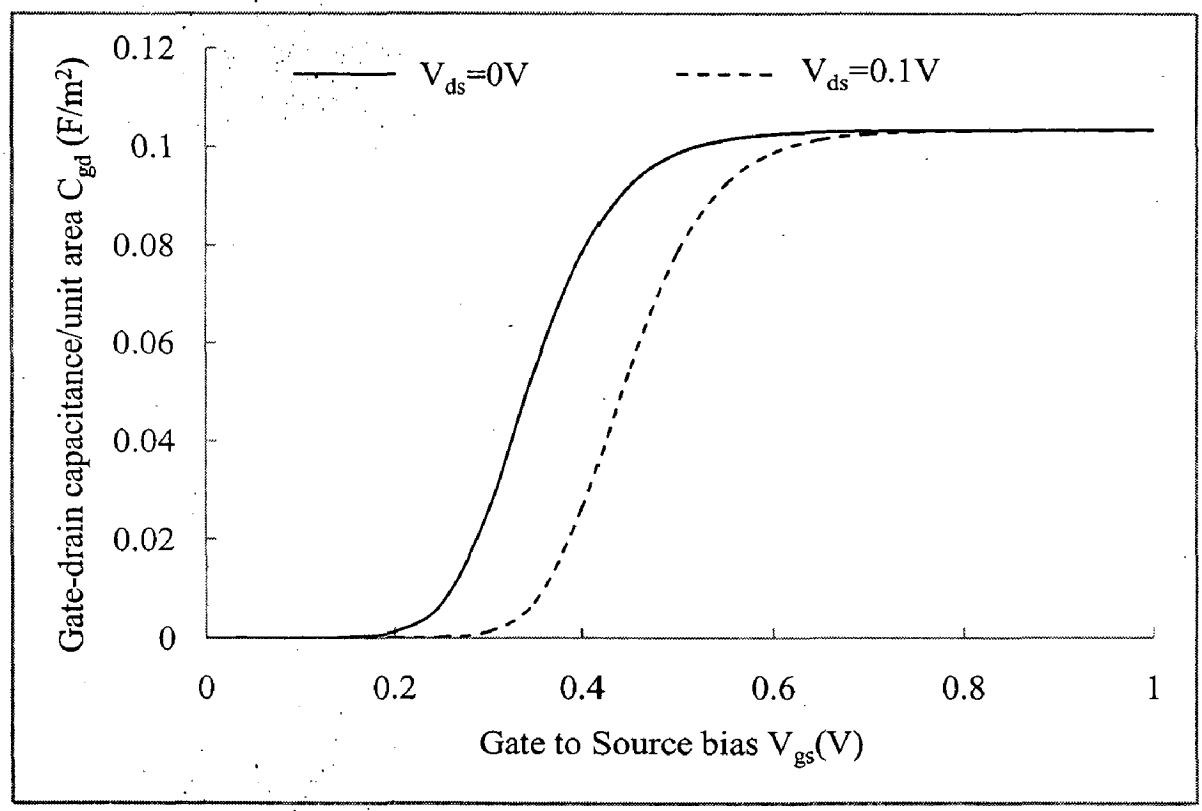


Figure 5.3 Normalized Gate-Drain capacitance variation with gate potential from analytical modeling of MGDG -MOSFET.

Figure 5.3 shows the variation of normalized gate to drain capacitance with gate to source voltage for two values of gate voltages 1V and 0.9V using L_{eff}=20nm, t_{ox}=1nm, t_{si}=5nm, W=30nm with Hf/AlN_x as gate metal. After inversion charge build up gate to drain capacitance increases with gate voltage and attains saturation after threshold condition is reached. Increased drain voltage delays the attainment of saturation point since it delays inversion charge build up.

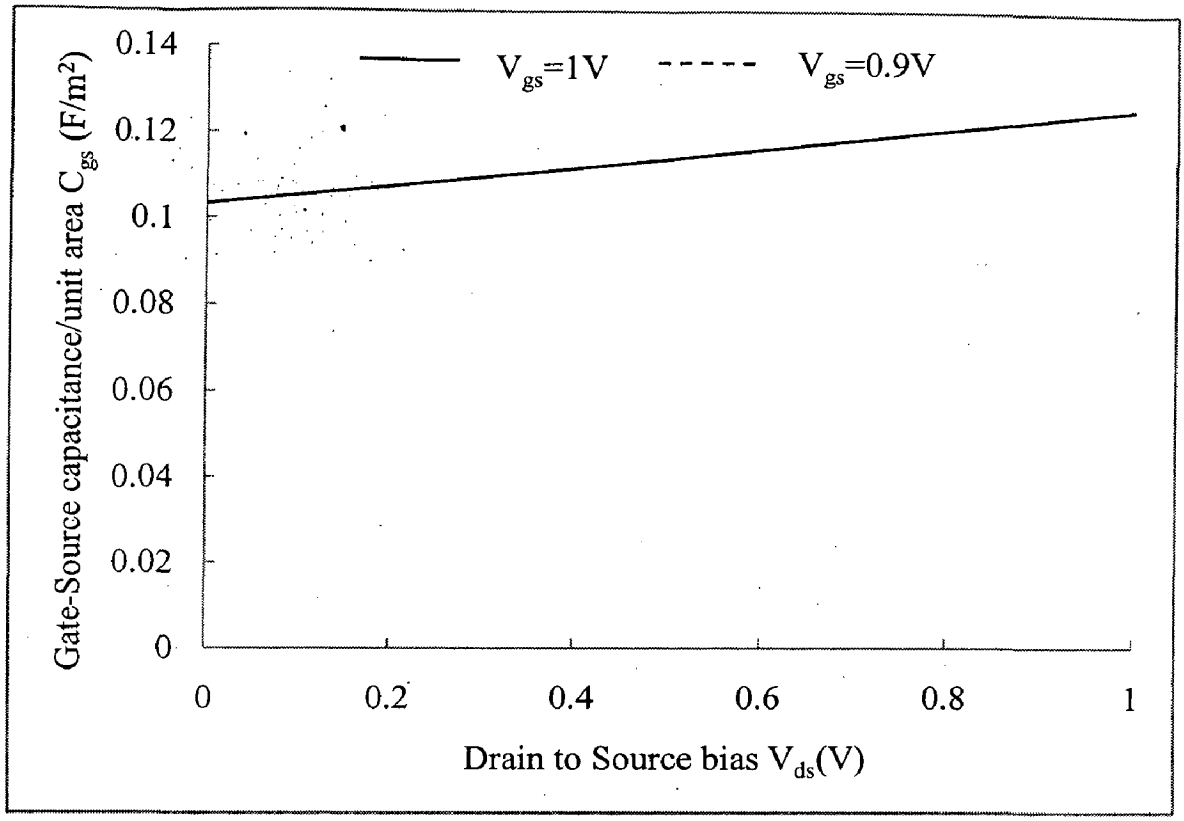


Figure 5.4 Gate-Source capacitance variation with drain potential from analytical modeling of MGDG –MOSFET

Figure 5.4 shows the variation of normalized gate to source capacitance with drain to source voltage for two values of gate voltages 1V and 0.9V using L_{eff}=20nm, t_{ox}=1nm, t_{si}=5nm, W=30nm with Hf/AlN_x as gate material. Symmetry can be observed in both C_{gs} and C_{gd} since both of them attains same values at V_{ds}=0V and after that the deviation starts due to partitioning of inversion charge into source and drain regions. From the figure it can be observed that as drain to source voltage increases gate to source capacitance increases due to slight increase of inversion charge and the variation follows that of given in [28] but with reduced normalized values since we are operating with lesser supply voltages. With reduced gate potentials it follows the same variation since inversion charge is increasing in contrast to decrease in case of gate-drain capacitance.

5.3 Estimation of Voltage Rise during Signal Transitioning Events

Typical configuration in most of the digital devices is Pullup network consisting of PMOS and Pull down network consisting of NMOS. Since the structure is symmetrical potential rise or fall during any particular transition is same [27]. Typically we can model the structure to be as in Figure 5.5.

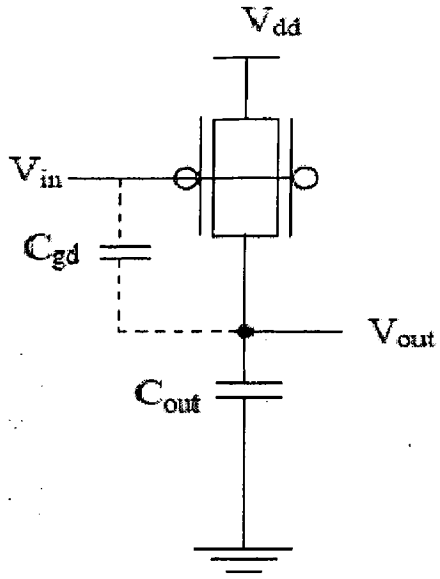


Figure 5.5 Glitch Model of General CMOS Logic Circuits.

Applying charge conservation at output node during 0 → 1 transition at input node,

$$V_{dd}C_{gd} + V_{dd}C_{out} = V_x C_{out} + (V_x - V_{dd})C_{gd} \tag{5.4}$$

where V_x is the potential at output during the transition at the input, C_{out} is the capacitance at the output node, V_{dd} is the supply voltage 1V in our case and C_{gd} is the gate-drain capacitance of DG MOSFET under consideration.

By solving above equation (5.4) we obtain,

$$V_x = \frac{V_{dd}(C_{out} + 2C_{gd})}{(C_{out} + C_{gd})} \tag{5.5}$$

A maximum of 0.7 mV potential rise is observed using fanout=10 in an inverter circuit designed with MGDG MOSFET's. In DG based SRAM's a maximum of 7mV rise is observed which will not affect the failure probabilities much. Drain to gate capacitance is less in Double gate devices due to increased control of gate on channel. The reduced gate-drain capacitance produces less glitch currents during switching the access transistors from off state to on state in SRAM cell and this reduces the problem of false triggering in feedback inverter and improves the read and writes margins there by facilitating more design margin for circuit designers.

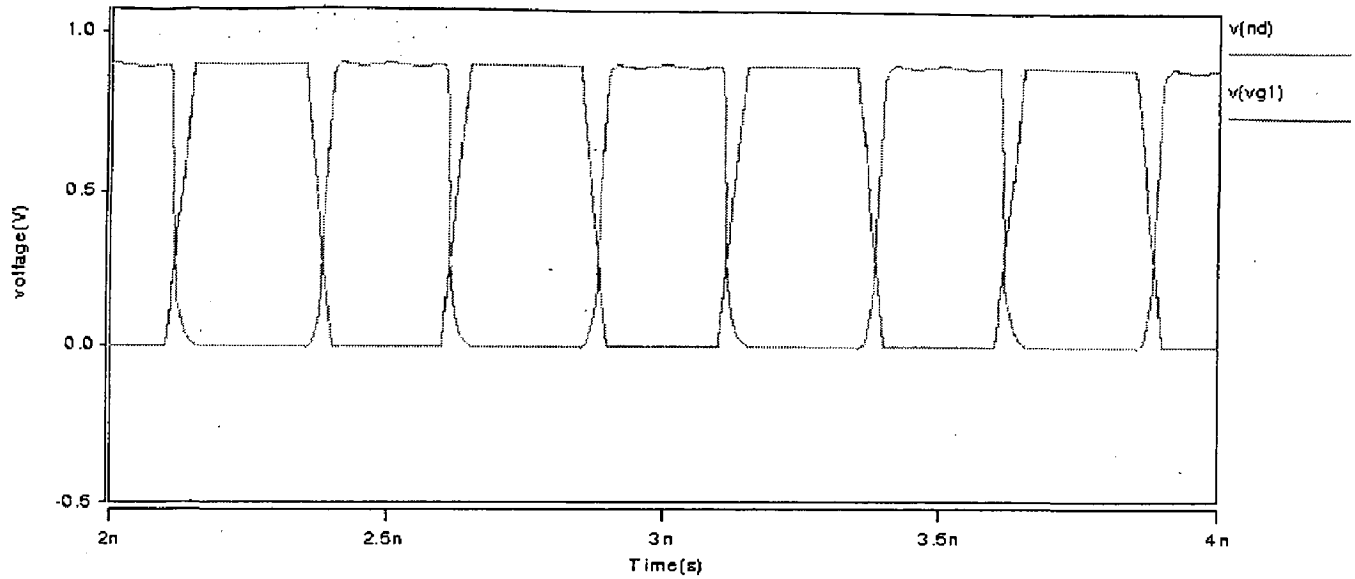


Figure 5.6 Inverter Transient simulation of MGDG inverter using HSPICE

Figure 5.6 shows the transient simulation of voltage transfer characteristics of inverter using BSIM SOI model cards for both front and backgates. V(nd) is output of the inverter and V(vg1) is common gate input of inverter designed using MGDG MOSFET. A delay of 0.8ps is observed for MGDG inverter and the voltage rise observed at the output validates with that of theoretical simulations as shown in Figure 5.7.

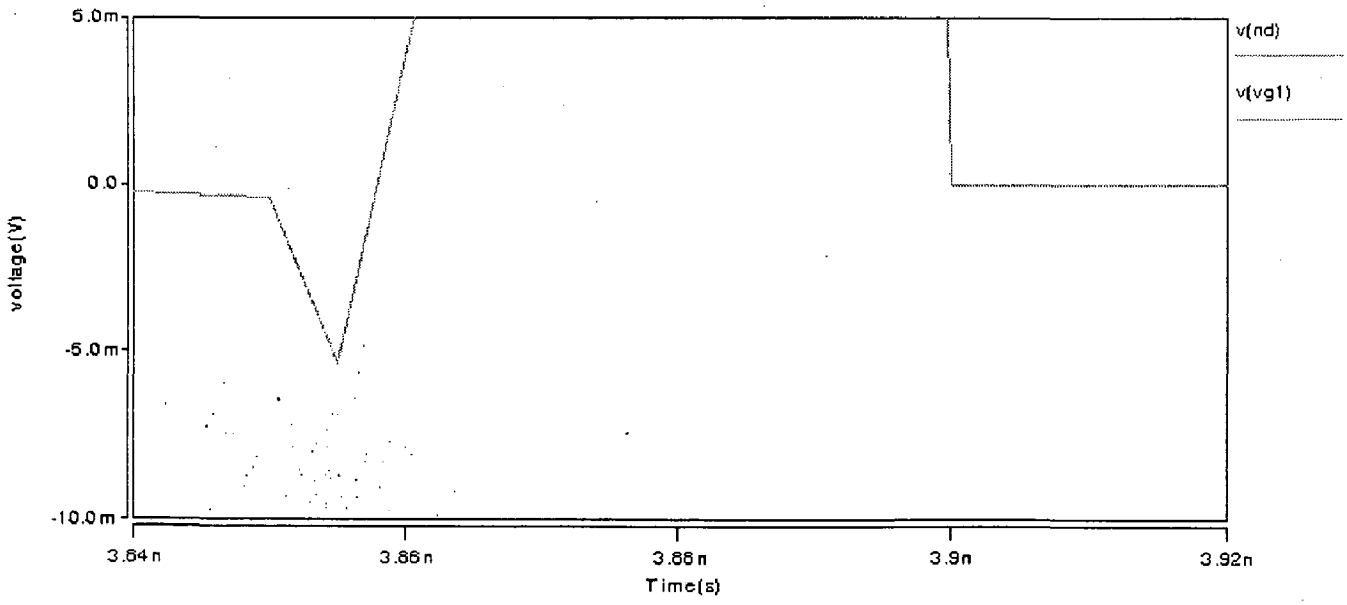


Figure 5.7 Validation of Potential fall using our model and HSPICE simulations.

Figure 5.7 Validation of Potential fall using our model and HSPICE simulations. The reduced gate to drain capacitance produces less glitch currents while switching the

access transistors from off state to on state, this reduces the problem of false triggering in feedback inverter used in SRAM design and improves the read noise margin.

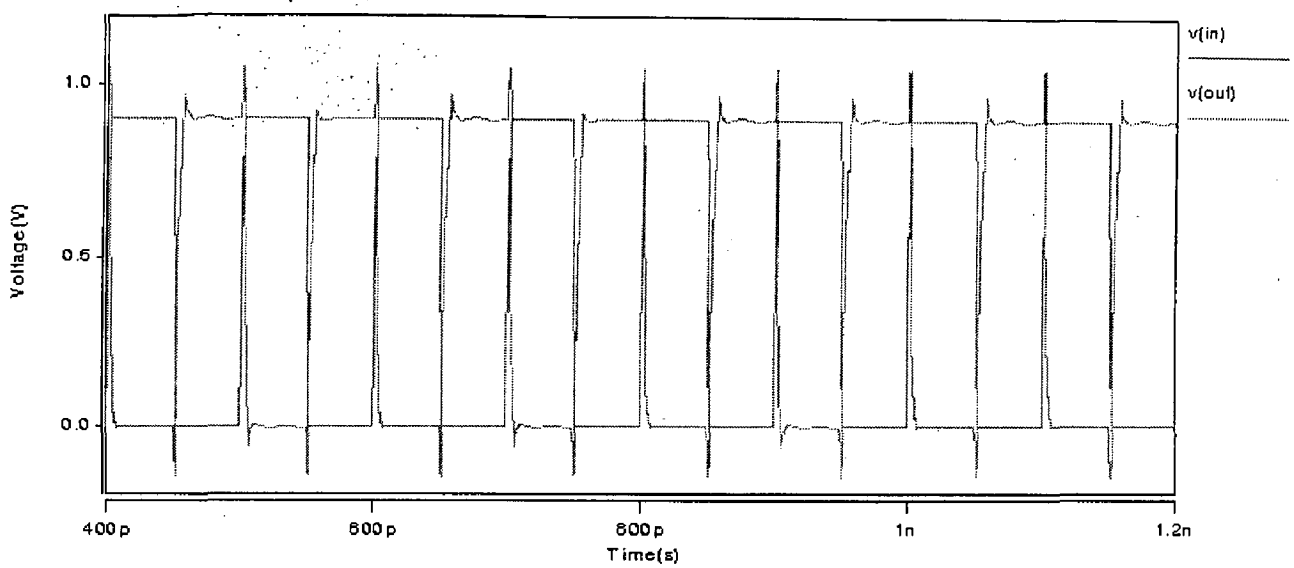


Figure 5.8 Inverter Transient simulation of Bulk CMOS inverter using HSPICE

Figure 5.8 shows the transient simulation of inverter designed using bulk MOSFET with similar transistor sizes at 32nm node using BPTM model cards. A delay of 2.1ps is observed showing the inferior performance of double gate structures which are for extending the scaling. But in subthreshold regime DG MOSFET performs well due to its near ideal subthreshold slope.

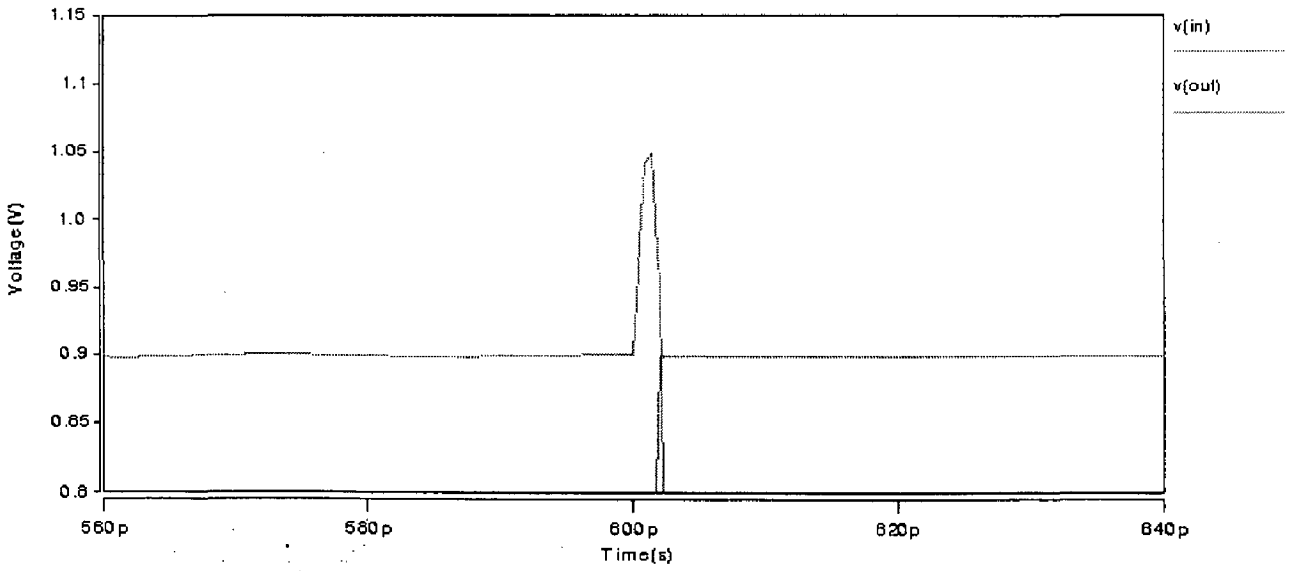


Figure 5.9 Magnified view of Potential rise using HSPICE simulations of bulk MOSFET.

Figure 5.9 shows the magnified view of the glitch at output of inverter and its value is found to be 0.15V which leads to power, timing and noise related problems and forces increased design margins. This clearly shows the superiority of MGDG devices in terms of glitches at the output.

5.4 Failure Probabilities and their Dependency on Leakage Currents

In addition to capacitance between input and output leakage currents in logic/memory circuits causes severe reliability problems especially with low voltage operation in nanometer regime. We found combined potential rise at critical nodes in memory both due to the small signal capacitances and due to leakage currents. Critical nodes are nodes whose potential variation is crucial for that particular read/write operation. Presence of leakage currents as well as on state currents makes voltage at '0' node to be raised to some non-zero voltage and voltage at '1' node to be lower than V_{dd}. This change in node voltages not only affect the drain to source voltages but also modify the node voltages of the p and n type MOSFETS and thereby influencing the leakage currents. In writing the KCL equations at nodes we have considered that subthreshold current flows in the same path of its origin, where as gate leakage current flows in the neighboring paths.

Applying KCL at the two nodes during read mode in figure 5.10 we get,

For '0' node

$$I_{edton\_3} + I_{gcs\_3} + I_{sub\_5} + I_{edtoff\_5} + I_{edton\_1} + 0.4I_{gcd\_1} + I_{edton\_6} + I_{edtoff\_2} + I_{ds\_3} - I_{ds\_1} = 0 \qquad (5.6)$$

For '1' node

$$I_{ds\_6} + I_{gcd\_6} - I_{btbtd\_2} - I_{sub\_2} - I_{edtoff\_2} = 0 \qquad (5.7)$$

In above equations the suffix 'ds' denotes drain current, 'edtoff' denotes offstate EDT current, 'edton' denotes onstate EDT current, 'sub' denotes subthreshold current, 'gcd' denotes gate to channel current and its drain component, 'btbtd' denotes drain to body band to band tunneling current and the symbol after underscore denotes transistor number.

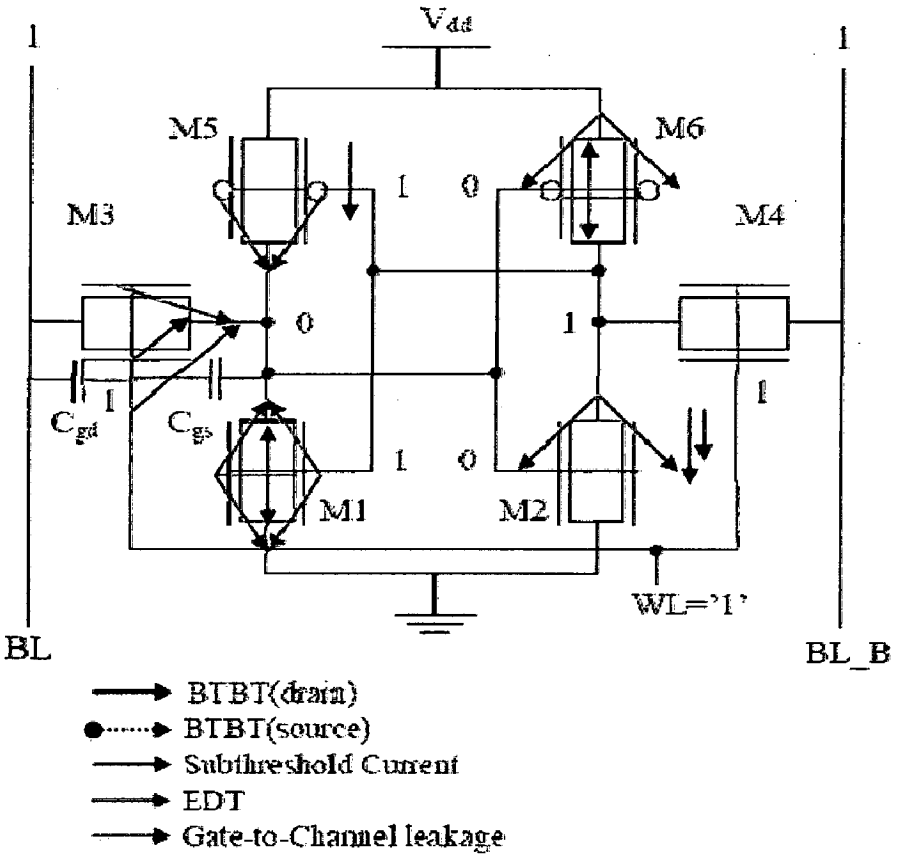


Figure 5.10 Leakage components in nanoscale DG SRAM cell during read operation.

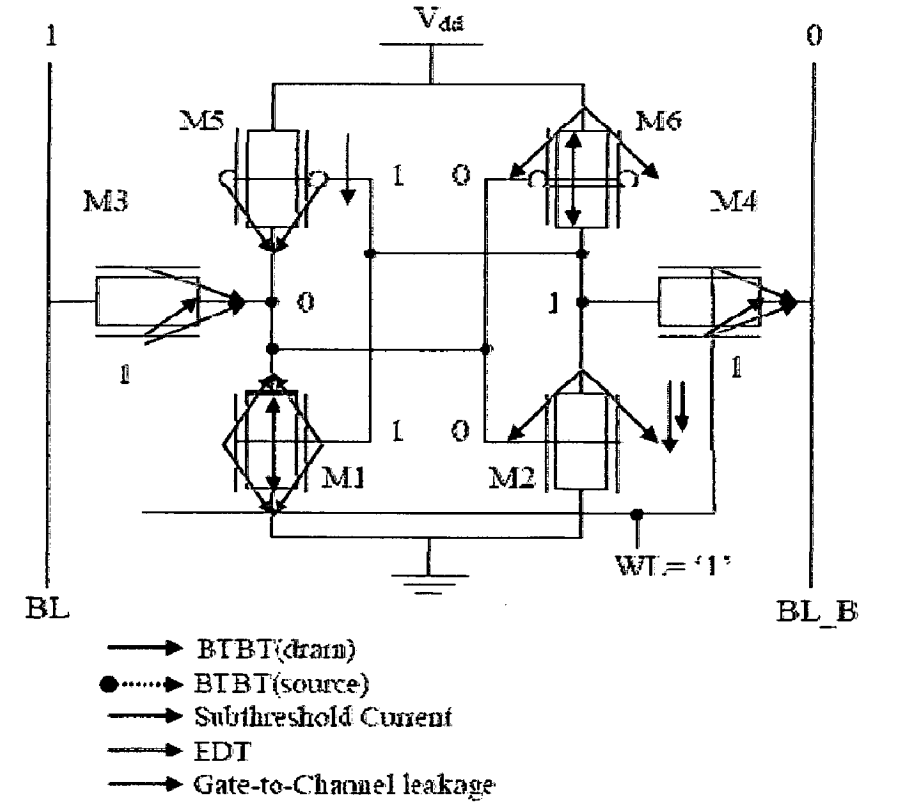


Figure 5.11 Leakage components in nanoscale DG SRAM cell during write operation.

The actual drain current expression is taken from [52], and we included quantum correction effects. We solve (5.6) and (5.7) self consistently in MATLAB simultaneous equation solver by giving some initial guess value to get the potential rise/fall at '0' and '1' nodes and accordingly leakage currents will also get modified. When the cell is in idle mode the potential rise at '0' node is found to be 10mV and potential fall at '1' node is found to be 17mV.The various leakage currents in different n-MOSFETS of MGDG are shown in the **table 5.1**. The first row represents leakage currents without considering the Interconnection effects i.e. potential variation at intermediate nodes due to leakage currents, while 2nd row represents those after these effects have been taken into account.

Table 5.1 Leakage Currents estimated using our analytical modeling for NMOS and their variation with potential fall at source.

Leakage ⟶	I_{sub} (V_{ds}=1) (mA/nm)	I_{gc} (V_{gs}=1) (mA/nm)	I_{edton} (V_{gd}=1) (mA/nm)	I_{edtoff} (V_{gd}=-1) (mA/nm)	I_{btbtd} (V_{gs}=-1) (uA/nm)
NMOS	1.298	0.8074	0.022	0.065	0.8712
NMOS(ΔV_s)	1.269	0.7124	0.0203	0.0632	0.762

Actually in the above table all leakage currents are found to be reduced but some times they can increase based on their surrounding potential. Suppose if we consider transistor M4 in read mode if at all there is a decrement in potential at '1' node due to leakage currents we will observe finite subthreshold leakage which ideally should be zero.

Table 5.2 Leakage Currents estimated using our analytical modeling for PMOS and their variation with potential fall at source.

Leakage ⟶	I_{sub} (V_{ds}=1) (uA/nm)	I_{gc} (V_{gs}=1) (nA/nm)	I_{edton} (V_{gd}=1) (nA/nm)	I_{edtoff} (V_{gd}=-1) (nA/nm)	I_{btbtd} (V_{gs}=-1) (nA/nm)
PMOS	0.7812	0.0939	7.98e-2	2.63e-2	0.0397
PMOS(ΔV_s)	0.7734	0.0912	7.734e-2	2.31e-2	0.0342

Gate leakage currents in PMOS are very less since oxide potential barrier is 4.5eV for PMOS compared to 3.14eV for NMOS using SiO_2 as gate dielectric which plays crucial

role in determination of gate leakage and EDT 'on' state leakage. Thus it is seen that due to the interconnection effect some leakage currents increases while others decreases and we are able to find steady state leakage currents due to potential rise/fall at intermediate nodes.

The width of pull-up PMOS considered in the analysis is 40nm and access NMOS transistor is 60nm for better writability and that of pull-down NMOS is 100nm for better readability. The various leakage currents in different n-MOSFETS of MGDG are shown in the **table 5.1** computed from our earlier analysis in [53] same way all leakage currents of PMOS are also tabulated in **table 5.2**. The first row represents leakage currents without considering the Interconnection effects i.e. considering potential variation at intermediate nodes due to leakage currents, while 2nd row represents those after these effects have been taken into account.

The threshold voltage of NMOS in our case is 0.31V and that of PMOS is -0.32V.Thus it is seen that due to the interconnection effect some leakage currents increases while others decreases and we are able to find steady state leakage currents due to potential rise/fall at intermediate nodes. In reading '0' node is critical since any potential raise there coupled with process parameter variations in M1 or M6 leads to read failure. When the cell is in idle mode the potential rise at '0' node is found to be 10mV and potential fall at '1' node is found to be 17mV.The potential fall at '1' node is more due to the more subthreshold leakage of M2. Simultaneous solution of KCL equations at '0' storing node of SRAM cell in Figure 5.10 gives potential rise in '0' node during the read operation to be 34mV which coupled with potential rise due to C_{gd} of 7mV will not raise above trip point of inverter M2-M6 hence read failure probability can be expected to be reduced. Since we are using supply voltage of 0.9V in above analysis we assumed trip voltage to be 0.4V. Similar analysis on Figure 5.11 using leakage currents in tables 5.1 and 5.2 shows that write failure probability using properly sized access and PMOS transistors (whose width ratio=1.5) is less and quick discharging takes place and it will not be worsened by combined effect of small signal capacitances and leakage currents. Using Berkeley predictive technology models for bulk CMOS technology at 22nm with Metal gate/high-K dielectric gives stand alone gate drain capacitance and gate-drain capacitance at lightly doped part of drain respectively to be[54],

CGD0=7e-11; CGD1=7.5e-13

Assuming symmetrical DGMOSFET structure with careful overlap regions and using BSIM SOI models the same are given by ,

CGS0= CGD0=19.27e-27; CGD1=Not given.

Above data shows that stand alone gate-drain capacitance is less as well as extracted small signal C_{gd} is also less for MGDG MOSFET which gives better noise, power and timing performance in digital/memory circuit design. Stand alone and small signal capacitances are added together while estimating the potential rise.

Chapter 6

Ultra Low Voltage SRAM Design Using MGDG MOSFET

6.1 Design Problems at Ultra Low Voltage SRAM

Memory power consumption can be reduced by reducing supply to a voltage which is just enough to retain data called data retention voltage which is further influenced by process variations of minimum geometry transistors used in present day technology. Maintaining almost constant Static Noise Margin (SNM) across different process corners is still challenging. One should maximize number of cells that can be connected to the bit line with reliable operation. Reduction of supply voltage during standby mode helps to reduce all the leakage currents to the minimum and the voltage which is just enough to retain cell data is called Data retention voltage (DRV). Analytical modeling of DRV for SRAM cell is needed by which the designer can find the minimum operating voltage of SRAM cell under process variations. Further memory in wireless sensor networks is in idle mode for longer times followed by a burst of data, so one should be able to operate reliably in ultralow voltage operation as well as achieving improved performance for faster processing of data.

6.2 Data Retention Voltage Analysis of MGDGMOSFET

In this work, we developed analytical modeling of Data retention voltage for MGDG MOSFET based SRAM cell based on previous work by B. H. Calhoun, H. Qin. *et. al* [9], [11] for bulk MOSFET. We found SNM variations with gate work function engineered MGDGMOSFET under different process corners and it is found that our MGDG MOSFET is more robust against process variations even in ultra low voltage operation. In order to stably preserve data in SRAM cell, the cross coupled inverters must have loop gain greater than one. Stability of SRAM cell is often indicated through Static Noise Margin (SNM), which is defined as the maximum possible square between VTC's of internal inverters [2], [9], [55]. Around Data Retention voltage VTC of internal inverters degrade to such a level that the loop gain reduces to one and SNM of SRAM cell falls to zero. Both PMOS and NMOS are in weak inversion region and equating their currents gives the transfer characteristics of the inverter. Applying above condition for M1-M5 inverters in Figure 6.1 yields,

$$I_{sn}\exp\left(\frac{V_{in}-V_{thn}}{m_n V_T}\right)\left(1-\exp\left(\frac{-V_{out}}{V_T}\right)\right) = I_{sp}\exp\left(\frac{V_{dd}-V_{in}-V_{thp}}{m_p V_T}\right)\left(1-\exp\left(\frac{V_{dd}-V_{out}}{V_T}\right)\right) \quad (6.1)$$

$$V_{in} = V_T\left(\frac{m_n m_p}{m_n+m_p}\right)\left(\ln\frac{I_{sp}}{I_{sn}}+\ln\left(\frac{1-\exp\left(\frac{-V_{dd}+V_{out}}{V_T}\right)}{1-\exp\left(\frac{-V_{out}}{V_T}\right)}\right)\right)+\frac{m_n V_{dd}}{m_n+m_p}+\frac{m_n m_p}{m_n+m_p}\left(\frac{V_{thn}}{m_n}-\frac{V_{thp}}{m_p}\right) \quad (6.2)$$

Where m_n, m_p are subthreshold slope factors for NMOS and PMOS respectively. V_{thn}, V_{thp} are threshold voltages for NMOS and PMOS respectively. I_{sp} and I_{sn} are subthreshold current at $V_{gs} = V_{th}$ and V_{ds} =0 for both PMOS and NMOS respectively. V_{dd} is supply voltage, V_T is thermal voltage, V_{in} is input voltage, V_{out} is output voltage of the inverter considered. Rather than p and n subscript one can use transistor number as subscript as in Figure 6.1.

Applying condition for DRV as the point where loop gain becomes one.

$$\left.\frac{\partial V_1}{\partial V_2}\right|_{\text{Left inverter}} = \left.\frac{\partial V_1}{\partial V_2}\right|_{\text{Right inverter}}, \text{ when } V_{dd} = DRV \quad (6.3)$$

From equations (6.1), (6.2) and (6.3) DRV value can be approximately given by,

$$DRV = V_T\left(\frac{m_1 m_6}{m_1+m_6}\right)\log\left[\left(\left(\frac{m_2+m_6}{m_2 m_6}\right)\frac{I_{s2}}{I_{s1}I_{s6}}\right)\times\left(\frac{I_{s3}}{m_1}+I_{s5}\left(\frac{m_1+m_5}{m_1 m_5}\right)\right)\right] \quad (6.4)$$

Above equation assumes that one is at perfectly '0' other node at perfectly '1', in general due to leakage currents it will not be so and there is small potential drain from node storing '1' and little bit rise at node storing '0' which can be evaluated by Kirchhoff's current law for leakage currents at respective nodes and it is estimated that 10mV rise is observed at node storing '0' and 17mV fall is observed at node storing '1'. The initial value of DRV is reasonably valid even leakage current analysis comes into picture. The value of subthreshold factor is analytically calculated to be ideal value of 1 for both PMOS and NMOS from our analysis in chapter 3. Ideal value of subthreshold factor allows for even lower DRV since transistors are almost ideal. We obtained DRV to be 79mV and it is little bit more than predicted by HSPICE simulations of 62mV since PMOS leakage in our case is underestimated.DRV is more influenced by off state

leakage current ratio of PMOS to access NMOS, so by properly optimizing the access transistor one can tune DRV according to the application.

6.3 Description of Subthreshold SRAM Cell Architecture

Figure 6.1 shows the read disturbance present at the '0' storing node of SRAM cell using minimum length transistors and '+' sign on PMOS of right inverter shows due to process variation its strength has been increased and '-' sign on NMOS shows due to process variation its strength has been decreased so it is more prone for read disturbance due to potential rise at '0' storing node and reduced trip point of inverter M2-M6.Read path in the below scheme consist of series connected NMOS's due to less drive current this leads to increase in read delay. Further, the disadvantage of this scheme is reduced driving capability of transistors with reduced supply voltage which results in degraded SNM.

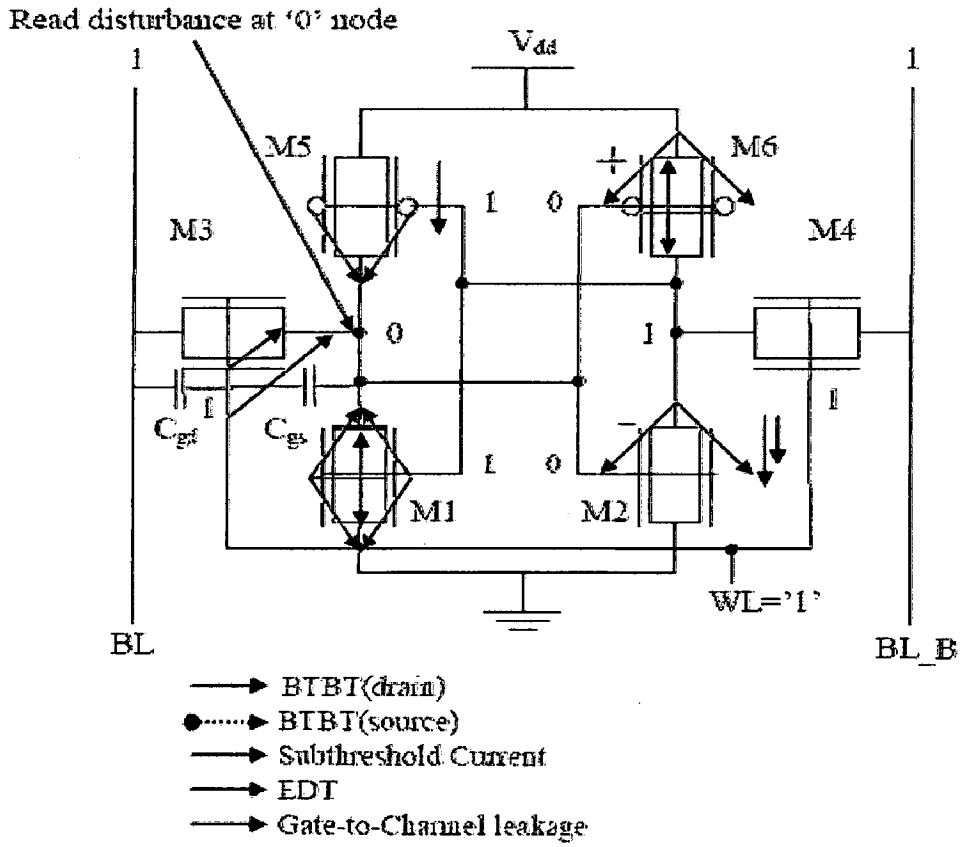


Figure 6.1 Read disturbance caused in nanoscale SRAM

Figure 6.2 shows the modification of conventional dual port memory cell for better readability in nanoscale regime by decoupling the storage nodes from bit lines [53]. In this case voltage at storage node is not influenced by read current so read stability degradation will not occur. Also, sense amplifier senses the current difference between connected gate MGDG with both gates at logic '1' and Independent gate MGDG where one gate is at '1' and other is at '0'. The main advantage of this scheme is improved

SNM. As supply voltage goes down read delay degradation as well as SNM remains almost constant for this scheme because ratio of on current at backgate voltage of V_{dd} to 0V increases. Read path in the proposed scheme consists of only one transistor compared to two transistors in earlier schemes there by leading to less delay.

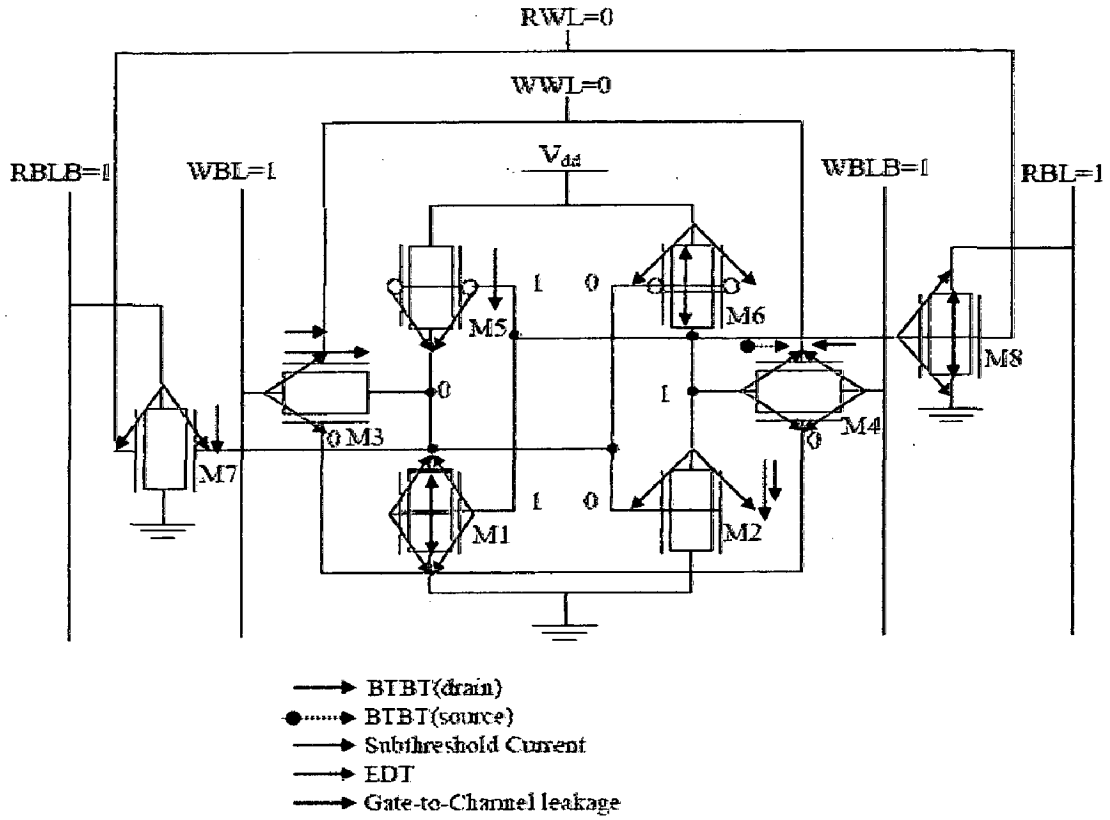


Figure 6.2 SRAM cell designed for subthreshold operation [56].

SNM is modeled mathematically [2] as

$$F1(V_L)=V_L+c$$
$$F2(V_L-S)=V_L-S+c$$
$$S=F2(V_L-S)-F1(V_L) \qquad (6.5)$$
$$\frac{\partial F1(V_L)}{\partial V_L}-\frac{\partial F2(V_L-SNM)}{\partial V_L}=0$$

Where F1 is transfer function of first inverter and F2 is transfer function of right inverter. Above equation shows maximum diagonal square that can be inserted into the lobes. Clearly from the above when the driving capability of transistors reduces due to reduction in supply voltage cell is more immune to disturbances due to degraded transfer functions F1 and F2.

Figure 6.3 shows the Static Noise Margin (SNM) of SRAM cell designed using MGDG MOSFET from H-Spice Simulations and MATLAB plotting. Due to decoupling of storage nodes from bit lines hold mode and read mode SNM are same and at 0.9V SNM is 197mV and at 0.4V it is 156mV clearly this degradation is much smaller than bulk MOSFET based SRAM's [31].

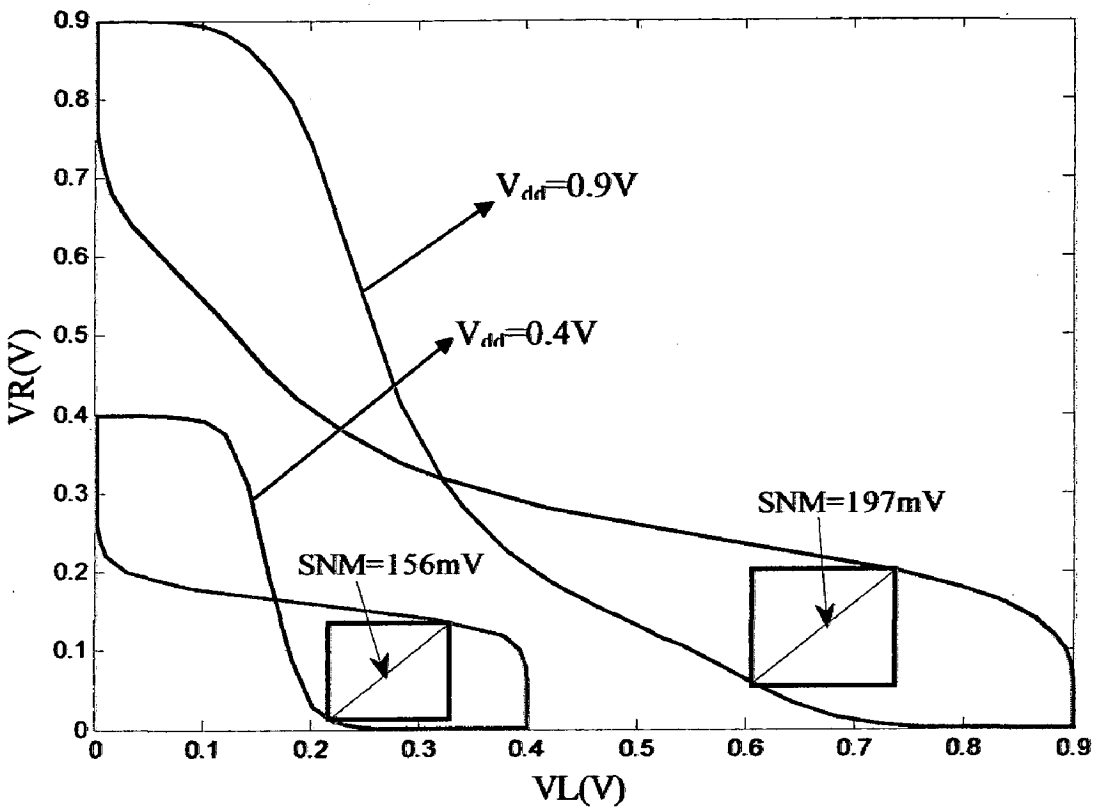


Figure 6.3 SNM under Read/Hold modes at different supply voltages.

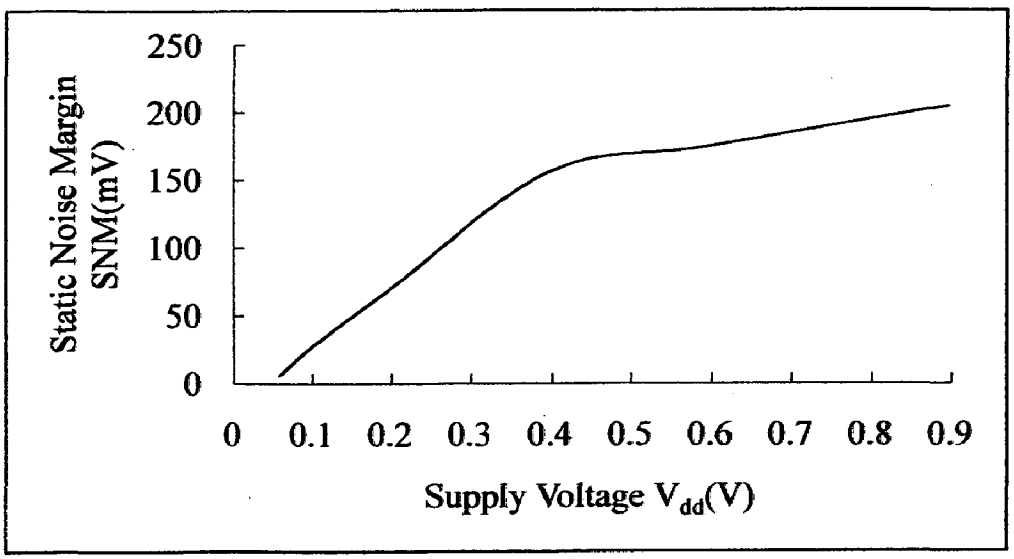


Figure 6.4 Variation of read/Hold mode SNM with supply voltage.

Figure 6.4 shows the variation of SNM with supply voltage and it is found that MGDG based SRAM cell can retain its data up to 62mV of supply voltage from HSPICE simulations which validates above analytical modeling. Also, SNM is found to degrade with supply voltage due to reduced driving capability of transistors making the transfer characteristics more immune to variations in transistor sizes.

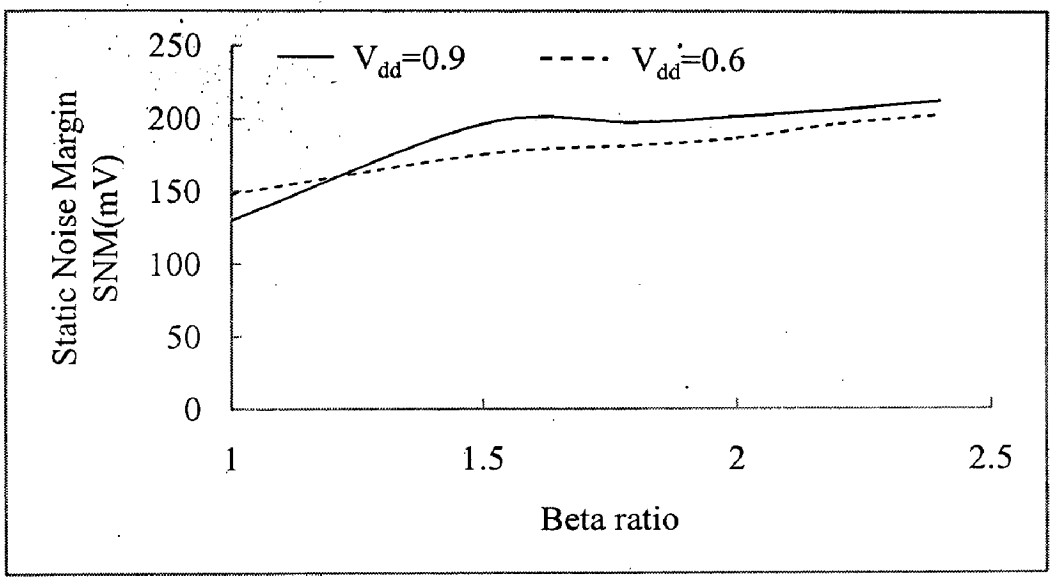


Figure 6.5 variation of read/hold mode SNM with Beta ratio

Figure 6.5 shows variation of read/hold mode SNM with beta ratio variations and it is found that our MGDG SRAM cell is more robust to process variations and can maintain welldefined SNM even at ultralow voltage operation.SNM degradation is less effected by beta ratio variations at lower supply voltages and more effected by beta ratio variations at higher supply voltages. This allows for more robust subthreshold operation of MGDG SRAM cell. Figure 6.6 shows the variation of read/hold mode SNM withthreshold voltage differences of cross coupled inverters and it is foud that due to threshold voltage differences SNM degrades more and 80mV variation is worst case variation where the cell is found to retain its data. Subthreshold SRAM is more influenced by process variations and due to leakages from neighbouring transistor in worst case number of transistors that can be connected to the bitline is limited [26]. One should calculate the optimum number of transistsors that can be connected to bitline by applying KCL on both sides and finding under worst case process variations as in equation (6.5).

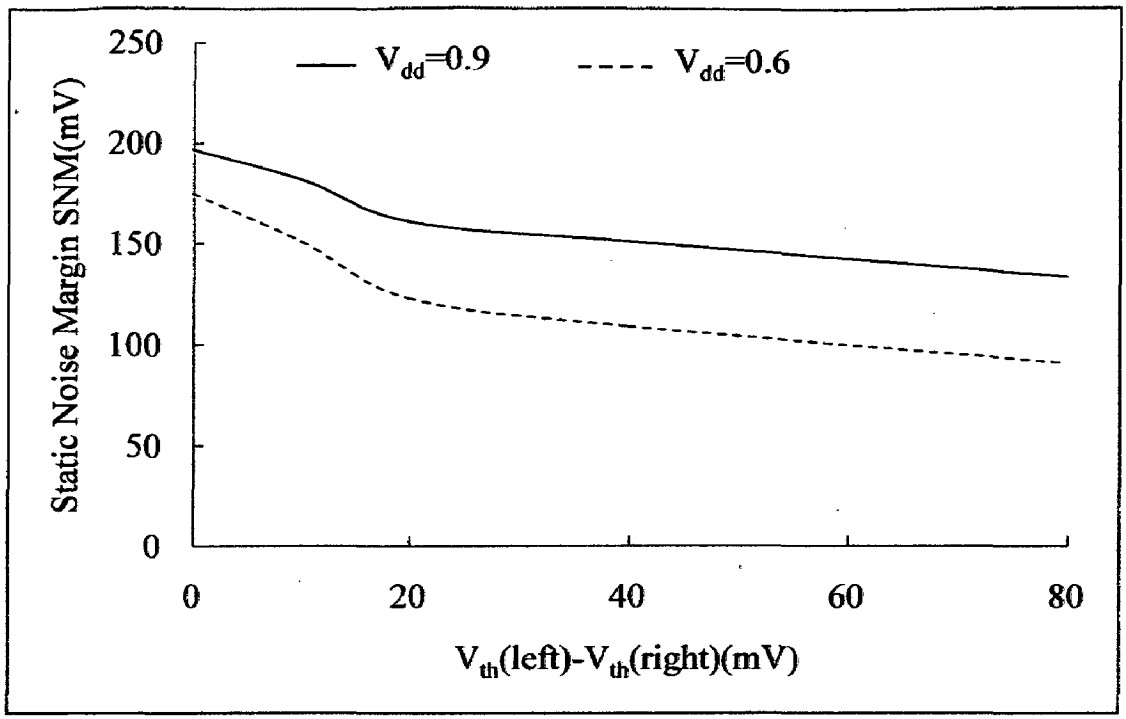


Figure 6.6 variation of read/hold mode SNM with threshold voltage differences of cross coupled inverters

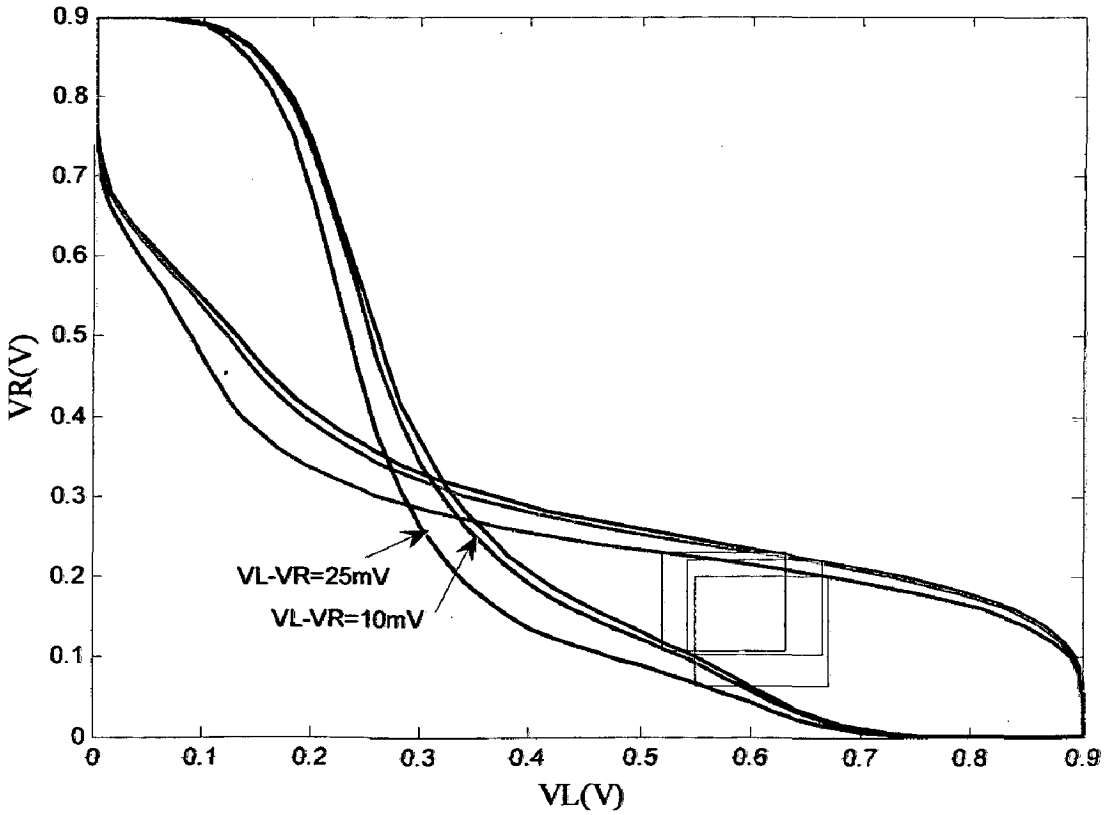


Figure 6.7 SNM variation due to Process Variation

Figure 6.7 shows the SNM variation under process variation where it is found that the MGDG SRAM cell is more robust to process variations.SNM variation remains almost

constant irrespective of process variations due to reduced sensitivity of MGDG MOSFET to parameter variations.

6.4 Results for Ultralow Voltage SRAM Cell Design

We have used Independent gate sense amplifier as reported in [57], for achieving high performance. The worst case condition during read operation is described in figure 6.8 where leakage drain from off transistors presents reduced differential for sense amplifier there by causing failure[31], [32]. Number of cells that can be connected to the bit line is given by the condition,

$$(n\text{-}1)\left[I_{off}@\left(V_{bg}=V_{dd}\right)\text{-}I_{off}@\left(V_{bg}=0\right)\right]<\left[I_{on}@\left(V_{bg}=V_{dd}\right)-I_{on}@\left(V_{bg}=0\right)\right] \quad (6.5)$$

Where $I_{off}@\left(V_{bg}=V_{dd}\right)$ is off current at backgate bias of V_{dd}, $I_{off}@\left(V_{bg}=0\right)$ denotes off current at backgate bias of zero. Similar explanation applies for on currents. Under worst case process variations $I_{on}@\left(V_{bg}=V_{dd}\right)-I_{on}@\left(V_{bg}=0\right)$=40nA for 32nm node, Assuming access transistor width of 50nm $I_{off}@\left(V_{bg}=V_{dd}\right)\text{-}I_{off}@\left(V_{bg}=0\right)$=0.612pA, one can calculate almost 50,000 transistor under ideal condition. Even under severe process variation one can accommodate for 1ktransistors/bitline.

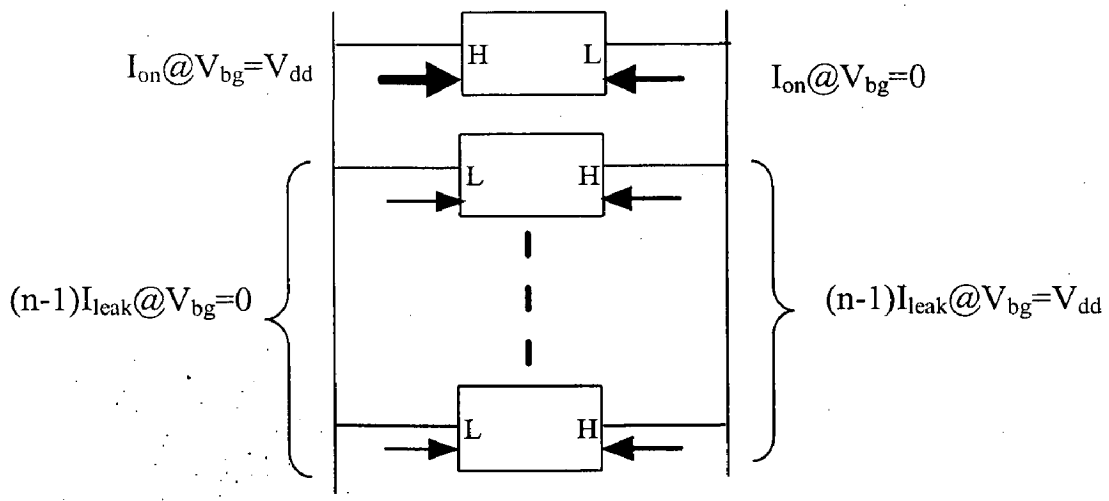


Figure 6.8 Worst case condition during read operation.

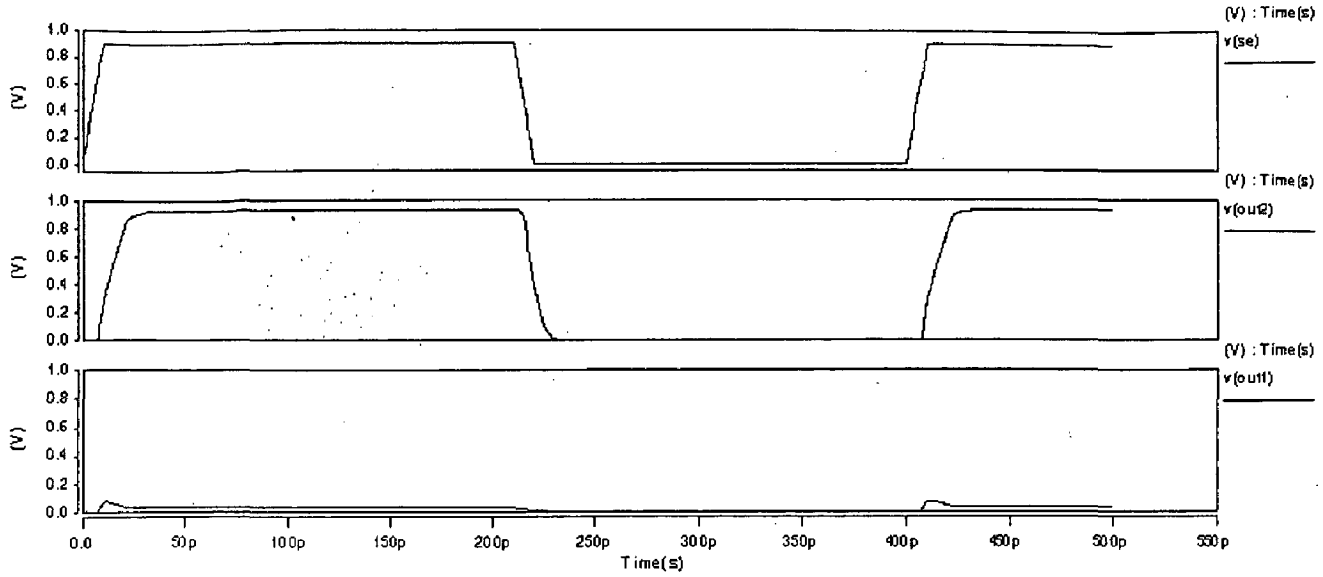


Figure 6.9 Output of Sense amplifier during reading phase of SRAM cell

Figure 6.9 describes the output of reading circuitry (sense amplifier and associated circuitry) during read operation (se) is sense amplifier enable signal. V (out2) is output2 of sense amplifier and V (out1) is output1 of sense amplifier. BLB is inverted version of bit line and gets discharged since '1' is written onto cell and we observe 'out2'rising high as shown in figure. V (out1) is zero at all times since after inversion pre-charged output goes to zero.

Delay observed in normal read operation of sense amplifier is 0.807ns (Assuming decoding delay of 0.641ns based on delay simulations of NAND gate) and power is 95uW.

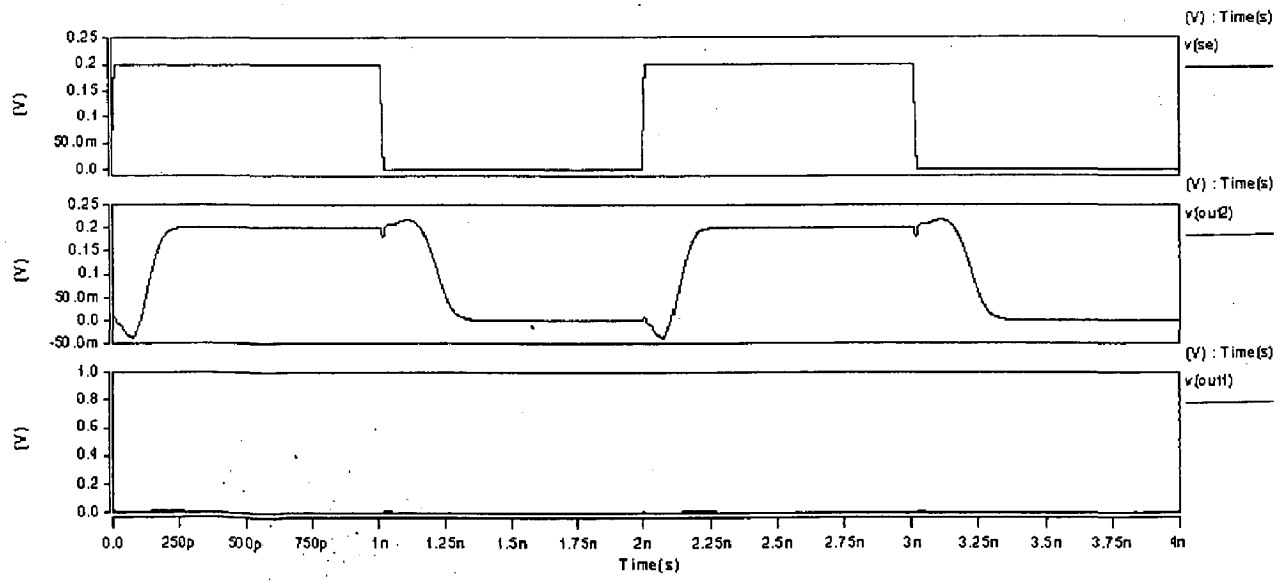


Figure 6.10 Output of Sense amplifier during reading phase of SRAM cell at ultra low voltage.

Figure 6.10 shows that it works well down to supply voltage of 0.2V. In subthreshold operation delay observed is 3.017ns (Assuming decoding delay of 2.1ns based on delay simulations of NAND gate) and power is 6.57uW.

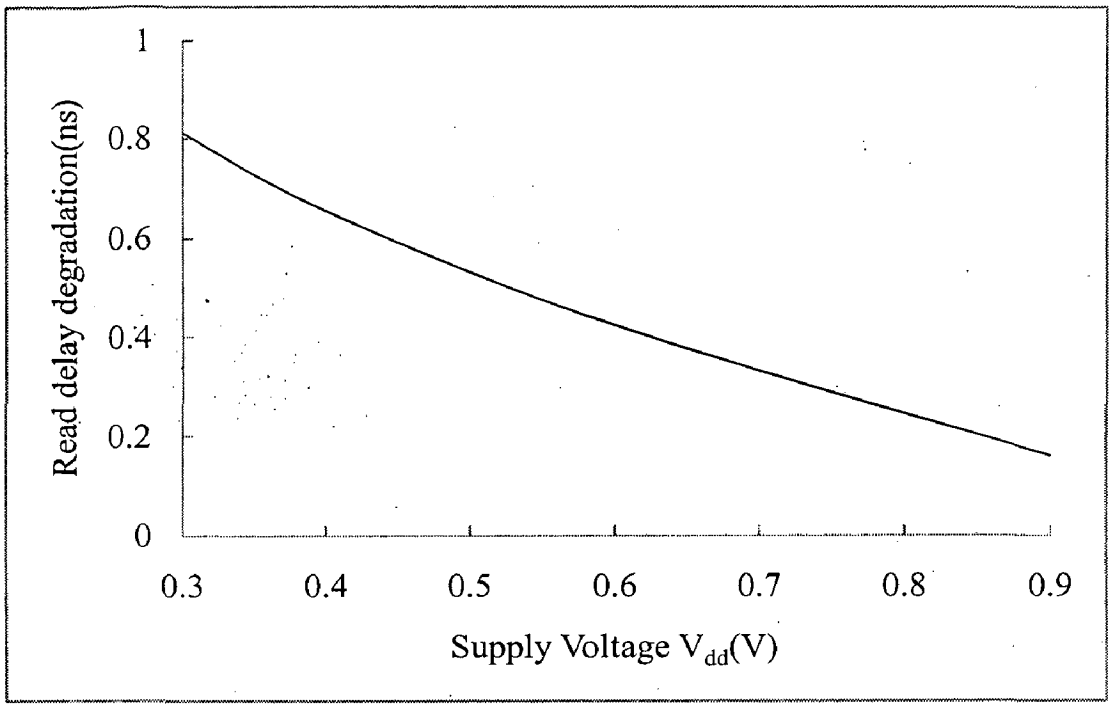


Figure 6.11 read delay degradation of the proposed scheme.

Figure 6.11 shows read delay degradation of the proposed scheme. Delay degradation is less in proposed scheme due to increased on current ratio at backgate bias of V_{dd} and 0V respectively at lower voltages. This clearly indicates the superior performance of proposed scheme in ultra low voltage operation.

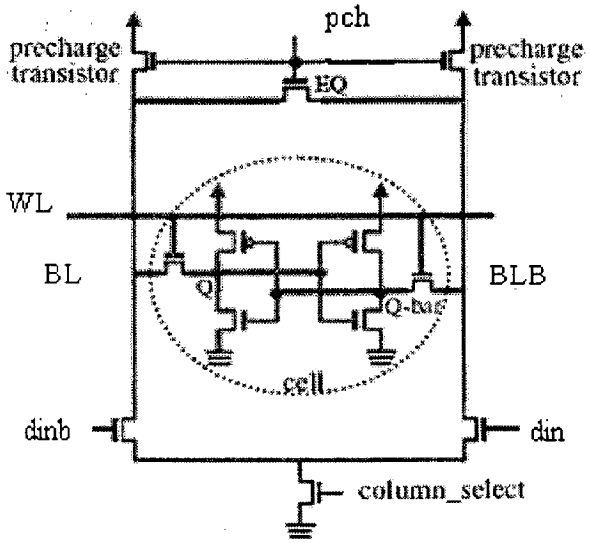


Figure 6.12 Circuit for writing into the memory cell [58].

Figure 6.12 shows overwriting approach of writing into the cell. Initially both the bit lines are pre-charged to V_{dd} during pre-charge operation. When Pch and WL for the memory cell goes high, the circuit evaluates the voltage in the bit lines based on data input.

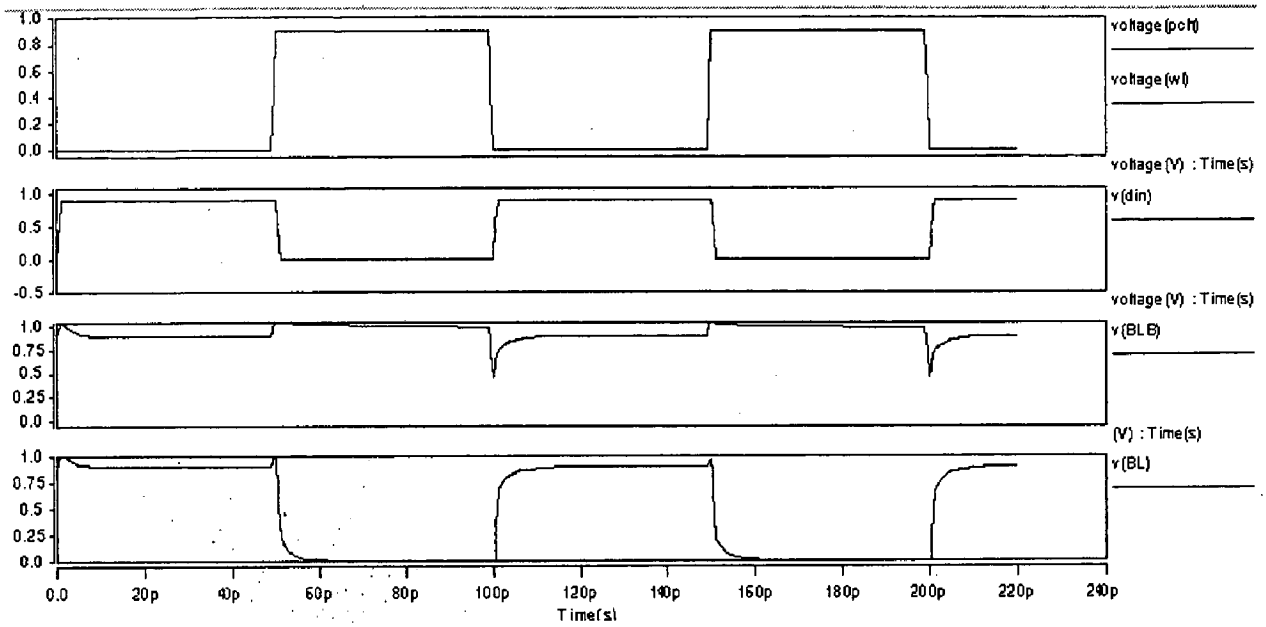


Figure 6.13 Output of writing circuitry of MGDG-SRAM cell at 0.9V supply voltage.

Figure 6.13 Output of writing circuitry of MGDG-SRAM cell at 0.9V supply voltage.
As can be seen when pch is low both the bit lines are pre-charged and based on data when word line goes high data will be written onto the cell.

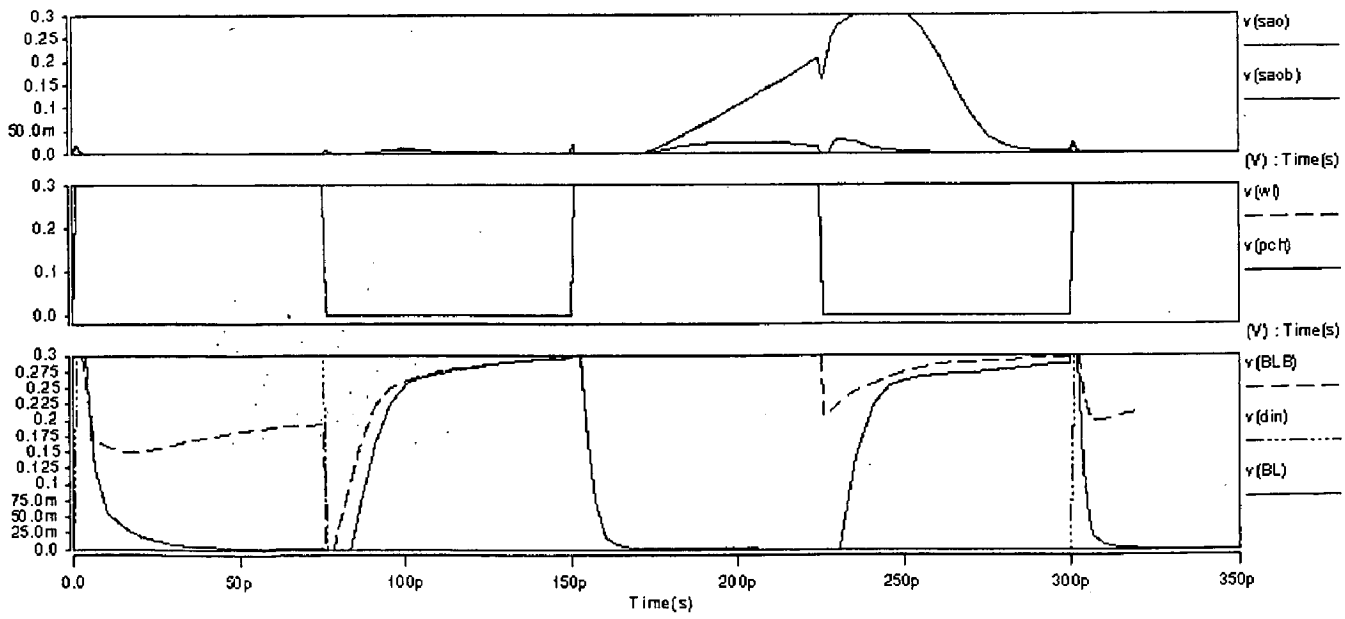


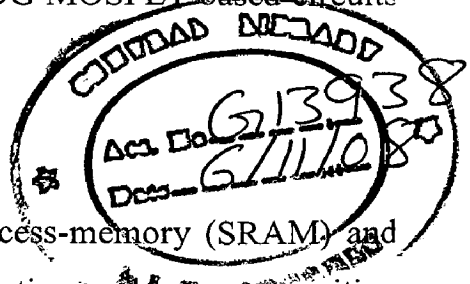
Figure 6.14 Output of complete SRAM cell at ultra low voltage operation.

Figure 6.14 shows the output of complete SRAM cell at ultra low voltage operation. Initially based both bit lines gets pre-charged to V_{dd} when pch is low. When word lines goes high data of '1' is written onto the cell and during next cycle sense amplifier is enabled during late in the cycle after proper differential gets developed across the cell and data of '1' is presented at the sense amplifier normal output which we have written in the previous cycles. Here due to subthreshold operation of circuit sense amplifier takes longer time of around 25ps to read the data.

Chapter 7

Conclusion and Further Scope

Our analysis shows that use of MGDG devices with intrinsic body doping reduces transition overhead introduced by body biasing mechanisms for leakage reduction. The design is insensitive to parameter variations when MGDG devices are used. We did analytical modeling of the small signal capacitances that affect circuit operation from which glitch voltage at the output has been evaluated and validated through HSPICE simulations and less glitch voltage has been observed for MGDG MOSFET than bulk MOSFET. Our analysis shows that use of MGDG devices with intrinsic body doping reduces voltage rise in output node during signal transition events. Also, we estimated all leakage currents by considering interconnect effect and used them in finding voltage rise/fall at the critical nodes of SRAM cell. Increased potential at output node during transition from 0-1 is responsible for presence of steady state charge in body of silicon film which causes noise in the system. Read/write failures have been shown to be reduced in SRAM designed with MGDG MOSFET, due to reduced leakage currents and reduced variability and also potential rise due to wordline signal transition from 0-1 causes very small potential rise at node storing '0' which otherwise may flip the data stored. We did rigorous HSPICE simulations of MGDG MOSFET based SRAM cell with process variations and estimated read/hold mode Static Noise Margin with process variations. We are able to operate the cell down to 0.3V supply voltage and it is less affected by process variations than at higher voltage. So, our gate workfunction engineered MGDG MOSFET is more robust to process variations and gives superior performance even under ultra low voltage operation. We are able to maintain almost constant SNM even under process variations at ultra low voltage operation. This work can be useful in characterization of delay and power in MGDG MOSFET based circuits there by making the job easier at higher levels of abstraction.



In short contributions of this dissertation are the following:

- A detailed discussion on prevalent static random-access-memory (SRAM) and cache design techniques, their leakage minimization schemes, transition

overhead generated and their minimization using MGDG MOSFET.

- We estimated the small signal capacitances and glitch voltage present in circuits designed using MGDG MOSFET and its verification through HSPICE.
- We estimated the leakage currents using interconnection effect and applied the same for estimating the voltage rise/ fall in SRAM cell designed using MGDG MOSFET.
- Estimated the Data retention voltage through analytical modeling as well as through HSPICE and it is found to be 62mV. Estimated the hold mode SNM to be 197mV at supply voltage of 0.9V at 32nm.
- Performed read/write operations on ULP SRAM cell at 0.3V supply voltage and estimated SNM across different process corners from HSPICE simulations.

Further Scope of this work is as follows,

1. Characterization of standard library elements designed using MGDG MOSFET for their delay and power which reduces design time at higher levels of abstraction.
2. Optimizing the access transistor so that its delay is almost independent of input wave form rise time for improved read and write times.
3. Usage of nitrided gate dielectrics makes uniform gate leakage currents for both PMOS and NMOS there by shrinking data retention voltage further and gives more robust SRAM cell.

Power Dissipation Analysis of Decoder Using Stack effect

At nanometer regime each leakage component plays important role in determining leakage. The subthreshold leakage is the weak inversion current between source and drain of an MOS transistor when the gate voltage is less than the threshold voltage and is given by,

$$I_{sub} = 2\mu_o C_g \frac{W}{L_{eff}} V_T^{\,2} \exp\left(\frac{V_{gs} - V_{th}}{nV_T}\right) \cdot \left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \qquad \text{(A.1)}$$

where μ_0 is the zero bias electron mobility, n is the subthreshold slope coefficient, V_{gs} and V_{ds} are the gate-to-source voltage and drain-to-source voltage, respectively, V_T is the thermal voltage, V_{th} is the threshold voltage, C_{ox} is the oxide capacitance per unit area, and W_{eff} and L_{eff} are the effective channel width and length, respectively. Due to the exponential relation between V_{th} and I_{sub}, an increase in V_{th} sharply reduces the subthreshold current. Subthreshold leakage is a strong function of the threshold voltage V_{th} and temperature T, since they both appear in exponential terms. Current in this regime is undesirable in digital designs, because it results in a leakage current when an ideal transistor would be completely cutoff. This leakage is especially egregious when multiplied by the millions of leakage paths present in modern designs.

A.1 Stack effect Analysis of Leakage Power

$$I_{s1} = I_o \exp[-V_{th} / nV_T] \qquad \text{(A.2)}$$

Where $I_o = 2\mu_o C_g \frac{W}{L_{eff}} V_T^{\,2}$, the factor $\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right)$ can be eliminated with reasonable accuracy when $\left(\frac{V_{ds}}{V_T}\right) > 2$.

Using BSIM SOI model [54] and substituting all the parameters as given in BSIM SOI model cards reported in table I,

$$V_{th} = v_{tho} + k1\sqrt{\phi_s} - \eta V_{ds} \quad \text{(A.3)}$$

Where V_{tho} is the threshold voltage at zero bias, ϕ_s is twice the Fermi potential, k_1 represent dependence of surface potential even after inversion, η represents Drain Induced Barrier Lowering (DIBL) effect which is found analytically to be 17mV/V.

$$I_{s1} = I_o \exp[-(k_1\sqrt{\phi_s} - \eta V_{dd})/nV_T] \quad \text{(A.4)}$$

But for two transistor stacking case,

$$I_{s2} = I_o \exp[-(k_1\sqrt{\phi_s} - \eta V_{ds2})/nV_T] \quad \text{(A.5)}$$

$$= I_o \exp[(-V_{ds2} - (k_1\sqrt{\phi_s} - \eta V_{dd}))/nV_T] \quad \text{(A.6)}$$

Solving above equations, We get

$$V_{ds2} = \eta V_{dd}/(1+\eta) \quad \text{(A.7)}$$

Hspice simulations show that $V_{ds3} < V_T$

$$I_{s3} = I_o \exp[(-(k_1\sqrt{\phi_s} - \eta V_{ds3}))/nV_T]\left(1 - \exp\left(\frac{-V_{ds3}}{V_T}\right)\right) \quad \text{(A.8)}$$

$$= I_o \exp[(-V_{ds3} - (k_1\sqrt{\phi_s} - \eta V_{ds2}))/nV_T] \quad \text{(A.9)}$$

$$= I_o \exp[(-V_{ds2} - V_{ds3} - (k_1\sqrt{\phi_s} - \eta V_{dd}))/nV_T] \quad \text{(A.10)}$$

Solving (A.8) and (A.9) and $V_{ds2} = \eta V_{dd}/(1+\eta)$ (A.11)

The exponential term can be replaced by $\exp\left(\frac{-V_{ds3}}{V_T}\right) = 1 - V_{ds3}/V_T$ for $V_{ds3}/V_T < 1$

Solving (A.9), (A.10) gives $\log\left(\frac{V_{ds3}}{V_T}\right) + \frac{(1+\eta)}{n}\frac{V_{ds3}}{V_T} = \frac{\eta^2 V_{dd}}{(1+\eta)nV_T}$ (A.12)

The typical BSIM SOI 3.2 parameters for 32nm FINFET are given by,

K_1=0.001, η=0.017, V_{tho}=0.2, n=1, V_{dd}=0.9V.

Substitution of above parameters in (A.12) makes the second term in Right Hand Side 0.0341 which can be neglected.

$$\log\left(\frac{V_{ds3}}{V_T}\right)+\frac{(1+\eta)}{n}\frac{V_{ds3}}{V_T}=0 \qquad (A.13)$$

V_{ds3} is given by V_{ds3}=0.54 V_T=14.1mv

So, leakage currents at 32nm for Single Stack, double stack and triple stack are respectively given by,

$$I_{s1}=I_o\exp\left\{\left((1+\eta)V_{ds3}-V_{tho}+\eta V_{dd}\right)/nV_T\right\}==1.8I_o\exp\{(-V_{tho}+\eta V_{dd})/nV_T\}$$

$$I_{s2}=1.8I_o\exp(-V_{tho}/nV_T)$$

$$I_{s3}=I_o\exp(-V_{tho}/nV_T)$$

$$I_{s1}:I_{s2}:I_{s3}=1.8\exp(\eta V_{dd}/nV_T):1.8:1 \qquad (A.14)$$

The above equation shows that Drain Induced Barrier Lowering (DIBL) plays important role in subthreshold regime and it is important to minimize it for low power applications. Since MGDG MOSFET has reduced Drain Induced Barrier Lowering effect we can use it in low power applications.

Table A-1 Parameters of BSIM SOI 3.2 NMOS Model card for 32nm FINFET

Vtho=0.31V	DVT1 = 0.55
k1 = 0.00001	NLX = 0
k2 = 0.001	DVTOw = 0
k3 = 0	DVT1w = 0
k3B = 0	DVT2w = 0
DVT0 = 0.002	

Appendix-B : List of parameters used in simulation

S. No	Parameter	Values (Reference)
1	m_0	$9.031 * 10^{-31}$ kg
2	m_1^*	$0.19m_0$
3	m_2^*	$0.98m_0$
4	m_{SiO_2}	$0.61m_0$
5	m_{d1}	$0.19m_0$
6	m_{d2}	$0.43m_0$
7	$E_{g_{SiO_2}}$	5 eV
8	$E_{g_{Si_3N_4}}$	9 eV
9	g_1	2
10	g_2	4
11	W	20nm [1]
12	L_{eff}	20nm [1]
13	DIBL	19mV/V
14	t_{si}	5nm [1]
15	t_{ox}	1nm [1]
16	ϵ_{si}	$104.47 * 10^{-12}$ Farad/m
17	ϵ_{ox}	$34.53 * 10^{-12}$ Farad/m
18	m	1.082
19	h	$6.625 * 10^{-34}$ Joule-sec
20	k	$1.38 * 10^{-23}$ Joules/kelvin
21	q	$1.602 * 10^{-19}$
22	V_{fb}	-0.21V
23	V_t	0.026mV
24	Φ_{Gfs}	-0.21V
25	Φ_{Gbs}	-0.21V
26	V_{thf}	-0.31V
27	V_{thb}	-0.31V
28	N_A	$1.5x10^{16}$ m^{-3}
29	$N_{D/S}$	10^{18} m^{-3}

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List of Publications

[1] Venkata Komal, Santosh Kumar Vishvakarma, Ramesh Joshi, Ashok Saxena, Sudeb Dasgupta, "Leakage Optimization for Nanoscale MGDG MOSFET using Dual Metal (Hf/HfN) Gates with AlNx Buffer Layer," *12th IEEE VLSI Design And Test Symposium (VDAT-08)*, Bangalore, India (Accepted).

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