DESIGN OF OP-AMP FOR ANALOG TO DIGITAL CONVERTERS

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices and VLSI Technology)

By

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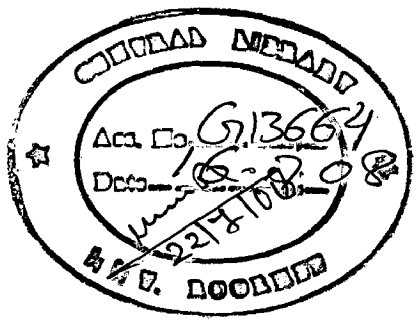

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is presented in this dissertation report, entitled **"DESIGN OF OP-AMP FOR ANALOG TO DIGITAL CONVERTERS"**, being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Electronics and Communication Engineering** with specialization in **Semiconductor Devices & VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work carried out from July 2006 to June 2007, under guidance and supervision of **Prof. A.K Saxena**, Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not been submitted for the award of any other Degree or Diploma.

Date: 27/6/07
Place: Roorkee

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CERTIFICATE

This is to certify that the statement made by the candidate is correct to the best of my knowledge and belief.

Date: 27/06/07
Place: Roorkee

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ABSTRACT

A method has been developed for determining component values and transistor dimensions for CMOS operational amplifiers (op-amp). Design objectives and constraints are specified as functions of design variables. The various design variables that are widely used in operational amplifier parameters like Common mode rejection ratio (CMRR), open loop gain, slew rate, Power Supply Rejection Ratio (PSRR) are designed. This approach gives robust designs i.e. designs guaranteed to meet specifications for a variety of process conditions and parameters.

In operational amplifier circuit at moderate gain and frequency there is a good agreement between actual and ideal performance. As gain and /or frequency are increased certain op-amp limitations come into play that effect circuit performance. Calculation of these limitations can be done with proper understanding of internal structure and the processes used to fabricate the op-amp. Design of device parameters is done by considering specification of these limitations.

Simulation study has been done using T-spice at .8um technology node. The theoretical calculations are in well agreement with the simulated output.

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PUBLICATION

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Chapter 1 Introduction

1.1 Introduction

Digital signal processing (DSP) requires an interface between real world analog signal and DSP function block. This is typically done by using Analog to Digital converter(ADC) .High speed Analog to Digital Conversion is required for many applications. Parallel pipelined ADC architecture is fastest, with low power and yields high resolution conversion [1, 2]. There are three most critical problems in these ADC's.

(i) Sample and Hold(S/H) block as it sees full bandwidth of input signal.

(ii) Clock jitter (jitter on sampling edge degrades performance when input frequency is high).

(iii) Path mismatching.

The primary objective of this work is to reduce the non-idealities of S/H circuit [2, 3]. Typically this is achieved by selecting optimized values of design parameters of operational amplifier (op-amp) used in design of S/H circuit.

Error sources of parallel pipelined ADC related to parallelism are

(i) Channel offset.

(ii) Channel gain mismatch.

(iii) Timing mismatch.

Channel offset is due to op-amp offset mismatch, charge injection of MOSFET, mismatch in S/H gain of each channel .This is additive and independent of input signal level and frequency. Channel gain mismatch is due to op-amp dc gain mismatch [4] .This has effect of convolving with existing spectrum and produces new frequency components at output. Timing mismatch is due to clock generator network, actual turning off time of MOS Switches in S/H circuits, thermal noise of electronic devices.

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By proper design of op-amp parameters can reduce nonlinearities of S/H circuit significantly. The automated sizing of CMOS op-amps directly from specifications so that circuit designer can spend more time doing real design i.e. carefully analyzing the tradeoff between competing objectives and less time doing parameter tuning or wondering whether certain set of specifications can be achieved. This method unambiguously determines feasibility of set of specifications and produces design that meets specifications or it provides proof that specifications can't be met.

Initially analytical expressions for Dimension, Bias, Signal swing and Power constraints are derived by hand (This can also be automated). In addition small signal transfer function, other constraints like Slew Rate, Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR) are derived by hand [5, 6, 7].

In this, various design parameters of op-amp like CMRR, Slew Rate and PSRR performance are computed. Finally, the model results which are theoretically calculated with Spice simulations are compared.

1.2 Outline of the Thesis

This thesis is organized into the following chapters.

Chapter1: Introduces the problem of op-amp design for S/H circuit. It gives overview of various design parameters of op-amp and introduces automated sizing of CMOS amplifiers directly from specifications.

Chapter2: Deals with the fundamentals of op-amp and its main design parameters. It explain about various specifications of op-amp like Unity Gain Bandwidth, CMRR, PSRR, Slew Rate (SR), Input common mode voltage range, Equivalent Input Noise, Maximum Output Voltage Swing.

Chapter3: Deals with the design constraints of two stage CMOS op-amp. It explains Dimension constraints, Bias conditions, and Signal Swing and Power constraints for automated sizing of individual components in op-amp design. It also explains small

signal transfer function constraints and other constraints like Slew Rate, CMRR and PSRR specifications for op-amp design.

Chapter4: This chapter deals with design of two stage CMOS op-amp from its parameters. It involves theoretical calculation of design parameters of op-amp.

Chapter5: This chapter shows the simulation results obtained from spice simulations at 0.8um technology node.

Chapter6: This chapter gives conclusion of present work and gives a note of future scope of this work.

2.1 Introduction

An operational amplifier, usually referred to as an 'op amp' for brevity, is a special kind of amplifier. A variety of mathematical operations can be performed, for configuring its external components [8]. In early 40's op amps were made from vacuum tubes. It consumes a lot of space and energy. After wards op amps were made smaller by implementing them with discrete transistors. Now a day's op amps are monolithic integrated circuits based on CMOS technology which are highly efficient and cost effective.

2.2 Model of Ideal Op Amp

Thevenin model of the op amp is shown in Figure 2.1. An op amp is a differential to single-ended amplifier [8, 9]. It amplifies the voltage difference ($V_d = V_p - V_n$) on the input port and produces a voltage V_o on the output port that is referenced to ground. This model still has the loading effects at the input and output ports as shown in Fig.2.1. The ideal op amp model was derived to simplify circuit calculations and is commonly used by engineers in first order approximation calculations.

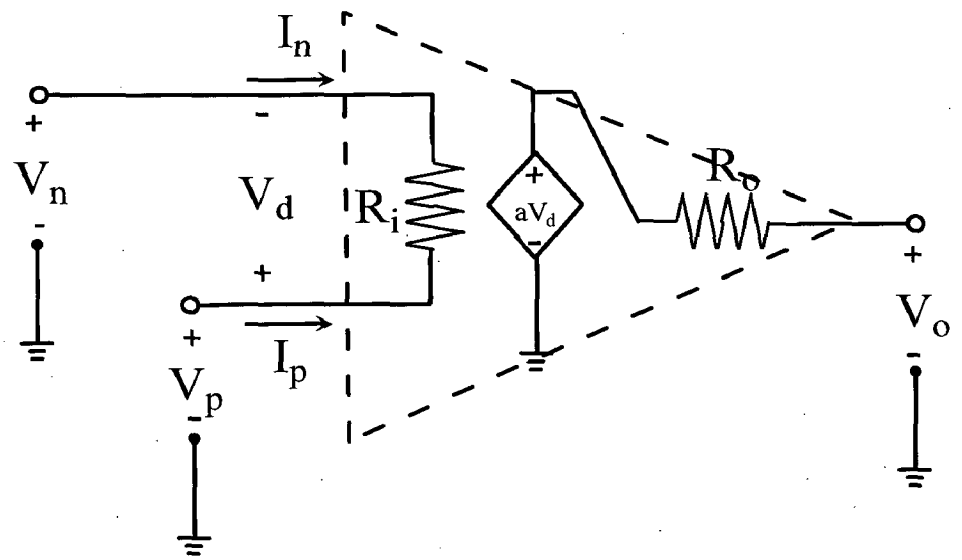

Fig.2.1: Thevenin model of the op amp

The ideal model makes three simplifying assumptions

- Gain is infinite a = ∞ (1)
- Input resistance is infinite $R_i = \infty$ (2)
- Output resistance is zero $R_o = 0$ (3)

By considering these assumptions to Figure 2.1, It will be converted as the ideal op amp model which shown in Figure 2.2. It's free from loading effects at the input and out put nodes. Consider the op amp as voltage controlled voltage source.

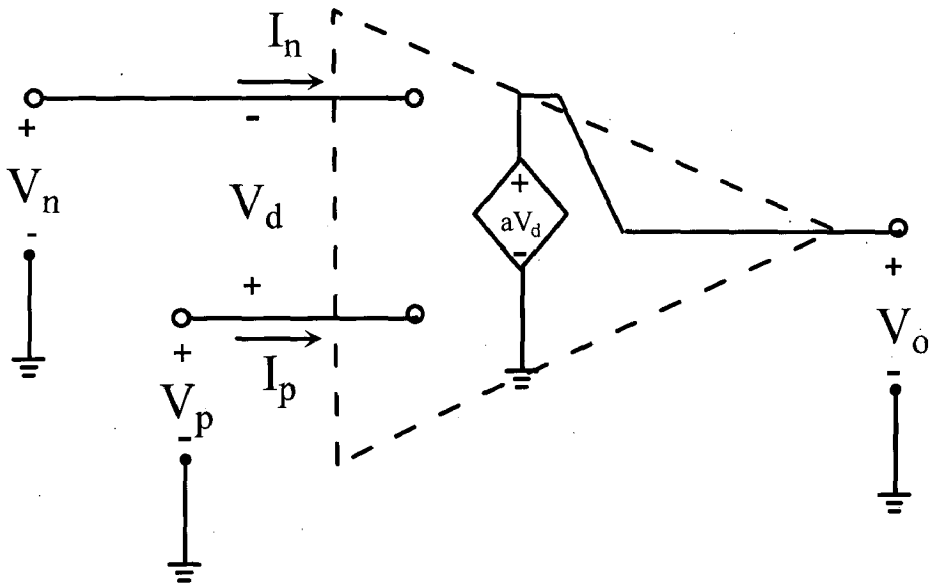

Fig. 2.2: Ideal Op Amp Model

Applying KCL at the i/p node for the ideal op amp model

$$\Rightarrow I_n = I_p = 0 \quad (4)$$

Applying KVL to the o/p loop for the ideal op amp model

$$\Rightarrow V_o = a\, V_d \quad (5)$$

For the liner mode operation, V_o must be a finite voltage. By definition $V_o = a\, V_d$.

Rearranging, $V_d = V_O / a$. Since $a = \infty$, $V_d = V_o / \infty = 0$.

$$\Rightarrow V_d = 0 \tag{6}$$

This is the basis of the virtual short concept.

For ideal op amp voltage at the output port depends only on the voltage difference across its input port. It rejects any voltage common to V_n and V_p.

$$\Rightarrow \text{Common mode gain} = 0 \tag{7}$$

Here frequency dependency is not considered.

$$\Rightarrow \text{Bandwidth} = \infty \tag{8}$$

$$\Rightarrow \text{Slew Rate} = \infty \tag{9}$$

There are no changes in performance over time, temperature, humidity, power supply variations, etc.

$$\Rightarrow \text{Drift} = 0 \tag{10}$$

2.3 Non-Inverting Op Amp

An ideal op amp by itself is diverging i.e. any finite input signal would result in infinite output. Connection of external components around the ideal op amp yields useful amplifier circuits [10]. Figure 2.3 shows a basic op amp circuit, the non- inverting amplifier. The input terminal marked with a + (V_p) is called the non-inverting input; – (V_n) marks the inverting input.

A relationship between the input voltage V_i, and the output voltageV_0, is required to understand the circuit operation. By applying KVL, KCL and ideal op amp characteristics, the relation between V_0 and V_i as follows

$$A = \frac{V_0}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1+\frac{1}{ab}}\right) \tag{11}$$

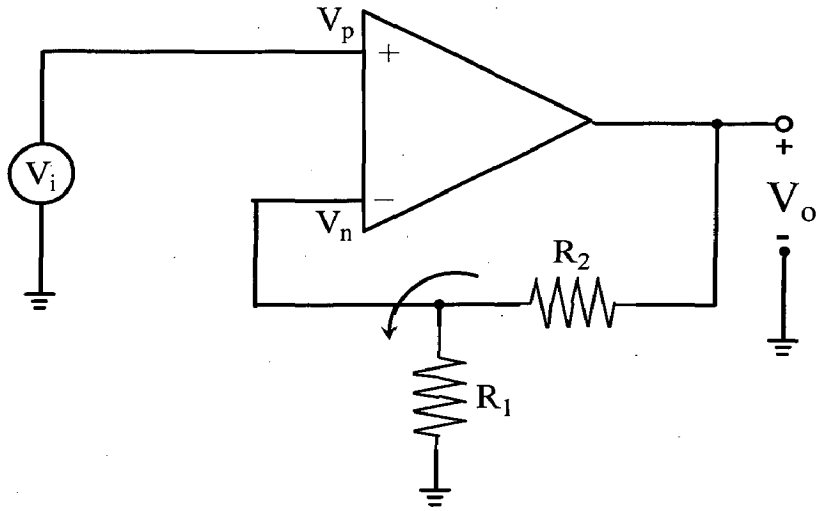

Fig.2.3: Non-Inverting Op Amp

2.4 Inverting OP Amp

The below Figure 2.4 is the inverting op amp circuit. The input terminal, + (V_p), is called the non-inverting input, whereas – (V_n) marks the inverting input. Here the input signal is applied to the inverting terminal via R_1 and the non-inverting terminal is grounded.

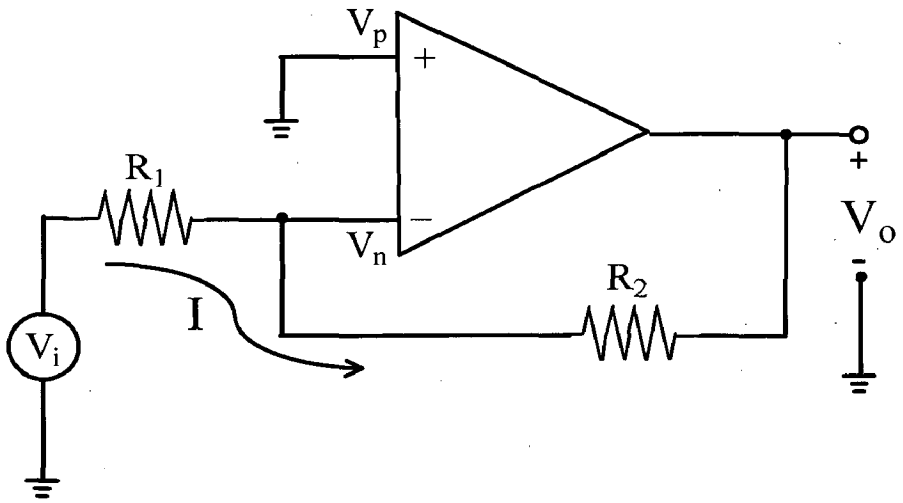

Fig.2. 4: Inverting Amplifier

A relationship between the input voltage V_i, and the output voltageV_0, is required to understand the circuit operation. By applying KVL, KCL and ideal op amp characteristics the relation between V_o and V_i as follows

$$A = \frac{V_o}{V_i} = 1 - \left(\frac{1}{b}\right)\left(\frac{1}{1+\frac{1}{ab}}\right) \tag{12}$$

2.5 Op Amp Specifications

After experimenting with op amp circuits at moderate gained frequency, will be noted very good agreement between actual performance and ideal performance. As gain and/or frequency are increased, certain op amp limitations come into play that effect circuit performance. In theory, with proper understanding of the internal structures and processes used to fabricate an op amp, one can calculate these effects.

2.5.1 Differential Voltage Gain (A_d)

Differential Voltage Gain (A_d), is the ratio of the output voltage change to the input differential voltage change, holding V_{CM} constant. This parameter is closely related to the open loop gain. Differential Voltage Gain measurement takes output loading effects in to account [3].

A_d is a design parameter when precise gain is required. Consider equation (11), where the loop gain of the non-inverting amplifier is given by:

$$A = \frac{Vo}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1+\frac{1}{ab}}\right) \tag{13}$$

$$b = \frac{R_1}{R_1 + R_2} \tag{14}$$

Gain of the circuit is controlled by selecting the appropriate resistor values. The term $1/ab$ in the equation is seen as an error term. Unless a or A_d is large in comparison with $1/b$, it will have an undesired effect on the gain of the circuit.

2.5.2 Unity-Gain Bandwidth and Phase Margin

There are five parameters that relate to the frequency characteristics of the op amp [8]:

- Unity-Gain Bandwidth (ω_c)
- Gain bandwidth product (GBP)
- Phase Margin at unity gain (PM)
- Gain Margin
- Maximum output-swing bandwidth (ω_{OM})

Unity-Gain Bandwidth (ω_c) and gain bandwidth product (GBP) are similar. ω_c specifies the frequency at which Differential Voltage Gain(A_d) of the op amp is 1.

$$\omega_c = \omega \quad \text{at} \quad A_d = 1 \tag{15}$$

GBP specifies the gain-bandwidth product of the op amp in an open loop configuration and the output loaded.

$$GBP = \omega \times A_d \tag{16}$$

Phase Margin at unity gain (PM) is the difference between the amounts of phase shifts a signal experiences through the op amp at unity gain and 180°.

$$PM = 180° - \text{phase shift} \quad \text{at} \quad \omega_c \tag{17}$$

Gain Margin is the difference between unity gain and the gain at 180° phase shift.

$$\text{Gain Margin} = 1 - \text{Gain at } 180° \text{ phase shift}$$

Maximum output-swing bandwidth (ω_{OM}) specifies the bandwidth over which the output is above a specified value.

$$\omega_{OM} = f_{MAX}, \text{ while } V_O > V_{MIN} \tag{18}$$

ω_{OM} is limited by Slew Rate since output becomes Slew Rate limited as the frequency gets higher .If output becomes Slew Rate limited it can not respond quickly enough to maintain the specified output voltage swing.

As noted earlier, it can be seen that A_d falls off with frequency. A_d (And thus ω_c or GBP) is a design issue when precise gain is required in a specific frequency band. Consider below equation (11), where the loop gain of the non-inverting amplifier is given by:

$$A = \frac{Vo}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1+\frac{1}{ab}}\right) \tag{19}$$

Circuit relative stability is specified by Phase Margin (PM) and Gain Margin. If op amp output swings rail-to-rail it will have higher output impedance, a significant phase shift is seen when driving capacitive loads which effects Phase Margin and hence circuit stability. CMOS op amps with rail-to-rail outputs have limited ability to drive capacitive loads and proper care has to be taken to maintain circuit stable under all operating conditions.

2.5.3 Common-Mode Rejection Ratio (CMRR)

Common-Mode Rejection Ratio, CMRR, is defined as the ratio of the differential voltage amplification to the common-mode voltage amplification, A_d / A_C. Ideally CMRR should has infinite value since ideal op amp specifications gives common mode gain as zero.

The common-mode input voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage. The real mechanism at work is $\Delta V_O / \Delta V_{CM}$.

CMRR = $\Delta V_{CM} / \Delta V_O$ (gives a positive number in dB).CMRR, is a DC parameter. CMRR falls off with increasing frequency due to internal capacitances coming into picture at high frequencies.

A common source of common-mode interference voltage is 50 Hz or 60 Hz noise from the AC mains. CMRR of op amp is degraded by external circuit configurations so proper care has to be taken while designing the circuit.

2.5.4 Power Supply Rejection Ratio (PSRR)

Power Supply Rejection Ratio (PSRR) is the ratio of power supply voltage change to output voltage change [7]. The supply voltage variation affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which in turn changes the output voltage. The real mechanism at work is $\Delta V_O/\Delta V_{CC\pm}$.

For a dual supply op amp, PSSR= $\Delta V_{CC\pm}/\Delta V_o$ (to get a positive number in dB). The term $\Delta V_{CC\pm}$ means that the plus and minus power supplies are changed symmetrically. For a single supply op amp, PSSR= $\Delta V_{DD}/\Delta V_O$ (to get a positive number in dB).

PSSR is also produced by mechanism of bias point shift like CMRR. Therefore PSRR is a DC parameter like CMRR; PSSR falls off as the frequency increases.

Switching power supplies can have noise on the order of 20 kHz to 200 kHz and higher. PSSR is almost zero at these high frequencies, so that noise on the power supply results in noise on the output of the op amp.

2.5.5 Slew Rate (SR) at Unity Gain

Slew Rate, SR, is defined as the rate of change in the output voltage caused by a step input [8]. Slew Rate of CMOS op amp has the units of $V/\mu s$. Internal structure of op amp (Fig.3.1) shows that voltage change in the second stage is limited by the charging and

discharging of capacitor C_C. The maximum rate of change occurs when either side of the differential pair is conducting .Since the differential pair is symmetric it causes total current of 2I to flow through the capacitor. This is the major limit to Slew Rate. Essentially, $SR = 2I/C_C$.

The requirement to have current flowing in or out of the input stage to change the voltage out of the second stage requires an error voltage at the input at anytime when the output voltage of an op amp is changing. An error voltage on the order of 120 mV is required for an op amp with a bipolar input to realize full Slew Rate. This can be as high as 1V to 3V for a JFET or MOSFET input.

Capacitor C_C can be used for adjusting Phase Margin to maintain stability of op amp. Reduction of C_C value increases realizable bandwidth and Slew Rate, but ensure that the stability of the circuit is maintained. To increase Slew Rate, the bias currents within the op amp are increased.

2.5.6 Input Common Mode Voltage Range(ICMR)

Normally there is a voltage that is common to the inputs of the op amp. If this common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range, V_{ICMR}, specifies the range over which normal operation is guaranteed.

2.5.7 Maximum Output Voltage Swing

The maximum output voltage, $V_{OM\pm}$, is defined as "the maximum positive or negative peak output voltage that can be obtained without wave form clipping when quiescent DC output voltage is zero".

The maximum out put voltage swing is limited by the following parameters.

- Output impedance of the amplifier.
- Saturation voltage of the output transistors.

- Power supply voltages.

Maximum and minimum output voltage is usually a design issue when dynamic range is lost if the op amp can't drive to the rails. This is the case in single supply systems where the op amp is used to drive the input of an analog-to-digital converter, which is configured for full scale input voltage between ground and the positive rail.

2.5.8 Equivalent Input Noise

The main source of the equivalent input noise is parasitic noise [11]. Noise is measured at the output of an op amp and referenced back to the input, thus, it is called equivalent input noise.

Equivalent input noise specifications are generally expressed in two ways.

- By specifying the spot noise i.e. The equivalent input noise is given as voltage, V_n (or current, I_n) per root hertz at a specific frequency.
- Specifying noise as a peak-to-peak value over a frequency band.

The spectral density of noise in op amps has a 1/f and white noise component. White noise is spectrally flat. Spot noise is inversely proportional to frequency and is usually significant only at low frequencies. Generally spot noise is specified at two frequencies. The first frequency is usually 10 Hz, where the noise exhibits 1/f spectral density. The second frequency is typically 1 kHz, where the noise is spectrally flat. The units of the spot noise is RMS $V/\sqrt{Hz}$ (or RMS $A/\sqrt{Hz}$ for current noise).

2.6 Absolute Maximum Ratings and Recommended Operating Conditions

The following typical parameters for the absolute maximum ratings and the recommended operating conditions of op amps are listed bellow [8]. Performance of op amp will be close to the typical values of specifications when operated under recommended conditions. When stressed beyond the maximum value an unpredictable behavior may cause permanent damage.

Absolute Maximums

- Supply Voltage
- Differential input voltage
- Input voltage range
- Input current
- Output current
- Duration of short-circuit current (at or below 25°C)
- Continuous total power dissipation
- Operating free-air temperature
- Storage temperature
- Lead temperature
- Recommended Operating Conditions
- Common-mode input voltage

Chapter 3 Analysis of the CMOS Based Two-stage Op-Amp

3.1. Introduction

The circuit shown in figure 3.1 is widely used two stage CMOS op-amp in A/D converters [5]. It consists of an input differential stage with active load followed by a common-source stage also with active load. Output buffer is not used in this circuit.

This op-amp architecture has many advantages like

- High open-loop voltage gain
- Rail-to-rail output swing
- Large common-mode input range
- In this architecture, only one frequency compensation capacitor is used.
- Small number of transistors is used in this architecture

The achievable band width of this architecture is reduced by the non dominant pole formed by the load capacitance and the output impedance of the second stage. Feed forward signal path through the compensating capacitor adds the right half plane zero [11, 12]. This, in turn, may severely degrade the phase margin of the amplifier. Compensation resistor R_c is made equal in value to the inverse of the transconductance of the second gain stage, the alternating current (AC) flowing through R_c will cancel the RHP zero as a result of the elimination of the 'feedthrough effect for a particular transconductance.

Design parameters for the two-stage op-amp are as follows:

- The widths and lengths of all transistors, i.e., W_1,……,W_8 and L_1,……,L_8.
- The bias current I_{bias}.
- The value of the compensation capacitor C_c.

There are also a number of parameters that are considered fixed, e.g., the supply voltages V_{DD} and V_{SS}, the capacitive load C_L, and the various process and technology parameters associated with the MOS models.

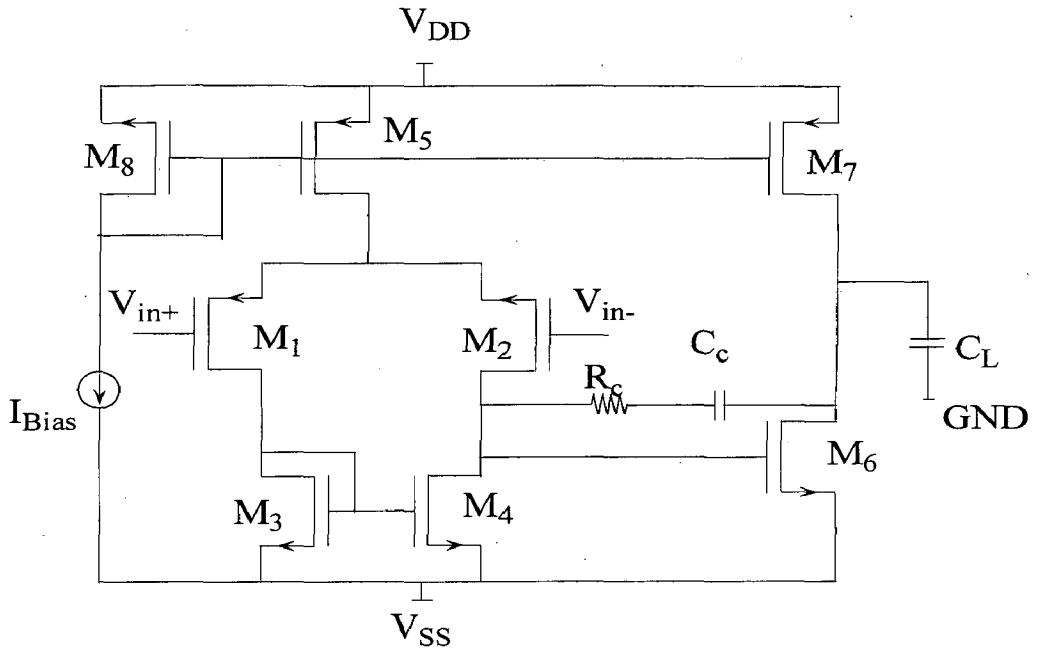

Fig.3.1: Two stage Op-Amp

3.2 Dimension constraints

Basic constraints involving the device dimensions are as follows: symmetry, matching, minimum or maximum dimensions and area limits [5, 6, 11].

3.2.1 Symmetry and Matching

To maintain symmetrical operation of the input differential pair, transistors M_1 and M_2 must be identical and transistors M_3 and M_4 must also be identical. This condition is mathematically stated as

$$W_1 = W_2;\ L_1 = L_2;\ W_3 = W_4;\ L_3 = L_4 \qquad (20)$$

The biasing transistors M_5, M_7, and M_8 must match, i.e., have the same length

$$L_5 = L_7 = L_8 \qquad (21)$$

Equations (20) and (21) effectively reduce the number of variables from 18 to 12. For example, eliminate the variables L_7 and L_8 by substituting L_5 wherever they appear. For clarity, continue the usage of the variables L_7 and L_8 in our discussion; for computational purposes, however, they can be replaced by L_5.

3.2.2 Limits on device sizes

The Lithography limitations and layout rules imposed minimum (and possibly maximum) sizes of the transistors

$L_{min} \leq L_i \leq L_{max}$

$W_{min} \leq W_i \leq W_{max}$ i = 1,.....,8: (22)

These 32 constraints can be expressed as constraints such as $L_{min}/L_1 \leq 1$, etc. since equality constraints are imposed, L_i is taken as constant i.e., 0.8μm.

3.2.3 Area

The die area of the op amp can be approximated as the sum of the constant device spacing, capacitor area and active area of the transistor.

$$A=\alpha_0+\alpha_1 C_c+\alpha_2 \sum_{i=1}^{8} W_i L_i \quad (23)$$

Here α_0, α_1 and α_2 are fixed area, ratio of capacitor area to capacitance and constant respectively. An upper bound should be imposed on the area, i.e., $A \leq A_{max}$, because it should be minimum.

3.2.4 Systematic input offset voltage

The drain voltages of M_3 and M_4 must be equal to reduce input offset voltage. This ensures that the current I_5 is split equally between transistors M_1 and M_2. This happens when the current densities of M_3, M_4, and M_6 are equal, i.e.

$$\frac{W_3/L_3}{W_6/L_6}=\frac{W_4/L_4}{W_6/L_6}=\frac{1}{2}\frac{W_5/L_5}{W_7/L_7} \quad (24)$$

3.3 Bias conditions, signal swing and power constraints

Transistors M_5 and M_7 form a current mirror with transistor M_8. Now calculate the bias currents I_5, and I_7 through transistors M_5 and M_7.

$$I_5 = \frac{W_5 L_8}{L_5 W_8} I_{bias},$$

$$I_7 = \frac{W_7 L_8}{L_7 W_8} I_{bias} \tag{25}$$

The current through transistor M_5 is split equally between transistor M_1 and M_2. This gives

$$I_1 = \frac{I_5}{2} = \frac{W_5 L_8}{2 L_5 W_8} I_{bias} \tag{26}$$

The currents I_1, I_5, and I_7 are used, in order to express other constraints, remembering that these bias currents can simply be eliminated. These constraints are expressed directly in terms of the design variables using equations (25) and (26).

3.3.1 Bias conditions

Assumptions for deriving the bias conditions are as follows [5, 6, 14, 15]

- The input terminals are at the same DC potential, the common-mode input voltage V_{cm}.
- Common-mode input voltage is allowed to range between a minimum value $V_{cm,min}$ and a maximum value $V_{cm,\,max}$.
- Output voltage is allowed to swing between a minimum value $V_{out,\,min}$ and a maximum value $V_{out,\,max}$.

The bias conditions are that each transistor M_1,....., M_8 should remain in saturation for all possible values of the input common-mode voltage and the output voltage.

Transistor M_1: The lowest common-mode input voltage, $V_{cm,\,min}$, imposes the toughest constraint on transistor M_1 remaining in saturation. The condition is

$$\sqrt{\frac{I_1 L_3}{C_{ox} / 2W_3}} \leq V_{cm,min} - V_{ss} - V_{TP} - V_{TN} \tag{27}$$

Transistor M_2: From section 3.2.4 drain voltage of M_1 must be equal to the drain voltage of M_2. Therefore, the condition for M_2 being saturated is same as the condition for M_1

being saturated, i.e., (27). Note that the minimum allowable value of $V_{cm,\ min}$ is determined by M_1 and M_2 entering the linear region.

Transistor M_3: From Fig.3.1: $V_{gd,\ 3} = 0$, transistor M_3 is always in saturation.

Transistor M_4: From section 3.2.4 the drain voltage of M_4 is equal to the drain voltage of M_3. So M_4 is also in saturation region.

Transistor M_5: The highest common-mode input voltage, $V_{cm,\ max,}$ imposes the toughest constraint on transistor M_5 being in saturation. The condition is

$$\sqrt{\frac{I_1 L_1}{C_{ox}/2W_1}} + \sqrt{\frac{I_5 L_5}{C_{ox}/2W_5}} \le V_{dd} - V_{cm,\max} + V_{TP} \tag{28}$$

Thus, the maximum allowable value of $V_{cm,\ max}$ is determined by M_5 entering the linear region.

Transistor M_6: The most stringent condition occurs when the output voltage is at its minimum value $V_{out,\ min}$

$$\sqrt{\frac{I_7 L_6}{C_{ox}/2W_6}} \le V_{out,\min} - V_{ss} \tag{29}$$

Transistor M_7: For M_7, the most stringent condition occurs when the output voltage is at its maximum value $V_{out,\ max}$

$$\sqrt{\frac{I_7 L_7}{C_{ox}/2W_7}} \le V_{dd} - V_{out,\max} \tag{30}$$

Transistor M_8: From Fig.3.1 $V_{gd,\ 8} = 0$, transistor M_8 is always in saturation.

In summary, the requirement that all transistors remain in saturation for all values of common-mode input voltage between $V_{cm,\ min}$ and $V_{cm,\ max}$, and all values of output

voltage between $V_{out,\,min}$ and $V_{out,\,max}$, is given by the four inequalities (27), (28), (29), and (30).

3.3.2 Gate overdrive

It is sometimes desirable to operate the transistors with a minimum gate drive voltage [5]. This ensures that they operate away from the sub threshold region, and also improves matching between transistors. For any given transistor this constraint can be expressed as

$$V_{gs} - V_T = \sqrt{\frac{I_D L_6}{C_{ox}/2W}} \geq V_{ovrerdrive,min} \qquad (31)$$

The typical overdrive voltage i.e. ΔV_o =200mV.

3.3.3 Quiescent power

From figure 3.1, the quiescent power of the op-amp is given by

$P = (V_{dd} - V_{ss})\,(I_{bias} + I_5 + I_7)$ (32)

Which is an function of design parameters.

3.4. Small signal transfer function [5]

Since the symmetry, matching, and bias constraints are satisfied, and consider the small signal transfer function H from a differential input source to the output source [5, 6, 14]. A standard small signal model is used for the transistors to derive the transfer function H. Small signal model is described in Appendix. The standard value of the compensation resistor is used, i.e.,

$Rc = 1/g_{m6}$ (33)

The transfer function can be well approximated by a four pole form

$H(s) = A_v/((1 + s/p_1)(1 + s/p_2)(1 + s/p_3)(1 + s/p_4))$ (34)

Here

A_v is the open-loop voltage gain,

$-p_1$ is the dominant pole,

$-p_2$ is the output pole,

$-p_3$ is the mirror pole,

$-p_4$ is the pole arising from the compensation circuit

In order to simplify the discussion –p1, …,-p4 are referred as p1,…,p4 .

Expressions for the gain and poles are as follows.

The open-loop voltage gain is

$$A_v=\left(\frac{g_{m2}}{g_{o2}+g_{o4}}\right)\left(\frac{g_{m6}}{g_{o6}+g_{o7}}\right)$$

$$=\left(\frac{2}{(\lambda_n+\lambda_p)^2}\right)\sqrt{\mu_n C_{ox}\mu_p C_{ox}\left(\frac{W_2 W_6}{L_2 L_6 I_1 I_7}\right)} \qquad (35)$$

The dominant pole is accurately given by

$$p_1 = g_{m1}/(A_v C_c) \qquad (36)$$

Since A_v and g_{m1} will have fixed value, C_c is a design variable.

The output pole p_2 is given by

$$p_2 = g_{m6}C_c/(C_1C_c + C_1C_{TL} + C_cC_{TL}) \qquad (37)$$

where C_1, the capacitance at the gate of M_6 , can be expressed as

$$C_1 = C_{gs6} + C_{db2} + C_{db4} + C_{gd2} + C_{gd4} \qquad (38)$$

and C_{TL}, the total capacitance at the output node, can be expressed as

$$C_{TL} = C_L + C_{db6} + C_{db7} + C_{gd6} + C_{gd7} \qquad (39)$$

The meanings of these parameters, and their dependence on the design variables, are given in Appendix.

The mirror pole p_3 is given by

$$p_3 = g_{m3}/C_2 \qquad (40)$$

Where C_2, the capacitance at the gate of M_3 , can be expressed as

$$C_2 = C_{gs3} + C_{gs4} + C_{db1} + C_{db3} + C_{gd1} \qquad (41)$$

The compensation pole p_4 is

$$p_4 = g_{m6}/C_1 \qquad (42)$$

3.4.1 Open-loop gain constraints

Since design constraints impose lower bound on the open loop gain, which is expressed as

$$A_{min} \leq A_v \tag{43}$$

Where A_{min} is given as lower limit on acceptable open-loop gain.

3.4.2 Minimum gain at a frequency

The magnitude squared of the transfer function at a frequency ω_o is given by

$$|H(j\omega_0)|^2 = \frac{A_v^{\,2}}{\prod_{i=1}^{4}(1+\omega_0^{\,2}/p_i^{\,2})} \tag{44}$$

Where p_i are the poles of two stage op amp and A_v is the gain of two stage op amp. Minimum gain a, which occur at a frequency ω_o, must satisfy the following constraint

$$|H(j\omega_0)| \geq a \tag{45}$$

It can also be written as, $a^2/|H(j\omega_0)|^2 \leq 1$ (46)

The transfer function magnitude $|H(j\omega_0)|$ decreases as ω increases (since it has only poles), so $|H(j\omega_0)| \geq a$, is equivalent to

$$\Rightarrow |H(j\omega_0)| \geq a \text{ for } \omega < \omega_o \tag{47}$$

As explained below this allows us to specify a minimum bandwidth or crossover frequency.

3.4.3 3dB bandwidth

The 3dB bandwidth w_{3dB} is the frequency at which the gain drops 3dB below the DC open-loop gain, i.e. $|H(j\omega_{3dB})| = A_v/\sqrt{2}$. Mathematically this can be expressed as,

$$A_v/|H(j\omega_{3dB})|^2 \leq 2 \tag{48}$$

In almost all designs p_1 will be the dominant pole. So 3dB bandwidth can be given by

$$\omega_{3dB} = p_1 = g_{m1}/(A_v C_c) \tag{49}$$

By calculation of ω_{3dB} value theoretically from the above equation gives extremely accurate value.

3.4.4 Dominant pole conditions

In order to operate the amplifier correctly, it must ensure that the dominant pole i.e., p_1 must be smaller than p_2, p_3, p_4 in terms of decades [5]. These conditions can be expressed as

$$p_1/p_2 \leq 0.1; p_1/p_3 \leq 0.1; p_1/p_4 \leq 0.1; \quad (50)$$

Where one decade is selected arbitrarily, i.e., a factor of 10 in frequency, as the condition for dominance. In fact these dominant pole conditions usually do not need to be included explicitly since the conditions for Phase Margin are generally stricter. It is a common practice to impose a minimum ratio between dominant and non-dominant poles.

3.4.4 Unity-Gain Bandwidth and Phase Margin

Unity Gain bandwidth ω_c can be defined as the frequency at which $|H(j\omega_c)| = 1$. The Phase Margin is defined as the phase of the transfer function at the Unity- Gain Bandwidth [5]:

$$PM = \pi - \angle H(j\omega_c) = \pi - \sum_{i=1}^{4} \arctan(\omega_c / p_i) \quad (51)$$

A Phase Margin constraint specifies a lower bound on the Phase Margin, typically between 30°-60°.

Normally Unity-Gain Bandwidth is expected to exceed a given minimum frequency, i.e.,

$$\omega_{c} \geq \omega_{c,\min} \quad (52)$$

An approximate expression for the Unity-Gain Bandwidth can be derived from dominant pole condition. If the parasitic poles p_2, p_3, and p_4 are at least a bit (say, an octave) above the Unity-Gain Bandwidth, then the Unity-Gain Bandwidth can be approximated as the open-loop gain times the 3dB bandwidth, i.e.,

$$\omega_{c,approx} = \frac{g_{m1}}{C_c} \quad (53)$$

By using this approximate expression for the Unity-Gain Bandwidth, Unity-Gain Bandwidth can be fixed at a desired value. The approximation (53) overestimates the actual Unity-Gain Bandwidth, since it ignores the decrease in gain due to the parasitic poles.

Assuming the open-loop gain exceeds 10 or so, the phase contributed by the dominant pole at the Unity-Gain Bandwidth, i.e., arc tan(ω_c/p_i), will be very nearly 90^0. Therefore the Phase Margin constraint can be expressed as

$$\sum_{i=2}^{4} \arctan(\omega_c / p_i) \leq \pi/2 - PM \qquad (54)$$

i.e., the non dominant poles cannot contribute more than 90^0-PM total phase shift.

Unity-Gain Bandwidth can be approximated by $\omega_{c,approx}$. For arc tan (x) less than 25^0 arc tan (x) $\approx$ x, which is quite accurate .Thus, assuming that each of the parasitic poles contributes no more than about 25^0 of phase shift, the Phase Margin constraint can be expressed as

$$\sum_{i=2}^{4} (\omega_{c,approx} / p_i) \leq \pi/2 - PM_{\min} \qquad (55)$$

The approximation error involved here is almost always very small since none of the non-dominant poles is too near ω_c [5].This ensures that the approximation of the phase contributed by non-dominant poles is good.

3.5. Some important constraints

In this section other important design constraints imposed by Slew Rate, CMRR and PSRR are considered [5].

3.5.1 Slew Rate

The Slew Rate can be expressed as

$$SR = \min \{2I_1/C_c, I_7/(C_c + C_{TL})\} \qquad (56)$$

In order to ensure a minimum Slew Rate SR_{min} one can impose the two constraints

$$\frac{C_c}{2I_1} \leq \frac{1}{SR_{min}} \quad ,$$

$$\frac{C_c + C_{TL}}{I_7} \leq \frac{1}{SR_{min}} \tag{57}$$

3.5.2 Common Mode Rejection Ratio

The Common Mode Rejection Ratio (CMRR) can be approximated as

$$CMRR = \frac{2g_{m1}g_{m3}}{(g_{o3} + g_{o1})g_{o5}} = \frac{2C_{ox}}{(\lambda_n + \lambda_p)\lambda_p}\sqrt{\mu_n\mu_p \frac{W_1W_3}{L_1L_3I_5^2}} \tag{58}$$

The CMRR can be calculated theoretically in terms of the device parameters. Minimum CMRR value can be achieved by proper selection of device dimensions.

3.5.3 Power Supply Rejection Ratio

The low-frequency positive Power Supply Rejection Ratio is given by

$$PSRR = \frac{2g_{m2}g_{m3}g_{m6}}{(g_{o2} + g_{o4})(2g_{m3}3g_{o7} - g_{m6}g_{o5})} \tag{59}$$

The PSRR can be calculated theoretically in terms of the device parameters. Minimum PSRR value can be achieved by proper selection of device dimensions.

4.1 Op-amp Specifications

Specifications of the two stage CMOS op amp used in Sample and Hold circuit of ADC are given below [5, 16]. Supply voltage V_{DD}=5v, V_{SS}=0v.

Constraint	Specification
Active length	≥ 0.8μm
Device width	≥ 2μm
Area	≤10000 μm^2
Common Mode Input Voltage	fixed at V_{DD} /2
O/P voltage range	[0.1- 0.9]V_{DD}
Quiescent power	≤ 5mw
Phase Margin	≥60°
Slew Rate	≥ 10 V/μs
Open Loop Gain	≥ 80dB
Unity Gain BW	≥10 MHz
CMRR	≥ 60 dB
PSRR	≥ 80 dB

Table.4.1: Specifications of the op amp

4.2 Constraints considered

The Quiescent power is constant as the power supply is constant.

$\therefore$ P= 5 mw

From the discussion in 3.4.5, Phase Margin is assumed as maximum.

$\therefore$ PM= 60°

In this calculation, the common mode input applied voltage is constant.

$\therefore V_{cm\ min} = V_{cm\ max} = V_{dd}/2$

A 0.8μm technology is used, so the device length of all the transistors is equal to 0.8μm and value of the bias transistor is taken as the minimum device parameter.

$$\therefore L_{min} = L_8 = 0.8\mu m$$

$$\therefore W_{min} = W_8 = 2\ \mu m$$

Capacitor load is taken as 3.5pF.

$$C_L = 3.5\ pF$$

Typical values of the device parameters $\mu_p C_{ox}$,$\mu_n C_{ox}$ are considered.

$\mu_p C_{ox} = 16\times 10^{-6}\ \mu A/V^2$

$\mu_n C_{ox} = 25\times 10^{-6}\ \mu A/V^2$

4.3 Calculations

4.3.1 Bias current calculation [5]

From Fig.3.1, it is observed that current flowing through M_8 and I_{bias} are equal and I_8 can be expressed in terms of device parameters.

$$\Rightarrow I_{bias} = I_8$$

$$I_{bias} = 1/2\ \mu_p C_{ox} (W/L)_8 (V_{gs8} - V_{dd} - V_{TP})^2$$

and

$$V_{gs8} = V_{ds8} = V_{dd}$$

Therefore

$$\Rightarrow I_{bias} = 1/2 \times 16 \times 10^{-6} \times ((2\times 10^{-6})/(0.8\times 10^{-6})) \times (0-0.7)^2$$

$$\Rightarrow I_{bias} \approx 10\times 10^{-6}\ A$$

4.3.2 Device widths calculation [5]

Quiescent power is 5mW and I_{bias} is 10μA ,V_{DD} =5V,V_{SS}=0V

Substituting these values in equation (32)

$$\Rightarrow P = (V_{DD} - V_{SS})(I_{bias} + I_5 + I_7)$$

$$\Rightarrow 5\times 10^{-3} = (5-0)(10\times 10^{-6} + I_5 + I_7)$$

$\Rightarrow I_5+I_7 = 99\times10^{-5}\,A$

$\Rightarrow W_5+W_7 = 0.1978\times10^{-3}$ ($\because L_5=L_7$)

By solving the above expression and equation (24) we get

$W_5 = 64.6\ \mu m$

$W_7 = 132.6\ \mu m$

$(\because \frac{W_5}{2W_7} = \frac{W_1}{W_3} = \frac{W_4}{W_6} = x)$

W_5, W_7, W_8 and I_{bias} values are substituted in the equation (25) ,to obtain I_5 and I_7

$$I_5 = \frac{W_5 L_8}{L_5 W_8} I_{bais}$$

$$= \frac{64.6}{2}\times\frac{0.8}{2}\times10\times10^{-6}$$

$$=323\mu A$$

$$I_7 = \frac{W_7}{L_7}\times\frac{L_8}{W_8}\times I_{bias}$$

$$=\frac{132.6}{0.8}\times\frac{0.8}{2}\times10\times10^{-6}$$

$$=663\mu A$$

From equation (26), it is known that currents I_1 , I_2 ,I_3 and I_4 are equal and their value is equal to half of I_5 . Substitute the value of I_5 in equation (26), to obtain I_1, I_2 ,I_3 and I_4.

$$\Rightarrow I_1 = I_2 = I_3 = I_4 = \frac{I_5}{2}$$

$$=323/2\ \mu A$$

$$= 161.5\mu A$$

The current I_3 is also expressed in terms of device parameters

$$\Rightarrow I_3 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_3}{L_3}\right)(V_{GS3} - V_{TN})^2$$

By substituting values of I_3 and device parameters in the above expression ,we get

$$\Rightarrow \frac{323\times10^{-6}}{2} = \frac{1}{2}\times 25\times10^{-6}\left(\frac{W_3}{0.8\times10^{-6}}\right)(0.97-0.7)^2$$

$$\Rightarrow W_3 = 143.55\ \mu m$$

From equation (20),

$$W_4 = W_3$$

$$\Rightarrow W_4 = 143.55\mu m$$

Rearrange equation (26), to get W_6 in terms of W_7, W_5 and W_8 .

$$W_6 = \frac{2W_7W_8}{W_5}$$

$$= 588.8\ \mu m$$

From biasing condition of M_6 and equation (31) it can be expressed as.

$$V_{G6} = V_{TN} + \Delta V_0$$

where ΔV_0 is over drive voltage and is equal to 0.2V

$$V_{G6} = 0.7+0.2$$

$$= 0.9\ V$$

From Fig.3.1 ,

$$V_{dm1} = V_{dm2} = V_{dm3} = V_{dm4} = V_{dm6}$$

But

$$V_{dm6} = V_{dd}/2$$

The current I_1 expressed in terms of device parameters is

$$I_1 = I_s/2$$

$$= \frac{1}{2}\mu_p C_{ox}\left(\frac{W_1}{L_1}\right)(V_{GS1} - V_{TP})^2$$

From Fig.3.1

$$V_{GS1} = V_{in+} - V_{ds}$$

$$= 0.97 \text{ V}$$

Substituting in I_1

$$\Rightarrow \frac{323\times10^{-6}}{2} = \frac{1}{2}16\times10^{-6}\left(\frac{W_1}{0.8\times10^{-6}}\right)(0.97-0.7)^2$$

$$W_1 = 238.8\mu\text{m}$$

From equation (20),

$$\Rightarrow W_1 = W_2$$

$$= 238.8\mu\text{m}$$

Calculation of all parasitic capacitance

$$\Rightarrow C_{TL} = C_1 + C_{db6} + C_{dd7} + C_{gd6} + C_{gd7} \approx 10.6\text{pF}$$

4.3.3 Slew Rate calculation

From equation (56), calculate the Slew Rate by substituting the values of C_{TL}, C_6, I_1 and I_7 [5] .

$$SR = \min\{2I_1/C_6, I_7/(C_6+C_{TL})\}$$

$$= \min\left\{\frac{2\times323\times10^{-6}}{2\times3.5\times10^{-12}}, \frac{663\times10^{-6}}{(3.5+10.6)\times10^{-12}}\right\}$$

$$= \min\{92.5, 88\}$$

$$= 88 \text{ V}/\mu\text{s}$$

4.3.4 Transconductances calculation of each device

For analysis of the op amp small signal model, the transconductance of each and every device is calculated [5]. The transconductance can be expressed in terms of device parameters, which are already calculated. By substitution of those values, the transconductance parameters of the op amp can be obtained.

$$g_{m6} = \sqrt{2\mu_n C_{ox} I_6 \frac{W_6}{L_6}}$$

$$= \sqrt{(2\times10^{-6}\times25\times10^{-6}\times115(\frac{588.8}{0.8}))}$$

$$= 2.0571 \times 10^{-3}\,\text{mho}$$

$$g_{m7} = \sqrt{2\mu_p C_{ox} I_7 \frac{W_7}{L_7}}$$

$$= \sqrt{(2\times16\times10^{-6}\times663\times10^{-6}\times(\frac{132.8}{0.8}))}$$

$$= 1.8752 \times 10^{-3}\,\text{mho}$$

$$g_{m5} = \sqrt{2\mu_p C_{ox} I_5 \frac{W_5}{L_5}}$$

$$= \sqrt{(2\times16\times10^{-6}\times323\times10^{-6}\times(\frac{64.6}{0.8}))}$$

$$= 0.914 \times 10^{-3}\ \text{mho}$$

$g_{m1} = g_{m2}$

$$= \sqrt{2\mu_p C_{ox} I_1 \frac{W_1}{L_1}}$$

$$= \sqrt{(2 \times 16 \times 10^{-6} \times 323 \times 10^{-6} \times (\frac{232.8}{2 \times 0.8}))}$$

$$= 1.034 \times 10^{-3} \text{ mho}$$

4.3.5 Unity-Gain Bandwidth calculation

From equation (53), calculate Unity-Gain Bandwidth ω_c by substituting g_{m1} and C_c [5].

$$\omega_{c\ approx} = g_{m1}/C_C$$

$$= 91428537.4 \text{Hz}$$

Typical values of the device parameters λ_n and λ_p are assumed as

$$\lambda_n = 15 \times 10^{-5} \quad V^{-1}$$

$$\lambda_p = 7 \times 10^{-5} \quad V^{-1}$$

4.3.6 Open loop gain calculation

From the small signal analysis the open-loop voltage gain is given by equation (35). Substituting all the calculated parameters and device parameters in this equation (35) the open-loop voltage gain is obtained [5, 17].

$$A_v = \left(\frac{g_{m2}}{g_{o2} + g_{o4}}\right)\left(\frac{g_{m6}}{g_{o6} + g_{o7}}\right)$$

$$= (\frac{2}{(\lambda_n + \lambda_p)^2}) \sqrt{\mu_n C_{ox} \mu_p C_{ox} (\frac{W_2 W_6}{L_2 L_6 I_1 I_7})}$$

$$= (\frac{2}{(15+7)^2 \times 10^{-10}}) \sqrt{(16 \times 10^{-6} \times 25 \times 10^{-6} (\frac{232.8 \times 588.8}{0.8 \times 0.8 \times \frac{323}{2} \times 10^{-6} \times 663 \times 10^{-6}}))}$$

$$= 90.6 \text{ dB}$$

4.3.7 CMRR calculation

CMRR value of the op amp is calculated by substituting all numerical values of the variables [5].

$$CMRR = \left(\frac{2g_{m1}g_{m3}}{(g_{o3} + g_{o5})g_{o5}} \right)$$

$$= \left(\frac{2C_{ox}}{(\lambda_n + \lambda_p)\lambda_p} \right) \sqrt{\mu_n \mu_p \left(\frac{W_1 W_3}{L_1 L_3 I_5^2} \right)}$$

$$= \left(\frac{2}{22 \times 7 \times 10^{-10}}\right) \sqrt{(16 \times 10^{-6} \times 25 \times 10^{-6} \left(\frac{232.8 \times 143.6}{0.8 \times 0.8 \times 323^2 \times 10^{-6} \times 10^{-6}}\right))}$$

$$= 92.6 \text{ dB}$$

4.3.8 PSRR calculation

Calculate PSRR value of the op amp by substituting all the numerical values of transconductance parameters [5].

$$PSRR = \frac{2g_{m2}g_{m3}g_{m6}}{(g_{o2} + g_{o4})(2g_{m3}3g_{o7} - g_{m6}g_{o5})}$$

Where

$g_{o2} = \lambda_n I_5/2$

$g_{o4} = \lambda_p I_5/2$

$g_{o5} = \lambda_p I_5$

$g_{o7} = \lambda_p I_7$

From the values of transconductances, currents and device parameters, using equation (59), PSRR value is obtained as 105.2593 dB.

4.4 Summary of the theoretical calculations

The Summary of theoretical calculated constraints values of the op-amp at 0.8 μm node is tabulated in table 4.2.

Constraint	Theoretical calculated value
$W_1 = W_2$	238.8μm
$W_3 = W_4$	143.5μm
W_5	64.6μm
W_6	588.8μm
W_7	132.6μm
W_8	2.0μm
$L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = L_7 = L_8$	0.8μm
I_{bias}	10×10^{-6}
Unity Gain Band width	91.4MHz
Open loop gain	90.6 dB
CMRR	90.2dB
PSRR	105.2593 dB
SR	88 V/μs

Table.4.2: Summary of theoretical calculations

These results are obtained from T-spice net list (at 0.8μm technology node) .Here we have taken the dual supply voltage for figure 3.1, with the supply voltages as 5v and 0v. The various simulated results that are obtained from the net list are discussed in the following sections. These results are matched with the theoretical results.

5.1. Differential Voltage Gain, UGB, and Phase Margin

The open loop gain(db) and UGB of the amplifier plots are shown in Fig5.1 .

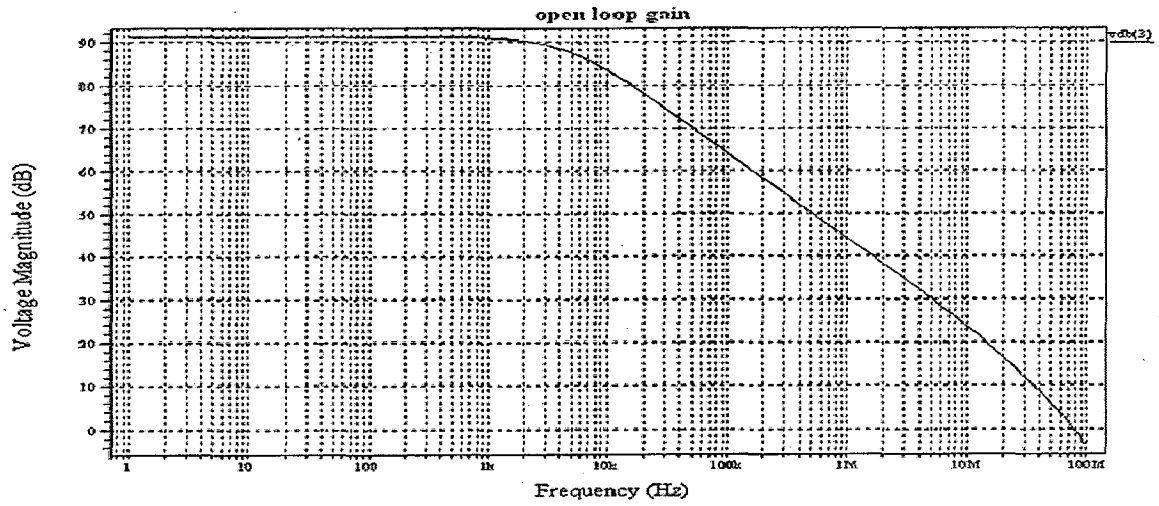

Fig 5.1: Open loop gain (dB) and UGB of the amplifier

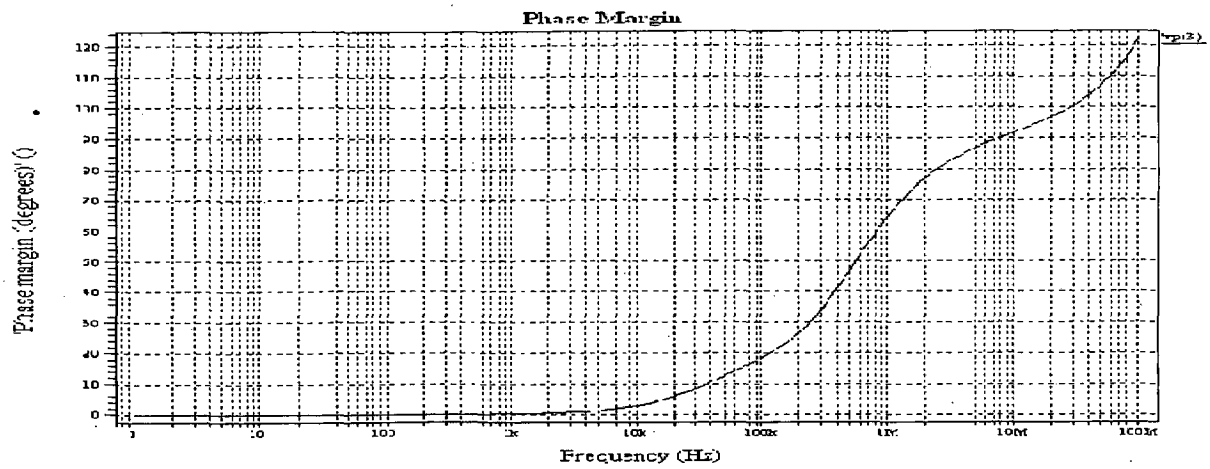

Fig 5.2: open loop phase (deg)

By plotting the gain in dB, the Unity Gain Bandwidth (UGB) is determined [13, 15]. By referring to fig 5.1 and 5.2, values of the Unity Gain Bandwidth, Differential Gain and Phase Margin are:

The Unity Gain Bandwidth 80.23MHz

The Differential Gain is 90.5dB.

Phase Margin = 180-117=63 degrees for 3.5pf capacitor load

5.2. ICMR

Unity-gain configuration is useful for measuring or simulating the input CMR. Fig 5.3 and 5.4 shows the ICMR characteristics of the op amp [13, 15]. The linear part of the transfer curve (slope unity) corresponding to the input common-mode voltage range. The initial jump in the voltage sweep from negative values of V_{in} to positive values is due to the turn-on of bias transistor of differential amplifier. Fig 5.4 is plotted between simulated values of the current through the bias transistor and input voltage.

By referring fig 5.3 and 5.4 the simulated value of ICMR is:

ICMR characteristics of the op amp: -1.80 t0 2.4v

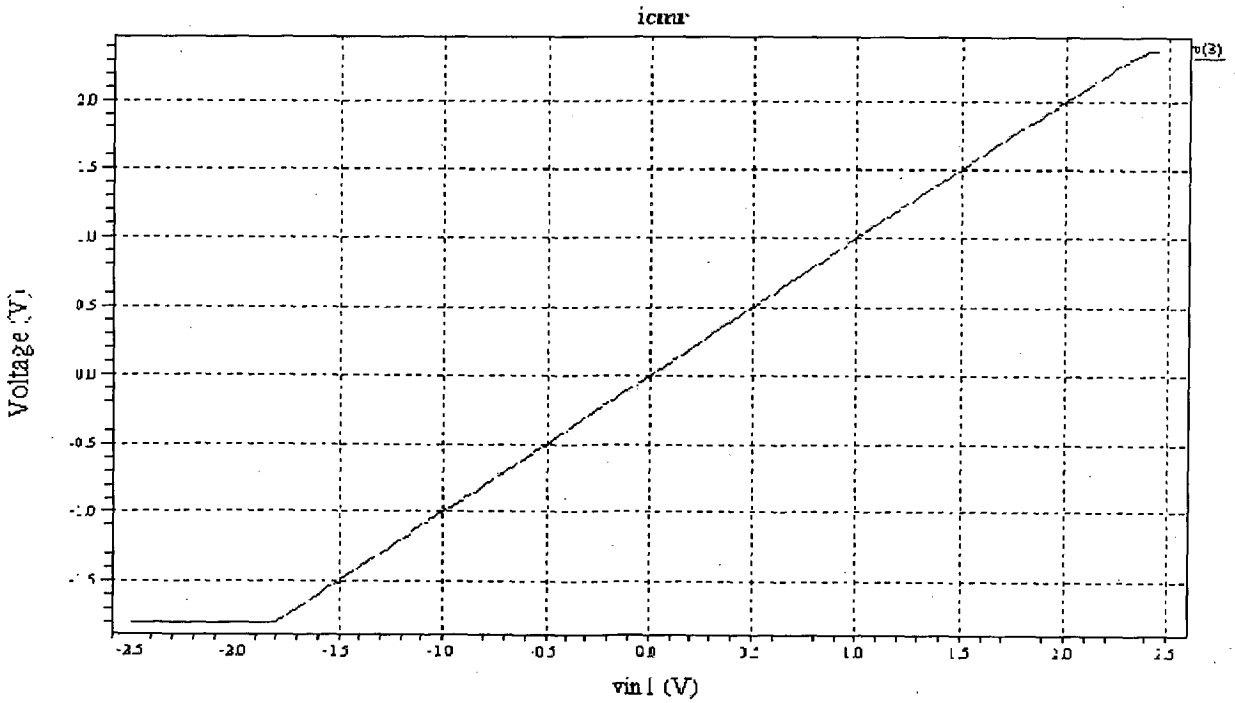

Fig 5.3: ICMR characteristics of op amp(1)

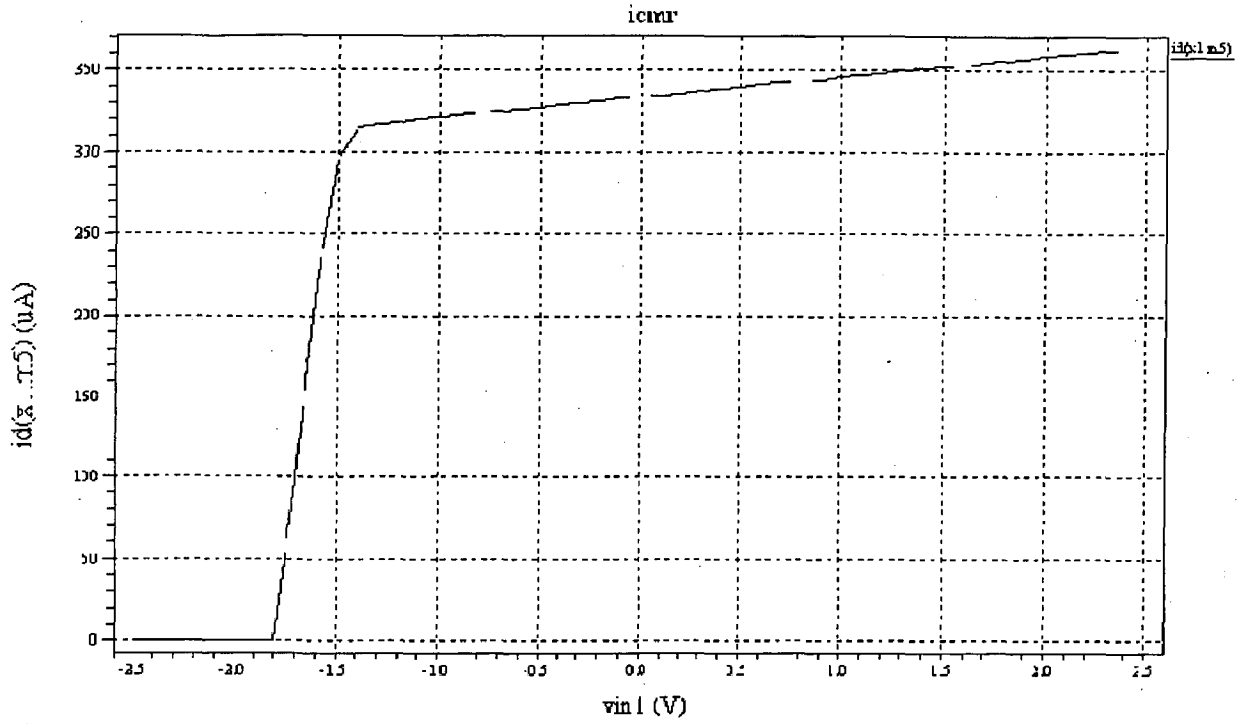

Fig 5.4: ICMR characteristics of op amp(2)

5.3. Output Swing

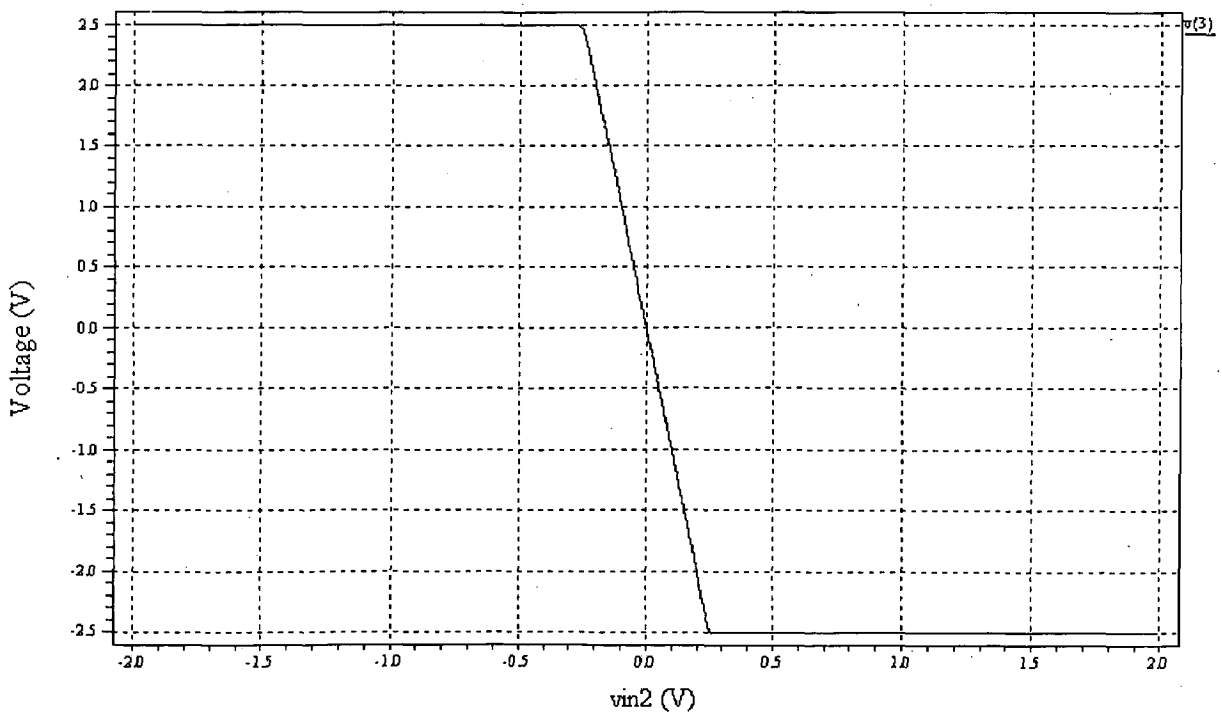

Fig 5.5: Output swing of the op-amp

In the unity gain configuration, the linearity of the transfer curve is limited by the CMR. Using the configuration of higher gain, the linear region of the transfer curve can be used to obtain the output-voltage swing of the amplifier. The results of the simulation are displayed in figure 5.5.

From the fig 5.5 the Output swing of the op amp is -2.5V to 2.5V

5.4. CMRR

Similar to calculation of differential gain, connect common signal to the both inputs and measure the gain. It is common mode gain.CMRR [13, 15] is the ratio of differential gain to common mode gain. If they are in dB subtract common mode gain from differential gain to get the CMRR.

By referring fig 5.1 and 5.6 the simulated values of the differential gain and commoan mode gain are:

Differential gain is 90.5dB

Common mode gain is -37dB

CMRR=127.5dB

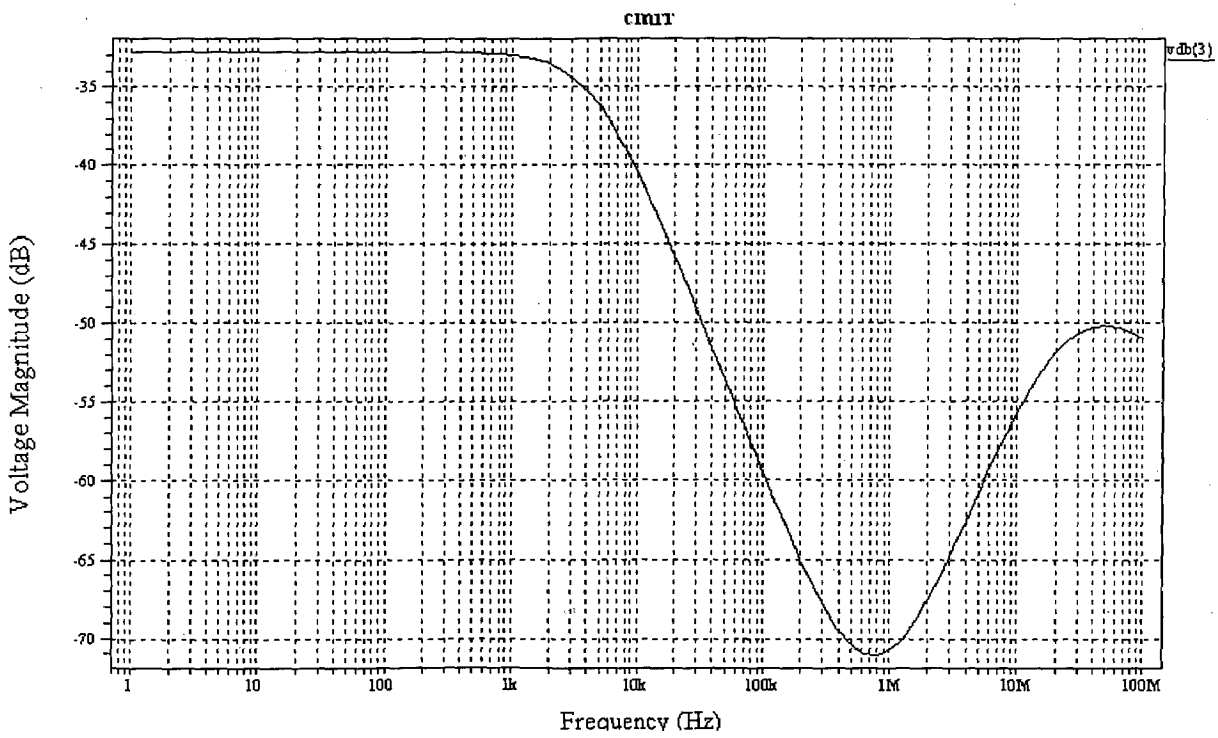

Fig 5.6: Common mode gain as a function of frequency for the amplifier

5.5. PSRR

PSRR is defined as the ratio of the differential gain A_v to the gain from the power supply ripple at the output with the differential input set to zero (A_d) [13, 15]. PSRR = A_v (V_{DD}=0)/A_d (V_{in}=0) .To calculate this, A_v and A_d are calculated separately.

By referring fig 5.1 and fig 5.7 simulated values of open loop gain is 90.6 dB and gain for power ripple is -73.0dB

Gain for signal = 90.5 dB

Gain for power supply noise = -73.0dB

PSRR= 90.5-(-73.0) =163.5dB

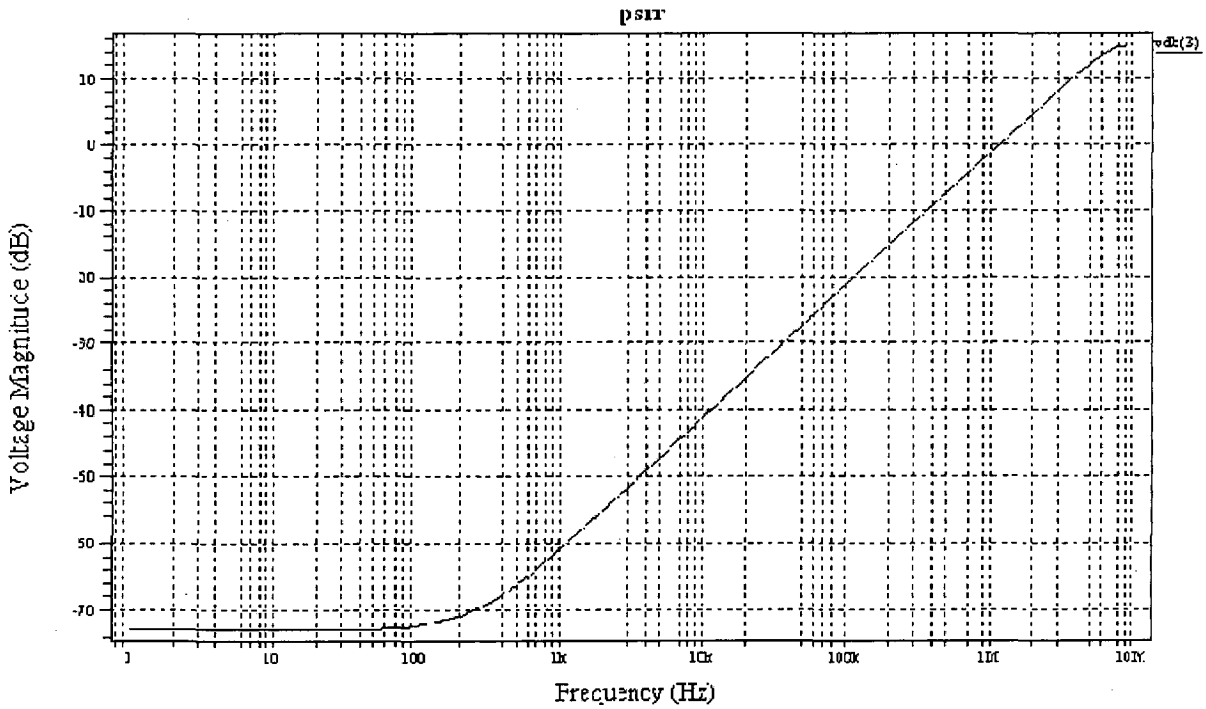

Fig 5.7: gain from power supply ripple to the output

5.6. Slew Rate (SR)

The fig 5.8 has been plotted between output voltage (V) of op-amp and time (ms) through simulation.

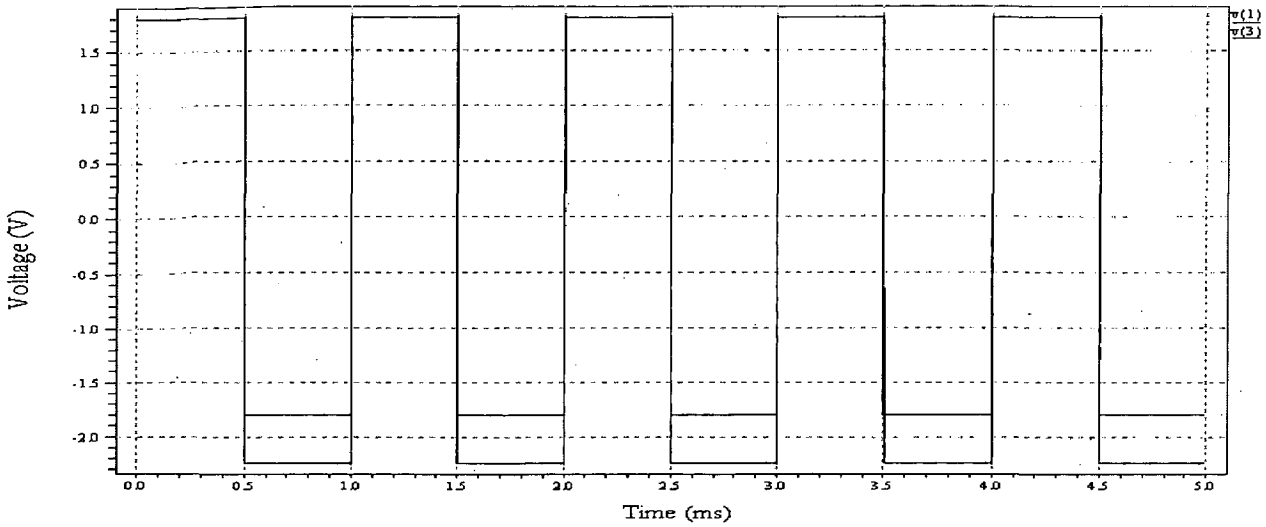

Fig 5.8: Slew Rate characteristics

By referring to fig 5.8 the simulated values of Slew Rate are:

Slew Rate for rising edge is 86.2V/us

Slew Rate for falling edge is 87.6V/us

Average Slew Rate is 86.9V/us

If the applied step is small, then output should not slew and the transient response will be a linear response. If the input step magnitude is sufficiently large, the op amp will slew by virtue of not having enough current to charge or discharge the load capacitances. Slew Rate is determined from the slope of the output waveform during the rise or fall of the output [13, 15]. The output loading of the op amp should be present during the Slew Rate measurements. The unity-gain configuration places the severest requirements on stability and Slew Rate because the feedback is the largest, resulting in the largest values of loop gain, and should be used as a worst-case measurement.

5.7 Summary of Simulation Results

The Summary of Simulation Results of the op-amp at 0.8 μm node is tabulated in table 5.1.

CHARECTERSTICS	REQUIRED SPECIFICATION	OBTAINED RESULTS
Gain(dB)	>80	90.5
Phase Margin(3.5pf)	>60	63
ICMR(V)	-1 to 2	-1.8 to 2.4
Output Swing(v)	>3	5
CMRR(dB)	>60	127.5
Slew Rate(v/us)	>10	86.9
UGB Product(MHz)	>10	80
PSRR(dB)	>80	163.3

Table 5.1: Summary of Simulation Results

Chapter 6 Conclusion and Future work

This work explains automated sizing of op-amp component values directly from specifications. This implies that the circuit designer can spend more time doing real design. The component values obtained after applying all the constraints are used for theoretical computation of various op-amp design parameters. The theoretically predicted values are validated against spice simulations at 0.8um technology node.

This method can be used to do full custom design for each op-amp in complex mixed signal integrated circuit. Each amplifier is obtained for a given load capacitance and required bandwidth and closed loop gain. Other op-amp configurations can also be analyzed and can be designed to meet specific goals. Layout of the amplifier can also be drawn and parametric analysis can be done to calculate the parasitic capacitances since they can degrade the performance of the amplifier.

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Appendix A MOSFET MODELS

MOSFET large and small-signal models are described in this section, which are effectively used in our calculation. The model, which is referred as GP0, is essentially the standard long-channel square law. This model can be inadequate for short-channel transistors also.

1) Large-Signal Models: For the intended operation of the op-amp requires all transistors to be in saturation. For an NMOS transistor this means

$$V_{DS} = V_{GS} - V_{TN} \tag{1}$$

When the NMOS transistor is saturated, i.e., (1) holds, the drain current is

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TN})^2(1 + \lambda_n V_{DS}) \tag{2}$$

Where

L Transistor channel length;

W Transistor width;

μ_n Electron mobility;

C_{ox} Oxide capacitance per unit area;

V_{TN} NMOS threshold voltage;

λ_n Channel-length modulation parameter.

In developing our bias constraints, the simplified large-signal equation is used.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TN})^2 \tag{3}$$

i.e., neglect the channel-length modulation. This introduces only a small error.

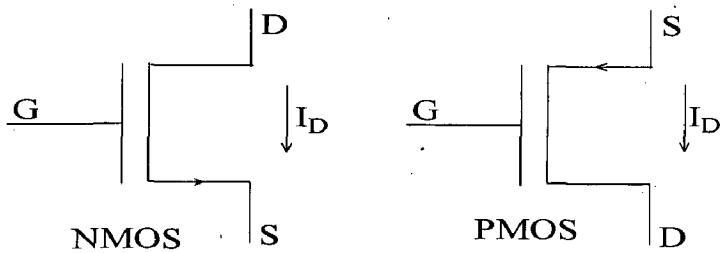

Fig.1. Transistorsymbols.

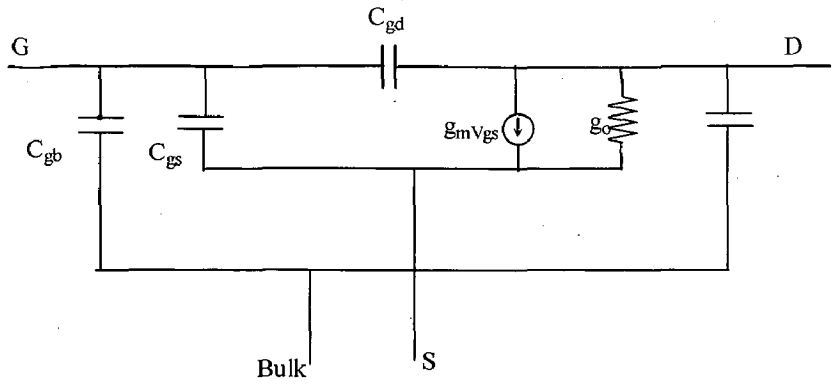

Fig. 2. Small signal model for a MOS FET.

The saturation condition for a PMOS transistor is

$$V_{DS} \leq V_{GS} - V_{TP} \tag{4}$$

The drain current is given by

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TP})^2(1 + \lambda_p V_{DS}) \tag{5}$$

Where

μ_p Hole mobility;

V_{TP} PMOS threshold voltage;

λ_p Channel-length modulation parameter.

Here too, neglect the channel modulation effects and use the simplified expression

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TP})^2 \tag{6}$$

2 Small-Signal Models: Fig. 2 shows the small-signal model. The operating point of MOS transistor is in saturation region. The values of the various elements and parameters are described below.

The transconductances g_m is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2\mu C_{ox} I_D \frac{W}{L}} \tag{7}$$

The output conductance g_o is given by

$$g_o = \frac{\partial I_D}{\partial V_{DS}} = \lambda I_D \tag{8}$$

Note that channel-length modulation is ignored in our transconductances expression, but must include it in the output conductance expression.The gate-to-source capacitance is given by the sum of the gate oxide capacitance and the overlap capacitance

$$C_{gs} = \frac{2}{3} WLC_{ox} + WL_D C_{ox} \tag{9}$$

Where L_D is the source/drain lateral diffusion length.

The source to bulk capacitance is a junction capacitance and can be expressed as

$$C_{sb} = \frac{C_{sbo}}{\left(1 + \frac{V_{SB}}{\psi_o}\right)^{0.5}} \tag{10}$$

Where

$$C_{sbo} = C_j L_s W + C_{jsW}(2L_s + W) \tag{11}$$

ψo is the junction built-in potential, and L_S is the source diffusion length.

The drain-to-bulk capacitance is also a junction capacitance given by

$$C_{db} = \frac{C_{dbo}}{\left(1 + \frac{V_{DB}}{\psi_o}\right)^{0.5}} \tag{12}$$

Where $C_{dbo} = C_{sbo}$ for equal source and drain diffusions.

The gate-to-drain capacitance is due to the overlap capacitance and is given by

$$C_{gd} = C_{ox} W L_D \tag{13}$$

The bulk terminal of the PMOS transistors is connected to the positive supply V_{DD} and that of the NMOS transistors is connected to the negative supply V_{SS}=0. The drain voltages of M_1, M_2, M_3 and M_4 are the same as the gate voltage of M_6, namely, $V_{G,6}$. In most designs, $V_{G,6}$ is a few hundred mill volts above .Thus, $V_{G,6}$ is given as

$$V_{G,6} = V_{TN} + \Delta V_o \tag{14}$$

Where a typical overdrive voltage of ΔV_o =200mV. The drain-to-bulk capacitances of M_1, M_2, M_3 and M_4 are then given by the expressions.

$$C_{db,1} = C_{db,2} = \frac{C_{dbo,1}}{\left(1 + \frac{V_{DD} - V_{TN} - \Delta V_o}{\psi_o}\right)^{0.5}} \tag{15}$$

$$C_{db,3} = C_{db,4} = \frac{C_{dbo,3}}{\left(1 + \frac{V_{TN} + \Delta V_o}{\psi_o}\right)^{0.5}} \tag{16}$$

The drain voltage of M_6 and M_7 is the output voltage of the amplifier. The quiescent output voltage is at mid-supply for an op-amp with small offset. Then, $V_{D,6}$ is obtained as

$$V_{D,6}=V_{DD}/2 \tag{17}$$

and the constant expressions for $C_{db,6}$ and $C_{db,7}$

$$C_{db,6} = \frac{C_{dbo,6}}{\left(1 + \frac{V_{DD}}{2\psi_o}\right)^{0.5}} \tag{18}$$

$$C_{db,7} = \frac{C_{dbo,7}}{\left(1 + \frac{V_{DD}}{2\psi_o}\right)^{0.5}} \tag{19}$$

GP1 Models

There are two types of GP models

1. GP0 model
2. GP1 model

GP0 model is same as the same as the standard long channel device models. It is also possible to derive device models that are more accurate than the long channel models. Analysis of the errors incurred by the GP0 model shows that most of the modeling error comes from the expressions for transconductance and output conductance. By fitting expressions to empirical data, or data obtained from a high-fidelity SPICE simulation and refer these models as GP1.

The following simple models are found that they will work very well. For NMOS devices, the expression

$$g_{d,NMOS} = 3.1\times10^{-2} W^{0.18} L^{-1.14} I_D^{0.82} \quad (20)$$

Where the output conductance is given in mill siemens, the bias current is in milliamps, and the width and length are in micrometers. This simple model provides a very good fit over a wide range of transistor width, length, and bias current. For PMOS devices, these two models are found useful i.e. first model ($g_{d1,PMOS}$) for devices operating at low drain-to-source voltage (M_5 and M_8) and second one ($g_{d2,PMOS}$) for devices operating at high drain-to-source voltage (M_1, M_2 and M_7).

$$g_{d1,PMOS} = 4.5\times10^{-1} W^{0} L^{-1.58} I_D^{1.04} \quad (21)$$

$$g_{d2,PMOS} = 8.9\times10^{-2} W^{0.13} L^{-1.97} I_D^{0.87} \quad (22)$$

Where again the output conductance is given in mill siemens, the bias current is in milliamps, and the width and length are in micrometers. For all other circuit parameters, the GP0 model is used as described above.

```
.model pmos1 pmos vto=-0.7 kp=50u gamma=0.57 lambda=0.05 phi=0.8 mj=0.5
mjsw=0.35 cgbo=700p cgso=220p cgdo=220p cj=560u cjsw=350p ld=0.014u tox=14n

.model nmos1 nmos vto=0.7 kp=110u gamma=0.4 lambda=0.04 phi=0.7 mj=0.5
mjsw=0.38 cgbo=700p cgso=220p cgdo=220p cj=770u cjsw=380p ld=0.016u tox=14n
x1 1 2 3 4 5 opamp

.subckt opamp 1 2 7 4 10
m1 5 1 3 3 pmos1 w=232.8u l=.8u ad=18p as=18p pd=18u ps=18u
m2 6 2 3 3 pmos1 w=232.8u l=.8u ad=18p as=18p pd=18u ps=18u
m3 5 5 10 10 nmos1 w=143.6u l=.8u ad=90p as=90p pd=42u ps=42u
m4 6 5 10 10 nmos1 w=143.6u l=.8u ad=90p as=90p pd=42u ps=42u
m5 3 8 4 4 pmos1 w=64.6u l=.8u ad=27p as=27p pd=21u ps=21u
m6 7 6 10 10 nmos1 w=588u l=.8u ad=564p as=564p pd=200u ps=200u
m7 7 8 4 4 pmos1 w=132.6u l=.8u ad=84p as=84p pd=40u ps=40u
m8 8 8 4 4 pmos1 w=2.0u l=.8u ad=27p as=27p pd=21u ps=21u
rc 6 9 500k
cc 9 7 3.5p
ibias 8 gnd 10u
.ends
```

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