DESIGN AND SIMULATION OF LOW JITTER PHASE LOCKED LOOP COMPONENTS

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices and VLSI Technology)

By

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JUNE, 2007

CANDIDATE'S DECLARATION

I hereby declare that the work, which is presented in this dissertation report, entitled **"DESIGN OF LOW JITTER PHASE LOCKED LOOP COMPONENTS "**, being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Electronics and Communication Engineering** with specialization in **Semiconductor Devices & VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work carried out from July 2006 to June 2007, under the guidance and supervision of **Prof. A.K Saxena**, Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not submitted for the award of any other Degree or Diploma.

Date : 22/6/2007
Place: Roorkee

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CERTIFICATE

This is to certify that the statement made by the candidate is correct to the best of my knowledge and belief.

Date: 25/6/2007
Place: Roorkee

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ACKNOWLEDGEMENT

I wish to express my deep sense of gratitude and sincere thanks to **Prof. A. K. Saxena**, Professor, Department of Electronics & Computer Engineering, IIT Roorkee for his valuable guidance. This work is simply the reflection of his thoughts, ideas, and concepts and above all, his efforts. I am highly indebted to him for his kind and valuable suggestions and of course, his valuable time during the period of the work. The quantum of knowledge I had gained during his inspiring guidance would be immensely beneficial for my future endeavors. Apart from that, I am also grateful to **Dr. S. Dasgupta**, Assistant Professor, Department of Electronics & Computer Engineering, and IIT Roorkee for his valuable guidance during my entire course work.

Next, I feel indebted to all those endless researchers all over the world whose work I have used for my dissertation work. Their sincerity and devotion motivates me most.

I am also thankful to all my friends for their continuous support and enthusiastic help.

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ABSTRACT

Phase locked-loops (PLLs) are widely used as frequency synthesizer, clock recovery circuit and to generate well-timed on-chip clocks in high-performance digital systems, such as microprocessor. There are many issues while designing a complete PLL such as, to design for low-power, high-speed, very high operating frequency, low jitter PLL, and low phase noise.

Power supply or substrate noise perturb sensitive PLL components due to switching activity in a digital system, specifically Voltage controlled oscillator. Thus due to various noises present creates jitter in the output signal of PLL. Timing jitter significantly degrades the performance of the system.

This research work intends to find out various Phase Locked Loop (PLL) components which generate least jitter, and design and simulate them using TSMC 0.35 μm technology using tanner tools. Phase frequency detector PFD is designed using True Single Phase Clock (TSPC) D Flip-Flop; Voltage Control Oscillator (VCO) is designed using pseudo-differential CMOS ring structure. A noise canceling circuit is used to minimize supply induced noise since supply noise is major source of jitter in VCO. Typical tuning range of 100MHz to 800MHz is achieved, VCO consumes 1.44mW of power at 800MHz, the Charge Pump(CP) circuit designed has wide output range and no jump phenomenon. The power consumption of CP is 2.3mW.The features of above components that ensure least jitter are explained.

PUBLICATION COMMUNICATED

[1] A.Paliwal, S.Dasgupta, A.K. Saxena "Study and design of low jitter 3.3V Phase locked loop components in 0.35µm technology" *International Conference on Signal Processing, Communications and Networking 2008, Guindy, India.*

CONTENTS

CHAPTER 1
INTRODUCTON

1.1 OVERVIEW

Clocks are used in high-performance digital systems to sequence operations and provide synchronization between various functional units. Requirement of higher data rates and higher performance have forced technology scaling, with more and more technology scaling we are moving towards higher clock frequency. Gordon Moore predicted that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years[1]. Phase locked loops are used in digital systems to generate precisely timed clocks. As the technology scales it poses challenge in generating clock with desired quality.

Apart from clock-generation the other applications of PLL include: clock recovery, deskewing, clock distribution, spread spectrum.

Instead of crystal oscillator, PLL is used to generate high frequency clock to all parts of a chip. This is due to inability of crystal oscillator to generate stable high frequency. For data communication between chips, PLL is used to synchronize the clock with input data rate to reliably receive high-speed data.

Timing uncertainty affects performance of all the above applications, or the designers have to compromise with speed. Timing uncertainty is quantified as 'Jitter'. Various sources of jitter are explained in later chapter. Jitter requirements are more and more stringent as system speed increases [2]. PLL designers generally optimizes for low power, high speed, high integration density, aim of this work is to minimize jitter. Purpose of minimizing jitter is to make clock in high performance digital system more accurate, since all digital systems are driven by clock. By identifying various sources of jitter in different components, we design those components in this work which generate low jitter.

1.2 PROBLEM STATEMENT

To study various sources of jitter in PLL components.

Through literature find out various low jitter PLL components.

Design and simulate the Phase frequency detector.

Design and simulate the voltage controlled oscillator.

Design and simulate the charge pump.

1.3 ORGANIZATION OF REPORT

In chapter 2 Basic concepts of PLL are which includes working of various modules of PLL such as Voltage controlled oscillator, Phase frequency detector and charge Pump.

In chapter 3 designs of components for low jitter is explained along with schematic.

Results are given in chapter 4, SPICE netlists are given in Appendices.

CHAPTER 2

PHASE-LOCKED LOOP FUNDAMENTALS

The basic concept of phase locking has remained the same since its invention in the 1930s [3]. Due to progress of semiconductor manufacturing processes, the integrated PLL has been developed for variety of applications. The configuration of PLL's can be either analog or digital, but most of them are hybrids composed of both analog and digital components. The first analog PLL IC's, NE565 and CD4046, were developed by Signetics and RCA in the 1970's [4].

Design and implementation of PLLs continue to be challenging as design requirements of a PLL such as clock timing uncertainty, power consumption and area become more stringent. In order to understand the challenges in the design of such a PLL, this chapter provides basic operation of phase-locked loops.

2.1 PLL DEFINITION

The basic block diagram of a PLL is shown in fig. 2.1[5,6]. A PLL is a feedback system that compares output phase with input phase and sets a fixed relation between them. It keeps an output signal synchronizing with a reference input signal in frequency as well as in phase. A PLL tracks the phase changes that are within the bandwidth of the PLL. A PLL also multiplies a low-frequency reference signal to produce a high-frequency signal.[4]

The working of a PLL is as follows. The phase frequency detector generates an average error output signal based on the phase/frequency difference between the feedback signal and the reference signal. Output of phase detector consists of a DC component and high frequency component, thus to drive the oscillator, and remove high frequency component PFD output is low pass filtered. The filtered error signal acts as a control signal (voltage or current) of the oscillator and adjusts the frequency of oscillation to align phase of feedback signal with phase of reference signal. The frequency of oscillation is divided down to the feedback signal by a frequency divider. The phase is locked when the feedback signal has a constant phase error and the same frequency as the reference signal.

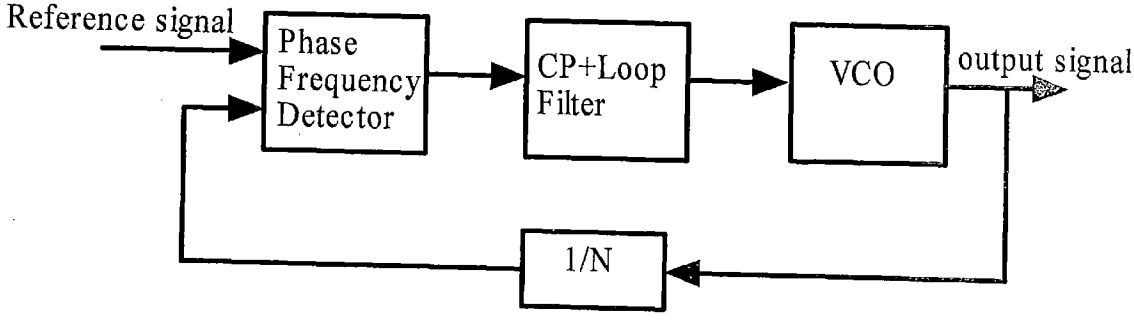


Fig. 2.1 Block diagram of PLL

Because the feedback signal is a divided version of the oscillator's clock frequency, the frequency of oscillation is N times the reference signal.

2.2 PLL COMPONENTS

The block diagram of a charge-pump PLL is shown in fig.2.1. A PLL comprises of several components:

(1) Phase-frequency detector
(2) Charge-pump
(3) Loop filter
(4) Voltage-controlled oscillator
(5) Frequency divider

Each of the above blocks is described in detail below.

2.2.1 VOLTAGE CONTROLLED OSCILLATOR:

Overview of oscillators: An oscillator is system that generates a periodic output without any input. Consider a unity gain feedback system shown in fig.2.2 [3]

$$\frac{v_{out}}{v_{in}}(s) = \frac{H(s)}{1+H(s)}$$

If this circuit satisfies two conditions namely :

$$|H(j\omega_o)| \geq 1$$

$$\angle H(j\omega_o) = 180^\circ$$

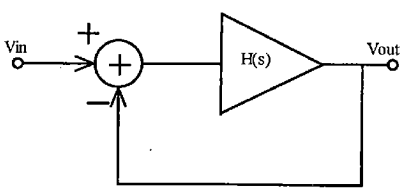


Fig. 2.2 Unity Feedback system.

Then circuit may oscillate. ω_o is oscillation frequncy. This is known as Barkhausen's criterion. Above two are necessary conditions for oscillation but not sufficient. These two criterions are difficult to meet together, and if they are not met the circuit will not sustain oscillation.

A VCO is one of the key components in a PLL, and it has a great impact on the PLL's overall performance. For CMOS based VCO design in current technology, LC and ring based VCOs are two typical choices used in PLL design. LC VCOs have a superior phase noise performance compared with ring VCOs. However, an LC VCO has a small tuning range, large layout area and possibly higher power. For reasons of design simplicity and cost effectiveness, a ring VCO based PLL is often considered first to determine if it can meet the performance requirements.

Ring oscillators

This section will explore some properties of ring oscillators. These properties are frequency of oscillation, small-signal gain and topologies.

General properties of ring oscillators

The ring oscillator comprises N amplifiers connected in a feedback loop. Each amplifier stage acts as an inverter it will just delay the signal with time t_d, and hence it is referred to as a delay cell.

Frequency of oscillation

The large-signal frequency at which the ring oscillator will oscillate at, is determined by:

$$f_{osc} = \frac{1}{2.N.t_d} \tag{1}$$

where N denotes the number of stages used. The number of stages used is mainly determined for expected level of performance for power dissipation and the phase-noise.

Start-up and oscillation criteria

The transfer function for a ring oscillator with the number of stages set to N can be shown to be:

$$H(s) = \frac{A_o^N}{(1+\frac{s}{\omega_p})^N} \tag{2}$$

A_o is gain at ω_{osc} and ω_p is 3dB bandwidth. It comprises the transfer functions of the individual delay cells. One of the criterion for oscillation is a phase shift of 180°, which is each stage contributes with 180°/N degrees of phase shift. The frequency at which this occurs is given by:

$$\tan^{-1}\left(\frac{\omega_{osc}}{\omega_p}\right) = \frac{180^\circ}{N} \Rightarrow \omega_{osc} = \omega_p \tan\left(\frac{180^\circ}{N}\right) \tag{3}$$

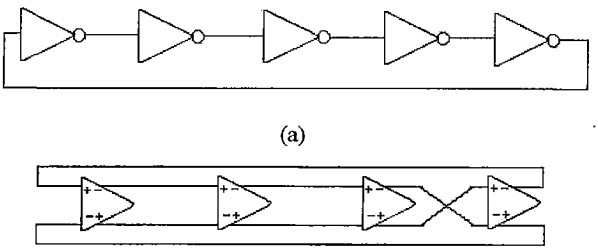
The other criterion for oscillation is a loop gain greater than 1 at ω_{osc}. Thus one can calculate the minimum voltage gain per delay cell by inserting the oscillation frequency expression (3) into the gain equation found from the transfer function (2) and solving. This calculation yields the following expression for the minimum voltage gain of each delay cell:

$$A_o = \sqrt{1+\left(\tan\left(\frac{180^\circ}{N}\right)\right)^2} \tag{4}$$

To ensure start-up and oscillation the gain should be chosen with margin above the minimum gain due to process and temperature variations. It is worth noting that the small-signal frequency of oscillation, as expressed by equation (3), is not necessarily equal to the large-signal frequency of oscillation. This discrepancy arises because the small-signal frequency is determined by small-signal parameters such as the output resistance and capacitance of each cell whereas the large-signal frequency is determined by the equivalent resistance of the load and the capacitance of each cell. This difference in oscillation frequency will make the oscillator start oscillate at the small-signal frequency but as the amplitude grows and the circuit becomes more nonlinear the frequency will shift to the large signal frequency [3]

Topologies

There are two main topologies for the ring-oscillator delay cells. The topologies are the differential and the single-ended one; their implementations can be seen in fig. 2.3[3].



(a)

(b)

Fig. 2.3 (a) Single ended (b) Differential topology

Comparison of single ended and differential topology:

To choose a topology for oscillator, the first question is should it be single-ended or differential. Here comparison between the advantages and disadvantages of each is done.

Differential oscillators can have an even number of stages. This is useful, because it means we can have quadrature clocks without additional circuitry. Tapping the signal at two opposite nodes in a differential oscillator will be $\pi/2$ radians apart. Single-ended ring oscillators, on the other hand, require phase shifting or frequency dividing circuits to generate a quadrature clock, since the phase shift at each node is π/N apart, where N is the odd number of stages in the ring oscillator.

Differential topology has limited output swing. The differential amplifier has problems with excursions toward ground, whereas the single-ended stage has rail to rail swing.

One major concern with integrated circuits is substrate noise injection from switching circuits. In this regard, the differential topology has the advantage, due to constant biasing of a current source. The current remains relatively constant independent of the differential pair switching. In the single-ended case, crowbar current flows during each transition,

which causes the supply to ripple with the current transient drops across the resistive supply lines[7]

The power supply insensitivity of differential oscillators is superior to that of the single-ended oscillators, in the same way that differential signaling has superior external noise rejection over single-ended signaling[7]

The phase noise performance of single-ended ring oscillators is very weakly dependent on the number of stages in the ring, whereas increasing the number of stages in a differential oscillator increases the phase noise, when keeping oscillation frequency and power constant[7].

2.2.2 PHASE FREQUENCY DETECTOR

Introduction:

The phase detector (PD) detects the phase difference between the reference signal and the feedback signal from the VCO and frequency divider. PD of a PLL can be an analog multiplier, an exclusive-or (XOR) gate or a J-K flip-flop, etc, for a frequency synthesizer and clock generation a charge-pump PLL with a tri-state phase-frequency detector (PFD) is used which detects frequency errors as well.

Conventional Tristate PFD:

A PFD is usually built with memory elements such as flip-flops, latches, etc. fig. 2.4[5] shows a widely used PFD based on two flip-flops. This edge-triggered tri-state PFD has a linear phase detection range of $+2\pi$ to -2π radians. It is duty-cycle insensitive as the circuit is an edge-triggered sequential machine. The delay in the reset path is put sometimes to eliminate the dead zone (undetectable phase difference range). The functionality of the PFD is depicted by its state machine diagram, and waveforms of its inputs and outputs shown in fig. 2.5 and 2.6 respectively.

The PFD can be in one of four states:

Up = 0, Dn = 0

Up = 1, Dn = 0

Up = 0, Dn = 1

Up = 1, Dn = 1

The fourth state is eliminated by gate connected at output. We can assign the remaining states as follows :

Dn = 1, Up = 0 → state = -1

Up = 0, Dn = 0 → state = 0

Up = 1, Dn = 0 → state = +1

That is why sometime this is called three state PFD.

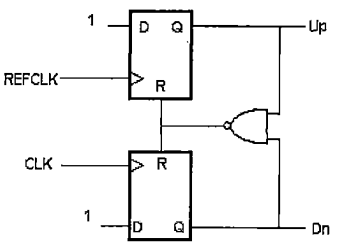


Fig 2.4 The conventional tristate PFD

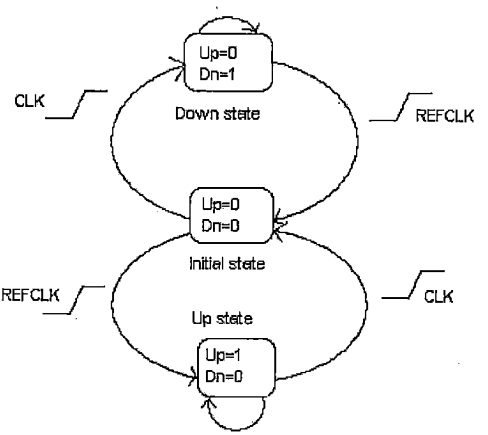


Fig.2.5 State diagram of PFD

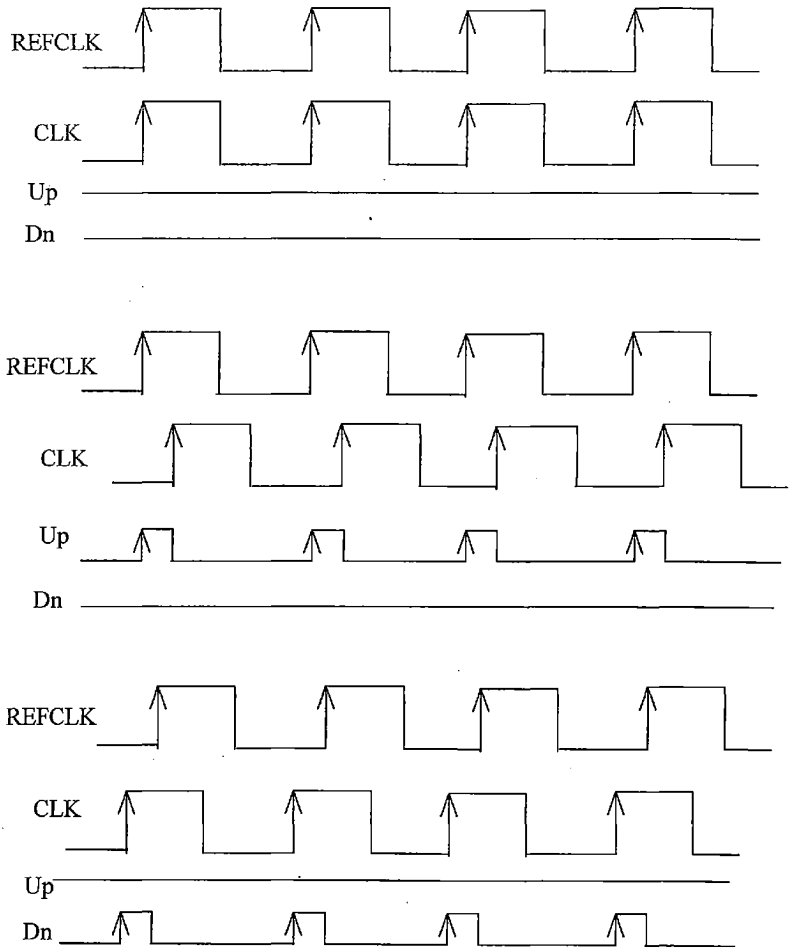


Fig 2.6 Output wave form for different cases

A transition of the reference input sets the output Up high; a following transition of the input CLK sets high the output Dn, thus creating a reset pulse at the output of the NAND gate, that will reset both of the outputs. When the outputs are returned to a low state, the reset pulse is terminated and the circuit is ready for the next input transition. Since each flip-flop in the detector exhibits a finite output pulse width, finite rise and fall times issues are essentially eliminated.

2.2.3 CHARGE PUMP

The conceptual diagram of the charge pump is shown in fig. 2.7[15]. It consists of two switched current sources driven by the tri-state PFD. The width of the output current pulse is proportional to the phase error at the PFD inputs. Thus the phase error is converted into a proportional amount of charge at the charge pump output.

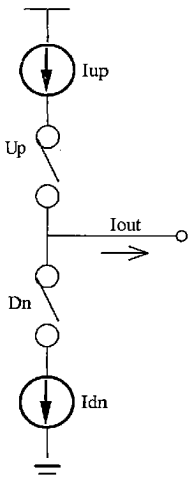


Fig 2.7 Conceptual diagram of charge pump.

The advantages of the PFD and charge pump include:

1. The capture range is only limited by the VCO output frequency range.
2. The static phase error is zero if the mismatches and offsets are negligible.

Working of charge pump:

As shown in fig.2.8[3], if QA is high Iup deposits charge on Cp this condition occurs when A leads B. If QB is high Idn removes charge from Cp , this is when B leads A. If QA and QB both are low Vout remains constant. Though QB is high for a short time due to reset delay but the difference between average values of QA and QB still accurately represents the input phase or frequency difference. Fig.2.9 shows the corresponding waveform.

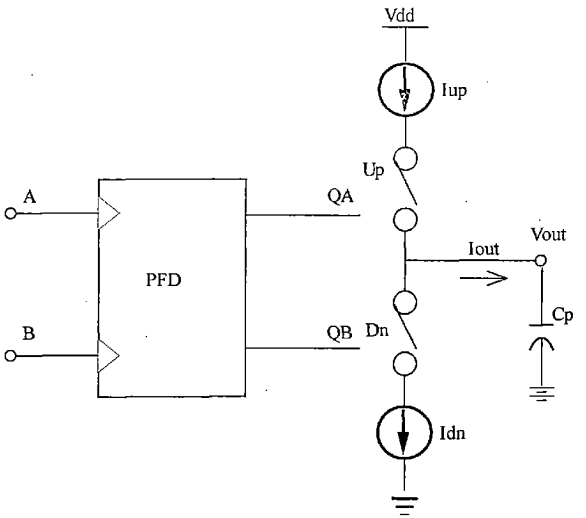


Fig. 2.8 PFD with Charge Pump

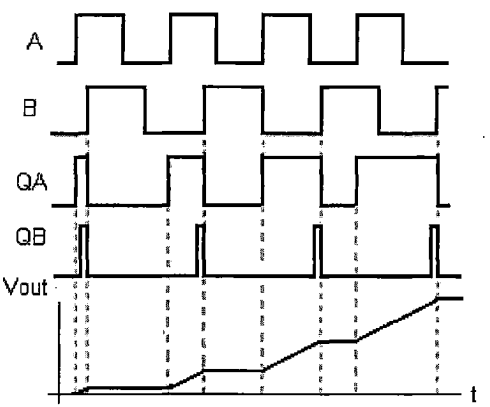


Fig. 2.9 Waveform showing working of Charge Pump.

Nonidealities in Charge Pumps

A charge pump implementation can have following nonideality.

1.**Leakage current** : Small currents that flow when the switch is off.

2.**Mismatches in the Charge Pump** :The up and down (charge and discharge) currents are unequal.

3.**Timing Mismatch in PFD:** Any mismatch in the time at which the PFD provides the up and down outputs.

4.**Charge Sharing:** The presence of parasitic capacitors will cause the charge on the desired capacitor to be shared with the parasitic capacitors[8].

2.3JITTER AND IT'S SOURCES

2.3.1Definition[9]:

Jitter can be quantified in terms of either timing jitter or phase jitter. Phase jitter is defined as the standard deviation, $\sigma_{\Delta\varphi}$, of the phase difference ($\Delta\varphi$) between the first cycle and m^{th} cycle of the signal (Fig. 2.10). Timing jitter can be expressed in terms of phase jitter by $\sigma_{\Delta T} = (T/2\pi).\ \sigma_{\Delta\varphi} = (1/\omega_0)\sigma_{\Delta\varphi}$ where the signal period, T, is $2\pi/\omega_0$.

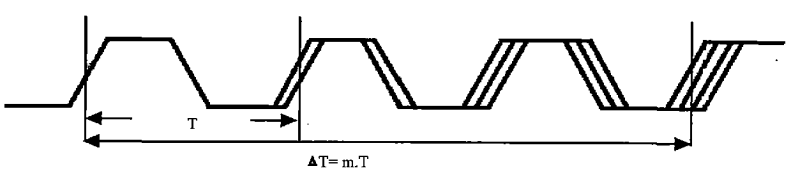


Fig.2.10 Timing jitter

Timing jitter is called short-term jitter for small ΔT and long-term jitter as ΔT goes to infinity. The tracking jitter, σ_{tr}, is a commonly used metric for a PLL output signal. It is measured as the phase difference between a clean reference signal and the PLL output signal as shown in fig.2.11.

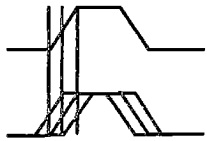


Fig.2.11 Tracking jitter

2.3.2 TYPES OF JITTER

There are many different types of jitter. Period jitter, cycle-to-cycle jitter and half-period jitter are described below.

Period Jitter

Period jitter is the change in a signal's output transition (typically the rising edge) from its ideal position over consecutive signal edges. Period jitter is measured and expressed in time or frequency.

Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the difference in a signal's period from one cycle to the next. Cycle-to-cycle jitter is the most difficult to measure usually requiring a timing interval analyzer. As shown in fig.2.12, t1 and t2 are the measured period values. And t2-t1,t3-t2 are measured jitter. The maximum value measured over multiple cycles is the maximum cycle-to-cycle jitter[10]

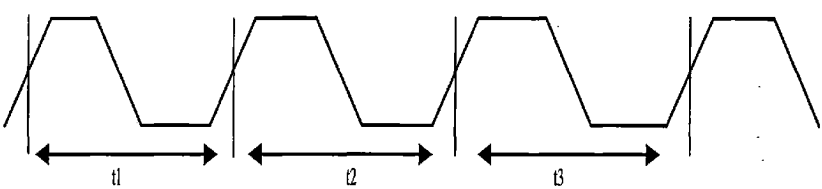


Fig.2.12 Cycle to cycle jitter

2.3.3 **Sources of Jitter** Common sources of jitter include:

- Supply noise
- Thermal Nose
- Substrate noise

- Internal circuitry of the phase-locked loop (PLL)
- Random thermal noise from a crystal
- Other resonating devices
- Random mechanical noise from crystal vibration
- Signal transmitters
- Traces and cables
- Connectors
- Receivers

Beyond these sources, cross talk, reflection, proximity effects, ground bounce, and electromagnetic interference (EMI) from nearby devices and equipment can also increase the amount of jitter in a device.

Reflection and cross-talk frequency-dependent effects may be amplified if an adjacent signal is synchronous and in phase. Aside from noise caused by power supplies and ground, changes in circuit impedance are responsible for most of the jitter in data transmission circuits [11].

2.3.4 Jitter components

The two major components of jitter are random jitter, and deterministic jitter.

Random Jitter

The random component in jitter is due to the noise inherent in electrical circuits and typically exhibits a Gaussian distribution. Random jitter (RJ) is due to stochastic sources, such as substrate and power supply. Electrical noise interacts with the slew rate of signals to produce timing errors at the switching points.

RJ is additive as the sum of squares, and follows a bell curve. Since random jitter is not bounded, it is characterized by its standard deviation (rms) value.

Deterministic Jitter

Deterministic jitter (DJ) is data pattern dependant jitter, attributed to a unique source. Sources are generally related to imperfections in the behavior of a device or transmission media but may also be due to power supply noise, cross-talk, or signal modulation.

output of feedback cascode). Feed-back cascode is used here because of its high output impedance, so that high output impedance will be seen by CCO. This reduces the supply noise sensitivity of the VCO.

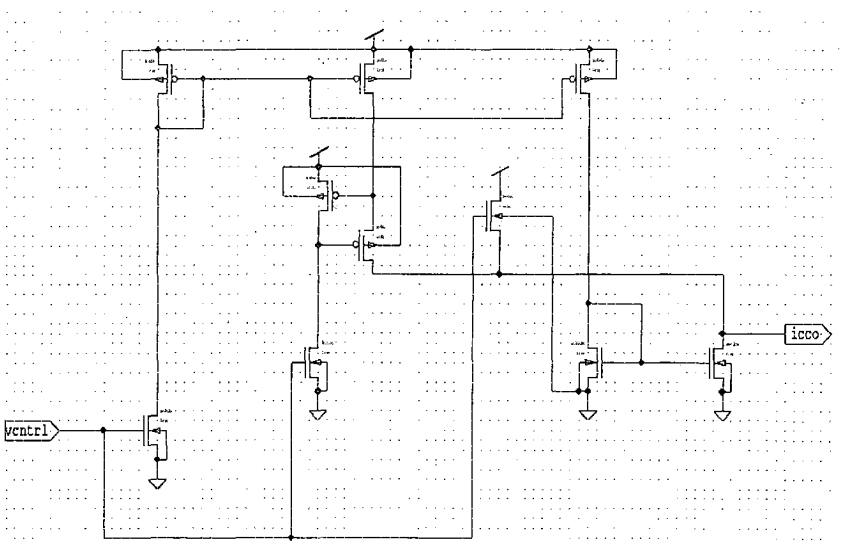


Fig. 3.2 V to I converter

The noise cancellation circuit used here compensates the residual variation of the output current I_{dr} due to supply noise. This circuit generates a compensator current, I_{co}, by mirroring a fraction of I_o (current generated by input transistor). I_{co} is then subtracted from I_{dr}. So the current to the VCO is $I_{dr} - I_{co}$. The ideal supply noise cancellation occurs when I_{dr} variation is equal to I_{co} variation due to V_{dd} noise. When V_{dd} noise causes equal variation in I_{dr} and I_{co} , ideal supply noise cancellation occurs. Therefore there will be no supply-induced variation in I_{CCO} (Drive current of CCO).The power supply sensitivity of noise canceling circuit is designed is less than feedback cascode circuit in V-I converter. A capacitor connected from V_{cco} to ground which helps to achieve power supply rejection.

Current controlled oscillator

The CCO is ring-oscillator based which has four stages of delay elements. The delay element is pseudo-differential inverter its output depends upon the two previous stages. This structure enhances the speed of the VCO. This is symmetrical delay element consists of 6 transistors, where input to the NMOS transistors comes from the immediate previous stage and input to the PMOS transistors comes from the stage that precedes the immediate previous stage. The cross-coupled PMOS transistors increase the transition state while input both PMOS and NMOS transistors are 'ON'. So the size of this transistor affects the transition of the output waveform the VCO. Increasing the size of the transistor makes output transition sharper.

Operation of delay cell & sizing

The output of the delay cell goes to zero if the input to the NMOS is '1' and input to the PMOS is '1' and goes to '1' if input to the PMOS transistor is '0', i.e. the output is controlled by NMOS transistor only while input to the PMOS transistor is '1' otherwise it is completely controlled by input PMOS transistor. So that the cell should be designed such that the input PMOS transistor size (width) is at least 4 times greater than the NMOS transistors, so that switching occurs and circuit oscillates. This VCO gives oscillations with various phases, so it can be used for multi-phase clocking scheme.

Design procedure

In delay cell, lengths of the transistors were fixed at minimum so that capacitance reduces and the current required for the higher frequency will be lesser, in turn it will reduce the power dissipation. Input PMOS transistor was designed such that size of its size is 4 times greater than the input NMOS transistor. The size of input NMOS transistor was kept as minimum. Since cross-coupled PMOS transistor doesn't have any impact on circuit performance its size was kept as minimum.

The capacitance at any output node

C_{OUT} = 2.drain capacitance + 2.gate capacitance

$= 2(3/2)\ (W_{p1} + W_{n1} + W_{p3}).L\ C_{ox} + 2(W_{p1} + W_{n1} + W_{p3}).L\ C_{ox}$

$= 5.(W_{p1} + W_{n1} + W_{p3}).L\ C_{ox}$

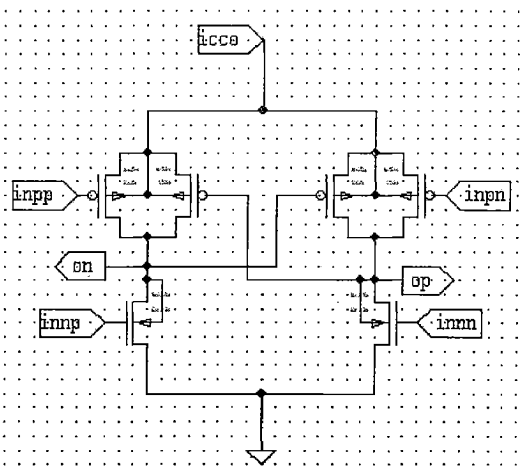


Fig. 3.3 Pseudo-differential Inverter

$$C_{OUT}.V_{SWING} = I_{CCO}/(4.F_{OSC})$$

$$I_{CCO}=4.C_{OUT}.V_{SWING}.F_{OSC} \quad [12]$$

Here C_{OX} is oxide capacitance

V_{SWING} is output swing of the VCO,(set it as 1V for initial design or find the approximate value from simulation to start with)

F_{OSC} is oscillation frequency of VCO

I_{CCO} is current delivered to CCO

Wp and Wn are widths of correspnding MOSFETs, L is length of MOSFETs.

Here constant value depends on the numbe of stages (delay elements) used in the CCO. Using the above equations the current range was chosen. Depending upon the current range the sizing of V to I converter was done such that it can deliver the whole current range. The noise cancellation circuit was designed such that it draws $1/10^{th}$ of the I_{dr}. The source follower transistor was designed such that it starts deliver the current while PMOS transistors starts to go out of saturation.

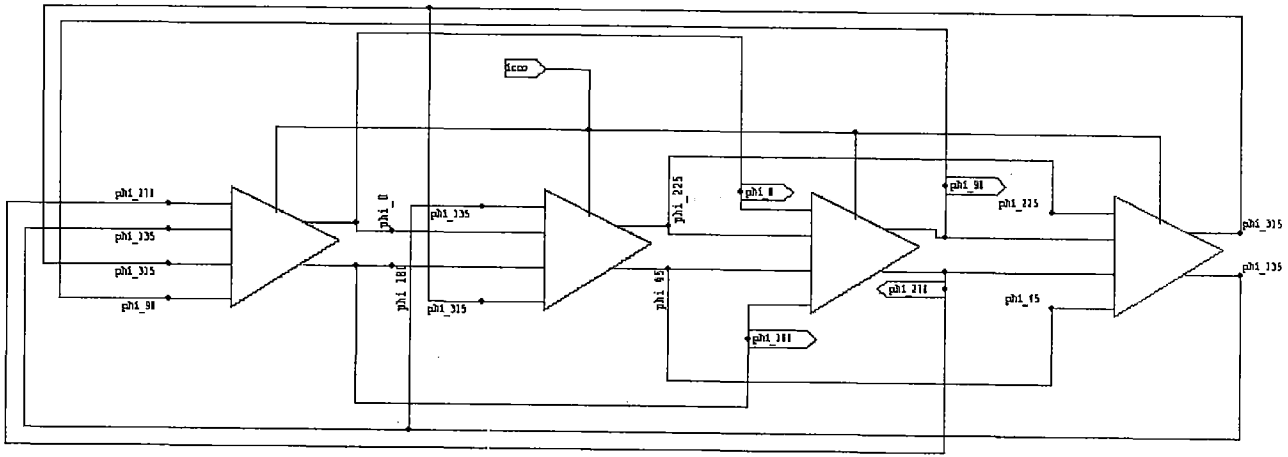


Fig. 3.4 Current controlled oscillator (Each cell is Psedo-differential inverter of fig.3.3)

3.2 PHASE FREQUENCY DETECTOR DESIGN

A conventional CMOS tristate PFD is shown in fig.3.5[5]. By plotting phase characteristic it can be found that that conventional PFD has significant dead zone. A dead zone will create large jitter in steady state. Due to internal delay of the PFD at high frequency its nodes will not completely charge and discharge, which will cause extra power consumption.

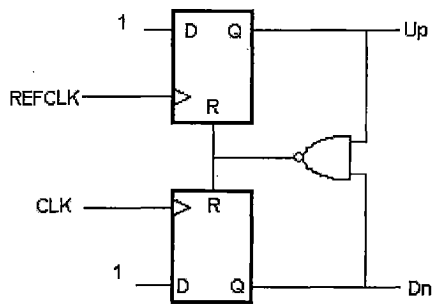


Fig.3.5. A conventional PFD

Phase characteristics of PFD is expected to be linear for a phase difference range of -2π to 2π,but reset path delay causes linear range to be smaller by some factor which can be measured. Fig. 3.6[13] illustrates the non-ideal behavior with the reference clock (REF) leading the output clock (CLK) causing an Up output. The finite reset delay of D flip-flop causes the subsequent leading edge of REF signal to arrive before the flip-flop reset, for those phase differences which are close to 2π. The reset overrides the new REF edge and does not activate the Up signal. The subsequent CLK edge causes a Dn signal, for a phase difference higher than $2\pi - \Delta$ where $\Delta = 2\pi.T_{RESET}/ T_{CLK}$; Dn signal will cause negative output. T_{RESET} is determined by propagation delay of logic gate in reset path and is not a function of input clock frequency. Due to above mention non ideality this PFD will give wrong information to CP periodically when the PLL is in acquisition state and frequency of output approach lock-in-range. Consider a case for which $T_{REF} = 2.T_{RESET}$, value of Δ for this case equals π and PFD outputs the wrong information half the total time and therefore will fail to acquire the lock. The maximum operating frequency will depend on reset path delay(T_{RESET}) and can be given as $f_{REF} <= 1/2.T_{RESET}$ [13].

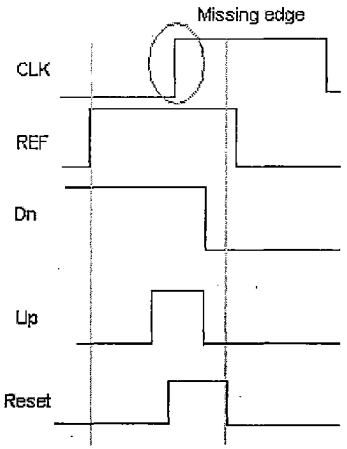


Fig.3.6. PFD nonideal behavior due to nonzero reset delay

The designed D flip-flop is TSPC flip-flop as shown in fig. 3.7[14]. The working of this flip flop is as follows: When input clock and reset signals are low node A is charged to V_{dd}. At the rising edge of clock signal, output node is connected to ground. Whenever node A is charged to V_{dd} output node becomes independent of input clock signal. On application of reset signal node A is disconnected from V_{dd} by mrl and connected to ground by mr2. As the node A gets discharged, the output node is charged through m2.

Whenever the 'Reset' signal is applied mrl prevents the short - circuit that can happen. The power consumption increases if clock signal is low in the condition of reset signal being high since a current path is made from V_{dd} to ground. Reset time will be faster if node A discharges fast, but as ml charges node A to V_{dd} while the mr2 discharges node A to ground reset time is increased. Full schematic of designed PFD is shown in fig.3.8. A conventional sequential type PFD structure is used with a pseudo - NOR gate for high-speed operation.

A conventional tristate PFD has large dead zone which generates large jitter in locked state. Apart from this due to nonideality it has frequency acquisition problem which create jitter. Designed PFD has very less dead zone hence it will not cause jitter in locked state [14].

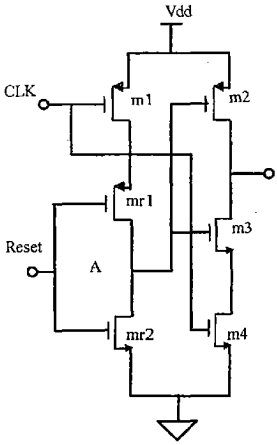


Fig. 3.7 TSPC D Flip-Flop

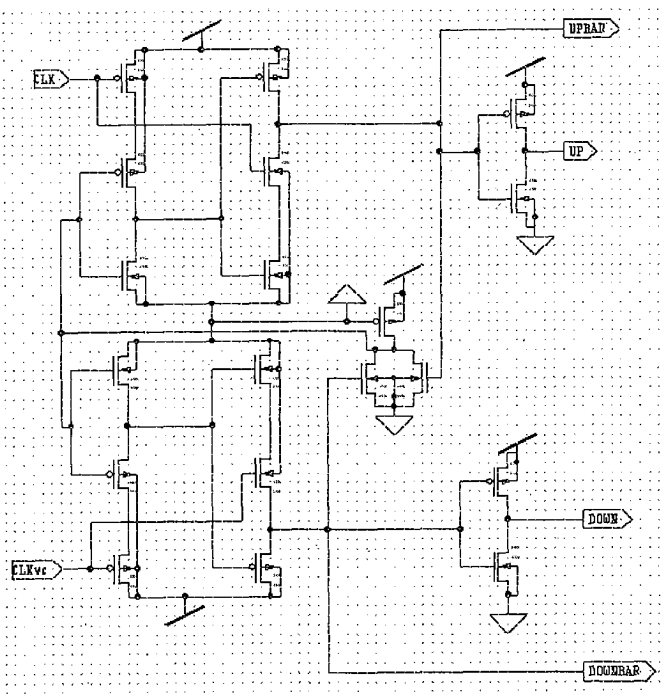


Fig. 3.8 TSPC D Flip-Flop Based PFD

3.3 CHARGE PUMP (CP) DESIGN

In locked state of PLL CP must produce a stable voltage so that constant frequency is produced at VCO output. Thus stable output is important design issue in CP [15].

Simplest CP consists of two switches and two current sources. In that Up and Dn signals are directly controlling the switches. Disadvantage of this CP is that when Up and Dn signals are logic -0 simultaneously output terminal is floating. This causes jump in output voltage producing a discontinuity at VCO output. This jump phenomenon can be considered as noise. It will make VCO frequency to be unstable.

Designed CP circuit has a simple structure as shown in fig 3.9 [15]. It is free from jump phenomenon. It consists of three main sections:

- A pump up circuit
- A pump down circuit
- A wide swing current mirror

1. **Pump Up circuit**: A pump Up circuit is a differential pair of two NMOS. The biasing of this is done with a current mirror. Along with it there is a weak pull-up current mirror. The differential inputs are driven by Up output nodes of PFD. Whenever the charge current has to be produced the Up+ terminal is made high by PFD. In this case bias current source with large value (Ibias) is steered to Mu1and difference of Ibias and Is flows through Mu3 and mirrored onto Mc5 to charge loop filter.

In the same way when Up+ terminal is low there may be small current flowing through Mu3 which will eventually get mirrored, but due to the presence of weak pull-up circuit Mcu1 turns Mu3 off by pulling up gate terminal of Mu3 to V_{dd}.

Thus by putting this weak pull up circuit there is sharp control over output.

2. **A pump down circuit:** The structure of pump- down circuit is same as that of pump-up circuit.

3. **Wide swing current mirror**: As technology scales, due to increase in short channel effect output impedance degrades. Therefore cascode current mirrors are preferred to increase output impedance but there drawback is that they reduce output swings [16].

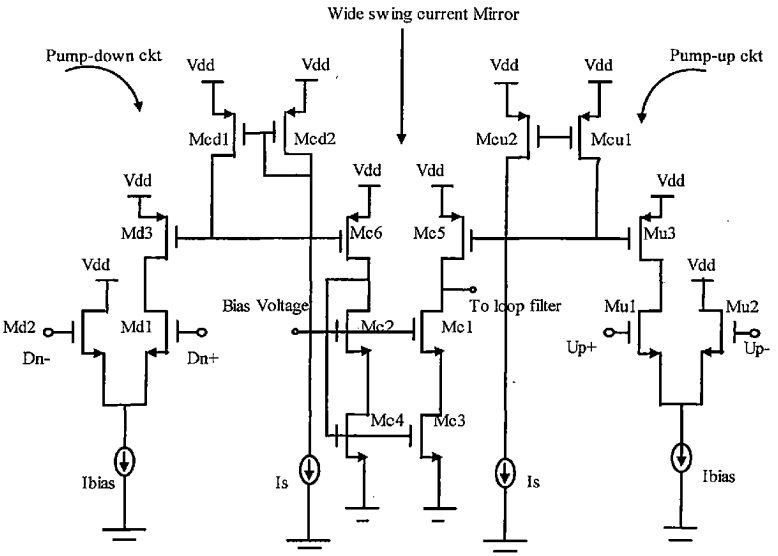


Fig.3.9 The charge Pump circuit

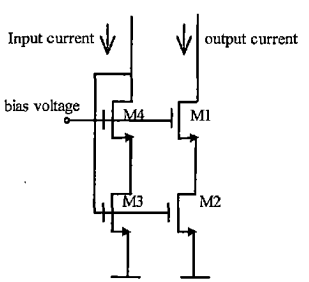


Fig.3.10 Wide swing current mirror

In this (shown in fig. 3.10) current mirror M2 and M3 are biased at the edge of triode region. Transistors M3, M4 are connected as if they are single diode connected transistor for creating gate-source voltage for M3. The function of M4 here is to reduce the drain source voltage of M3 such that drain source voltage of M2 is matched to it. This will help in achieving charging current of loop filter to be equal to discharging current which is one of important issue in charge pump design. Complete schematic of CP with loop filter is shown in fig. 3.11.

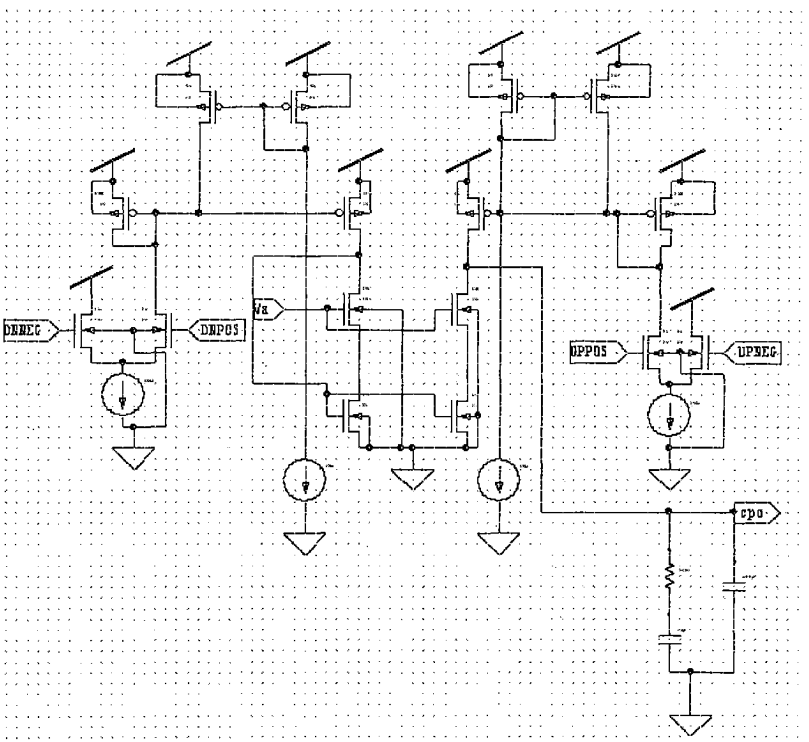


Fig 3.11 Circuit schematic of Charge Pump with loop filter

CHAPTER 4

RESULTS AND DISCUSSIONS

Results and corresponding discussion of various performance measurement tests done on PFD are as follows:

(a)Varying phase difference:

1. The reference signal and feedback signal are aligned (having same phase), the corresponding waveform is shown in fig.4.1.Both clock inputs to the phase detector have zero delay between them. With these inputs, the output is obtained of equal width, short duration Up and Dn pulses. The width of these pulses depends on the delay through the various stages of the phase detector. However, both the Up and Dn pulses are similar in all respects.

2. The reference signal is leading the feedback signal, the corresponding waveform is shown in fig.4.The phase detector produce wider Dn pulses and the Up pulses are short duration pulses.

3. The reference signal lagging the feedback signal, the corresponding waveform is shown in fig.4.3. The phase detector produce wider Up pulses while the Dn pulses continue to be short duration pulses .The phase error detection range of the PFD is not limited as in case of conventional tristate PFD.

(b)Varying frequency:

1. Frequency of the reference signal and feedback signal are same, the corresponding waveform is shown in fig.4.1. This test checks the functionality of the phase detector with different combinations of frequency differences between the reference clock and the feedback clock. Both clock inputs to the phase detector should have the same frequency. With these inputs, the output is equal width, short duration Up and Dn pulses.

2. A frequency of the reference signal is higher than feedback signal, the corresponding waveform is shown in fig.4.4. This causes the control voltage to increase and hence increase the frequency of operation of the VCO.

3. Frequency of the feedback signal is higher than feedback signal, the corresponding waveform is shown in fig.4.5. The phase detector produces wider Dn pulses causing VCO frequency to decrease. This PFD is capable of detecting both frequency and phase difference.

(c) Duty cycle sensitivity

The waveform corresponding to duty cycle sensitivity is shown in fig.4.6. The phase detector output is insensitive to these changes in duty cycle.

(d) Output Symmetry

The waveform corresponding to duty cycle sensitivity is shown in fig.4.1. These pulses are symmetrical in all respects. That is, they are of the same width and same amplitude and occur at the same instance without any delay.

Results and discussion for VCO:

1. V to I converter transfer curve is shown in fig.4.7. The V to I converter gives full range of current required by CCO.
2. VCO tuning range is shown in fig.4.8; it is obtained as 100MHz to 800MHz. A linear tuning range is must for a low jitter PLL and noise cancellation technique employed helps in obtaining linear tunning range.
3. Average power dissipation of VCO at 800MHz is 1.44mW.

Results and discussion for CP:

1. Charge pump charging the loop filter is shown in fig.4.9.
2. Charge pump discharging the loop filter is shown in fig.4.10. The charging and discharging of CP is obtained successfully, this CP is free from jump phenomenon, and thus it will not produce noise for VCO if connected at its output. A noise free CP is expected to create low jitter in output of PLL
3. Average power dissipation of CP is 2.3mW.

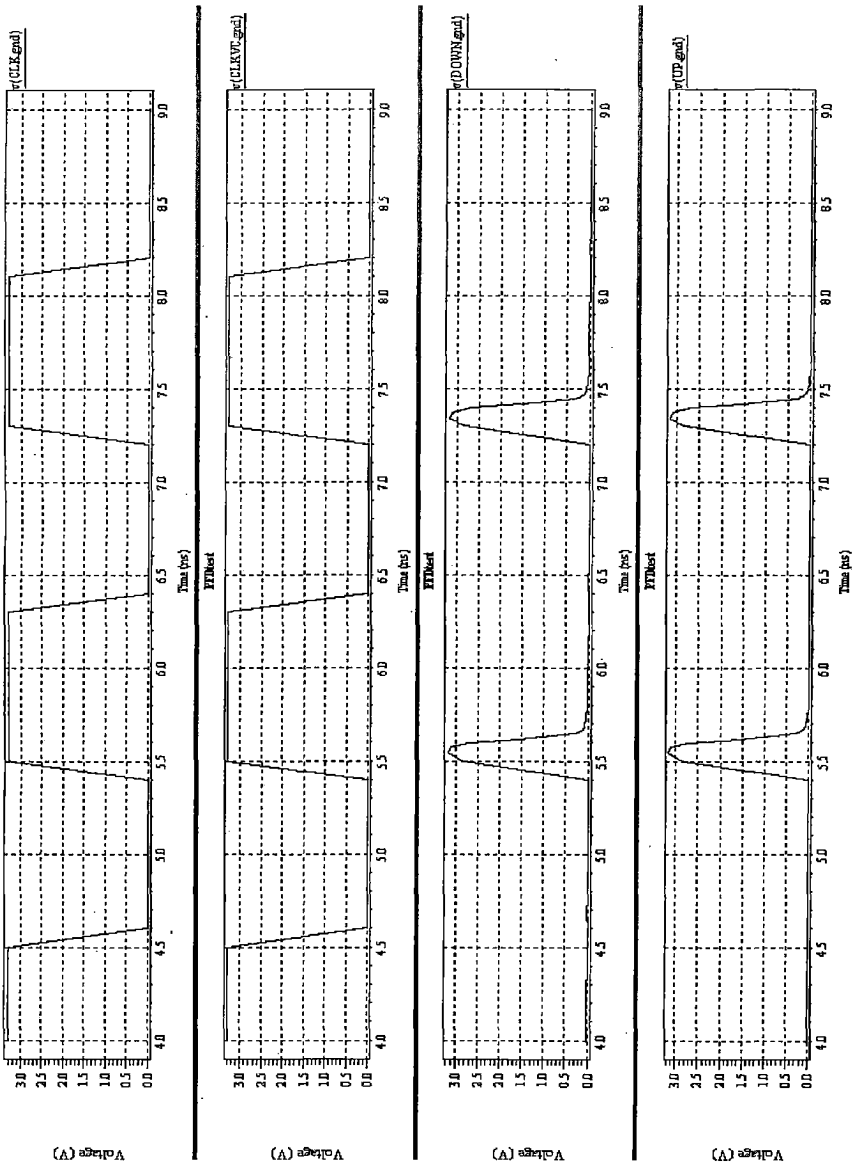


Fig 4.1 output when reference signal and feedback signal are aligned.

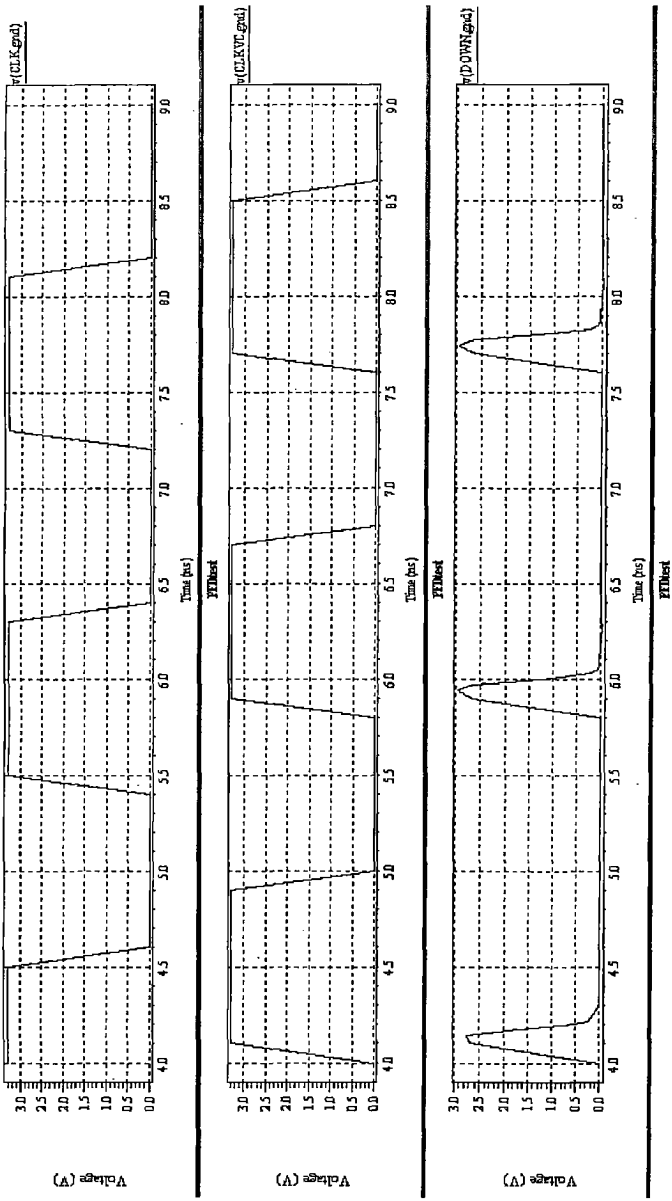


Fig. 4.2 output when reference signal leads feedback signal.

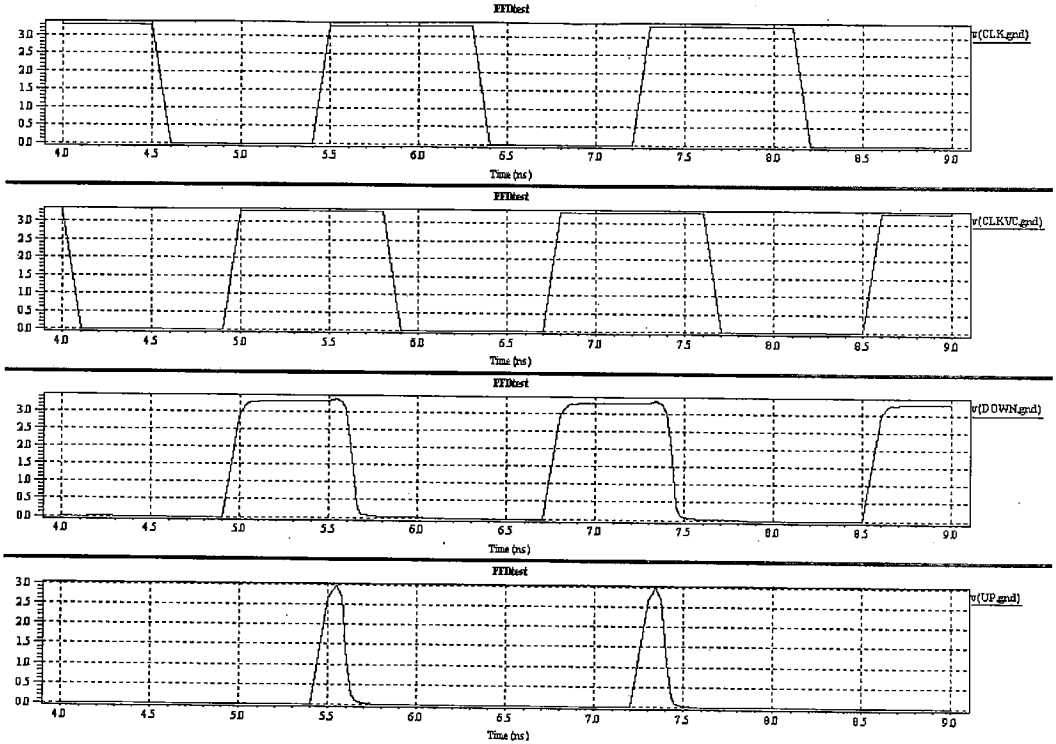


Fig. 4.3 output when reference signal lags feedback signal.

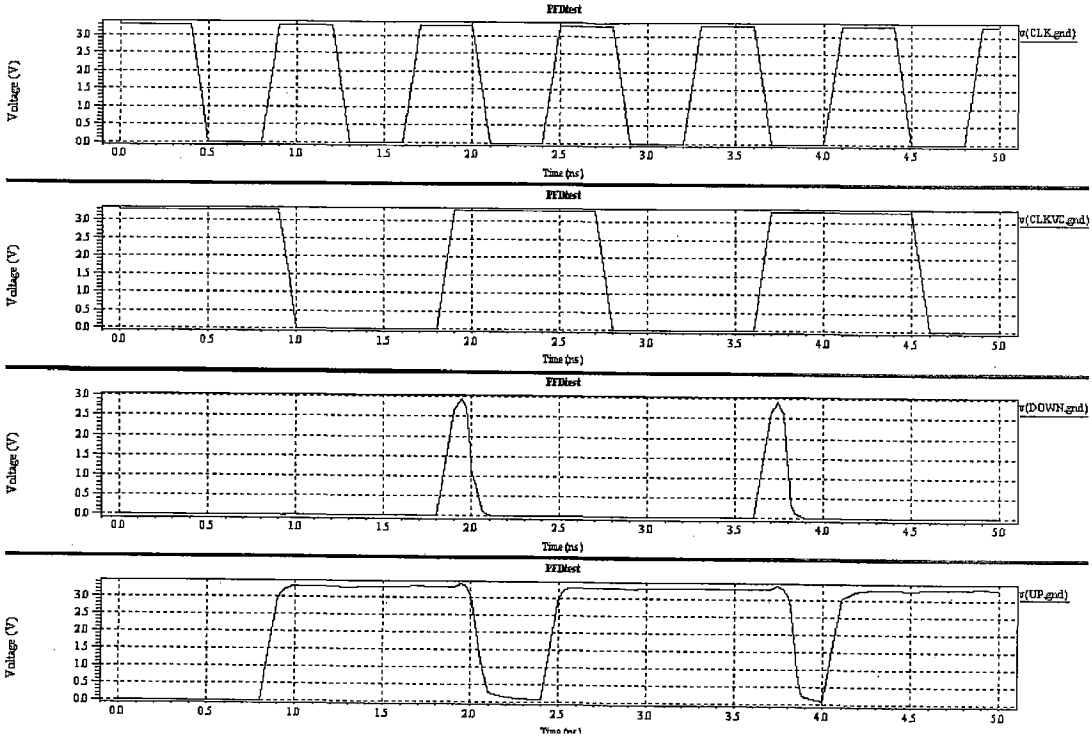


Fig. 4.4 output when frequency of the reference signal is higher than feedback signal

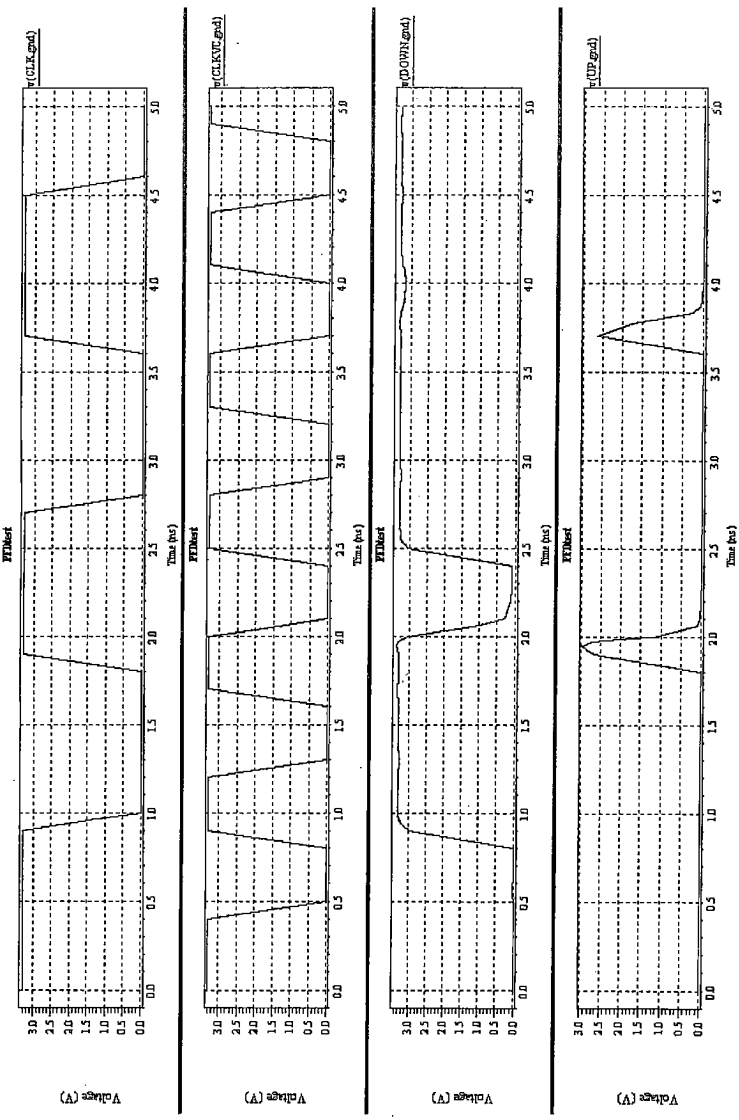


Fig. 4.5 output when frequency of the reference signal is smaller than feedback signal

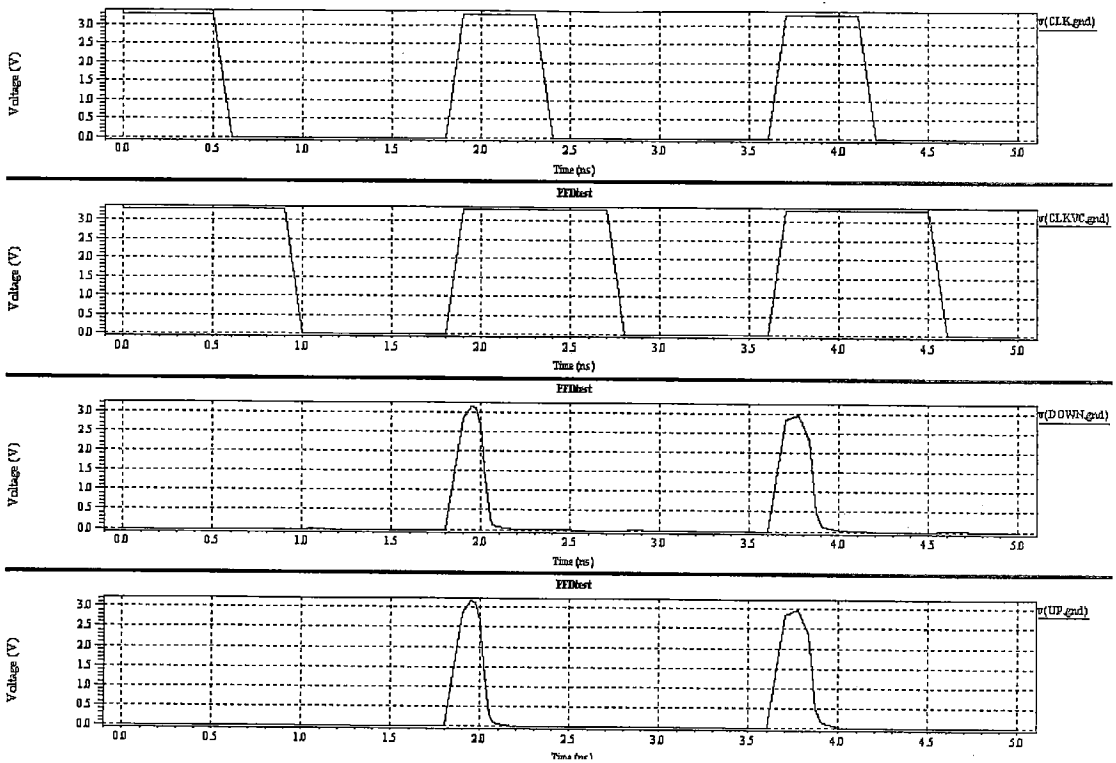


Fig. 4.6 output to check duty cycle sensitivity.

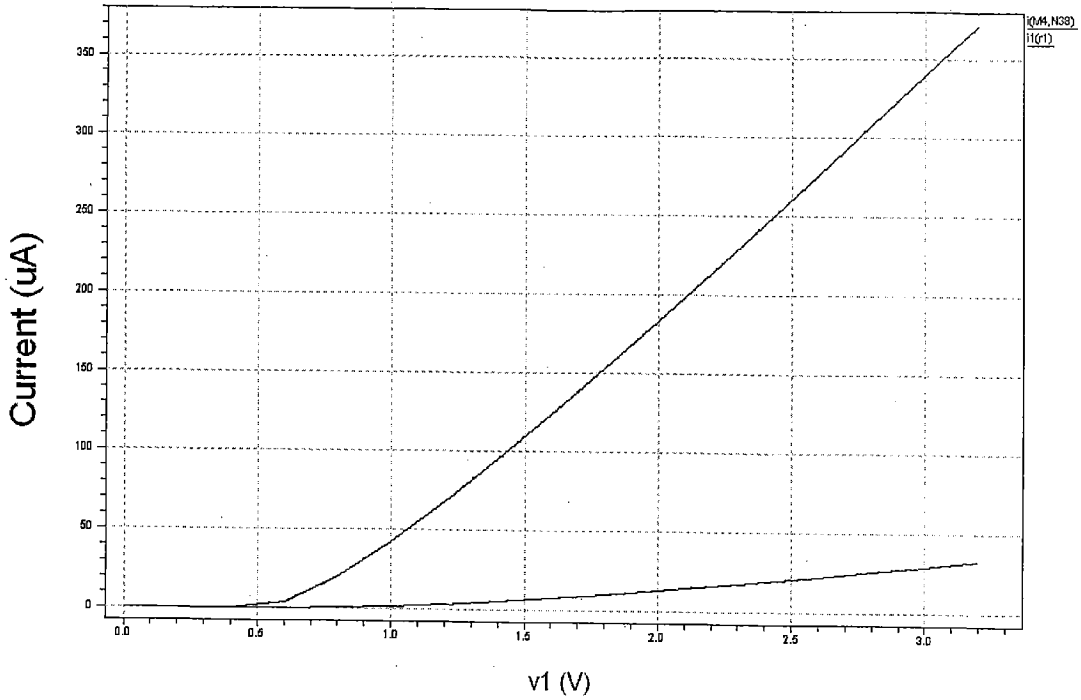


Fig. 4.7 V to I transfer curve.

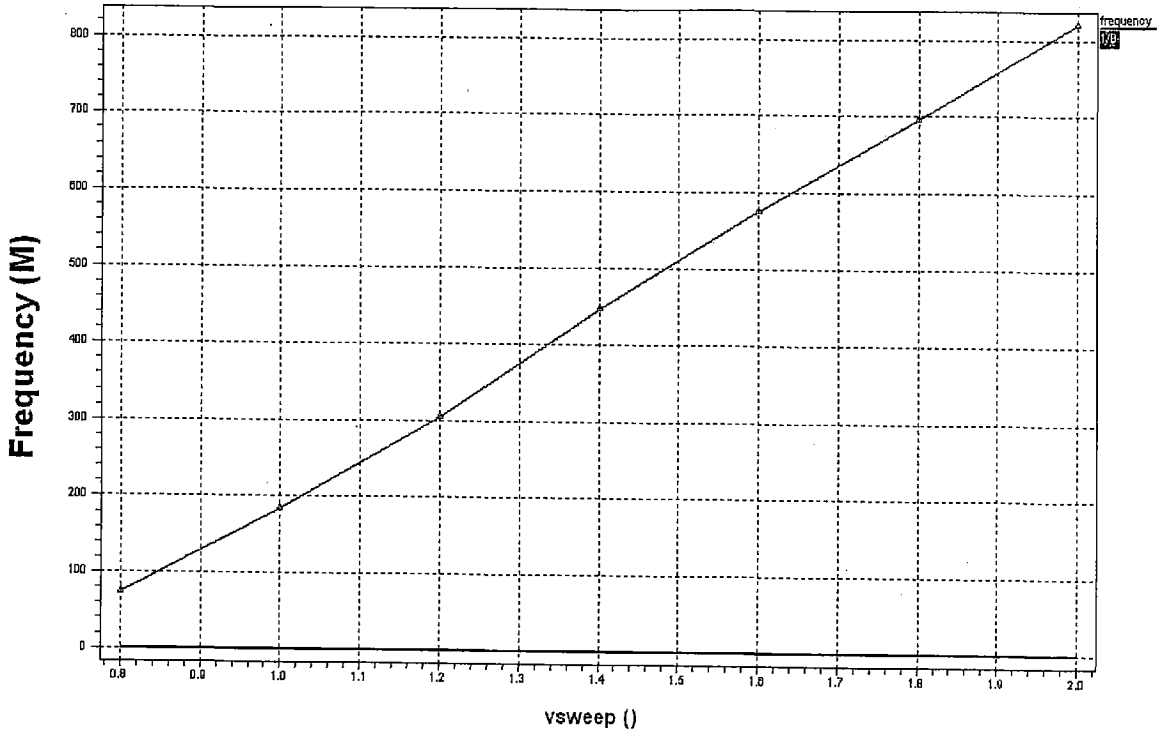


Fig. 4.8 VCO tuning range.

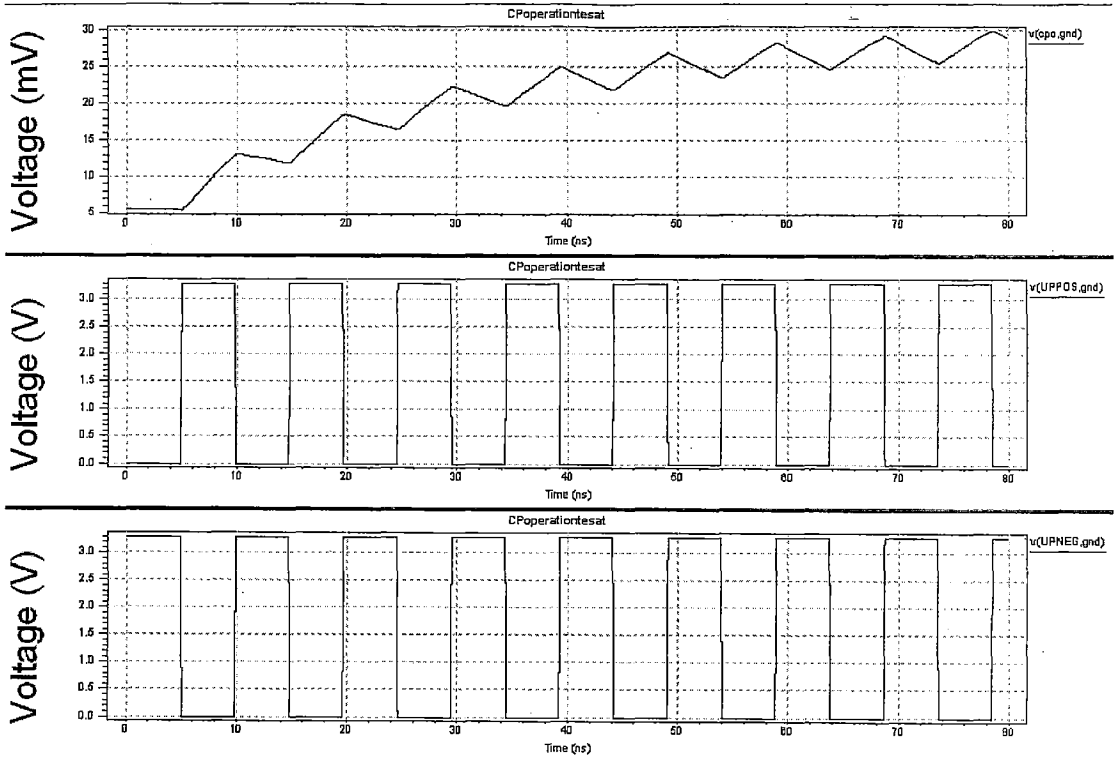


Fig.4.9 CP charging loop filter.

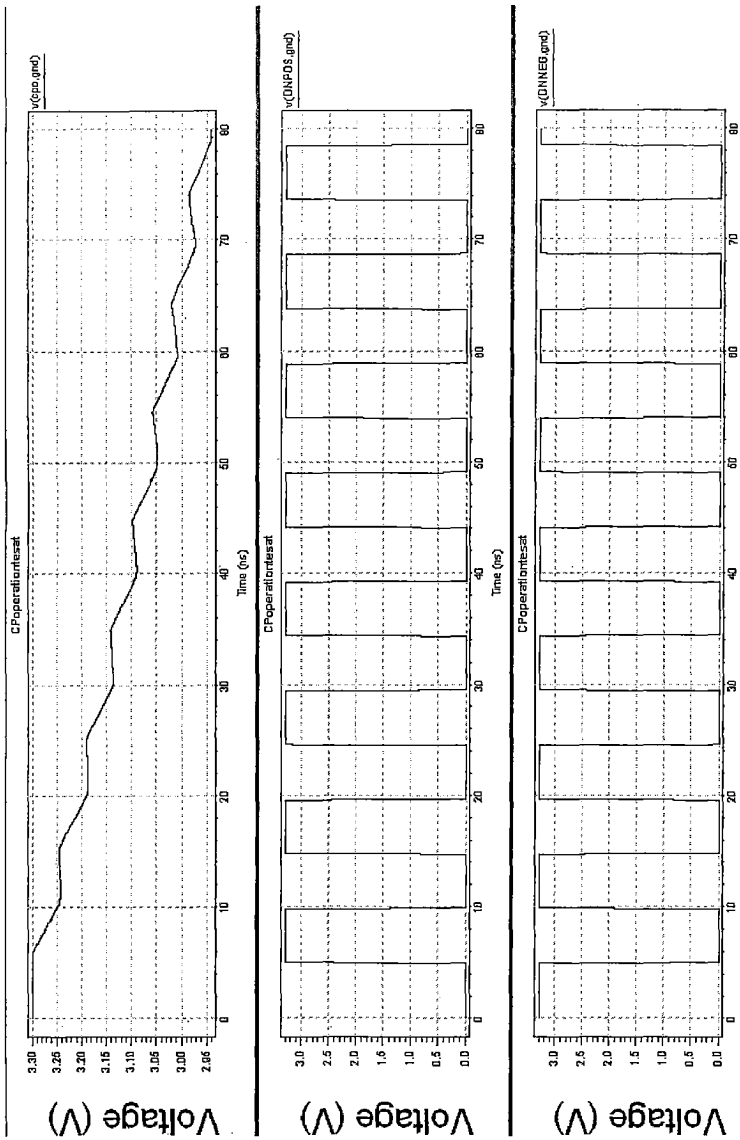


Fig. 4.10 CP discharging loop filter.

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SPICE IMPLEMNETATION CODES

NETLIST FOR PFD

```
* SPICE netlist written by S-Edit Win32 8.10
.MODEL NMOS NMOS                    LEVEL  = 49
+VERSION = 3.1        TNOM  = 27        TOX  = 7.6E-9
+XJ   = 1E-7        NCH   = 2.3579E17   VTH0  = 0.5085347
+K1   = 0.5435268   K2    = 0.0166934   K3    = 2.745303E-3
+K3B  = 0.6056312   W0    = 1E-7        NLX   = 2.869371E-7
+DVT0W = 0          DVT1W = 0           DVT2W = 0
+DVT0  = 1.7544494  DVT1  = 0.4703288   DVT2  = -0.0394498
+U0   = 489.0696189 UA    = 5.339423E-10 UB   = 1.548022E-18
+UC   = 5.795283E-11 VSAT  = 1.191395E5  A0   = 0.8842702
+AGS  = 0.1613116   B0    = 1.77474E-6  B1   = 5E-6
+KETA = 5.806511E-3  A1    = 0           A2   = 1
+RDSW = 1.88264E3   PRWG  = -0.105799   PRWB  = -0.0152046
+WR   = 1           WINT  = 7.381398E-8  LINT  = 1.030561E-8
+XL   = -2E-8       XW    = 0           DWG   = -1.493222E-8
+DWB  = 9.792339E-9  VOFF  = -0.0951708  NFACTOR = 1.2401249
+CIT  = 0           CDSC  = 4.922742E-3  CDSCD = 0
+CDSCB = 0          ETA0  = 2.005052E-3  ETAB  = 5.106831E-3
+DSUB = 0.2068625   PCLM  = 1.9418893   PDIBLC1 = 0.2403315
+PDIBLC2 = 5.597608E-3  PDIBLCB = -4.18062E-4  DROUT = 0.5527689
+PSCBE1 = 4.863898E8  PSCBE2 = 1.70429E-5  PVAG  = 1.0433116
+DELTA = 0.01       MOBMOD = 1          PRT   = 0
+UTE  = -1.5        KT1   = -0.11       KT1L  = 0
+KT2  = 0.022       UA1   = 4.31E-9     UB1   = -7.61E-18
+UC1  = -5.6E-11    AT    = 3.3E4       WL    = 0
+WLN  = 1           WW    = -1.22182E-15  WWN  = 1.137
+WWL  = 0           LL    = 0           LLN   = 1
+LW   = 0           LWN   = 1           LWL   = 0
+CAPMOD = 2         XPART = 0.4         CGDO  = 1.96E-10
+CGSO = 1.96E-10    CGBO  = 0           CJ    = 9.384895E-4
+PB   = 0.7644361   MJ    = 0.3394296   CJSW  = 2.885151E-10
+PBSW = 0.8683237   MJSW  = 0.1808065   PVTH0 = -0.0101318
+PRDSW = -159.9288563  PK2  = -9.424037E-4  WKETA = 4.696914E-3
+LKETA = -6.965933E-3  PAGS = 0.0718     )
.MODEL PMOS PMOS (                  LEVEL  = 49
+VERSION = 3.1        TNOM  = 27        TOX  = 7.6E-9
+XJ   = 1E-7        NCH   = 8.52E16     VTH0  = -0.6678491
+K1   = 0.4391761   K2    = -0.0114418  K3    = 30.0028131
+K3B  = -4.8836083  W0    = 4.596602E-6  NLX   = 5.261524E-7
+DVT0W = 0          DVT1W = 0           DVT2W = 0
+DVT0  = 0.9201674  DVT1  = 0.3997143   DVT2  = -0.0131532
+U0   = 146.2715388 UA    = 2.06943E-10  UB   = 1.669107E-18
+UC   = -1.99717E-11 VSAT  = 1.384423E5  A0   = 0.7240259
+AGS  = 0.3333763   B0    = 2.704595E-6  B1   = 5E-6
```

```
+KETA   = -8.398465E-3  A1    = 0          A2    = 1
+RDSW   = 3.10035E3     PRWG  = -0.084323  PRWB  = 0.1179404
+WR     = 1           WINT  = 5.378749E-8  LINT  = 7.000588E-9
+XL     = -2E-8       XW    = 0          DWG   = -1.395323E-8
+DWB    = 1.094885E-8  VOFF  = -0.15      NFACTOR = 1.5460516
+CIT    = 0           CDSC  = 1.413317E-4  CDSCD = 0
+CDSCB  = 0           ETA0  = 9.22207E-3   ETAB  = 3.283779E-3
+DSUB   = 0.2830114   PCLM  = 8.9992292   PDIBLC1 = 4.496569E-3
+PDIBLC2 = 1.89192E-4  PDIBLCB = -1E-3     DROUT  = 7.092917E-4
+PSCBE1 = 3.471965E10  PSCBE2 = 4.214986E-8  PVAG  = 14.9801196
+DELTA  = 0.01        MOBMOD = 1          PRT   = 0
+UTE    = -1.5        KT1   = -0.11       KT1L  = 0
+KT2    = 0.022       UA1   = 4.31E-9     UB1   = -7.61E-18
+UC1    = -5.6E-11    AT    = 3.3E4       WL    = 0
+WLN    = 1           WW    = -5.22182E-16  WWN   = 1.125
+WWL    = 0           LL    = 0           LLN   = 1
+LW     = 0           LWN   = 1           LWL   = 0
+CAPMOD = 2           XPART = 0.4         CGDO  = 2.307E-10
+CGSO   = 2.307E-10   CGBO  = 0           CJ    = 1.397333E-3
+PB     = 0.99        MJ    = 0.5501833   CJSW  = 3.961674E-10
+PBSW   = 0.9489964   MJSW  = 0.3790541   PVTH0 = 0.0194875
+PRDSW  = 141.3684631  PK2   = 1.139473E-3  WKETA = 6.477447E-3
+LKETA  = 4.151675E-3  PAGS  = 0.121025    LUA   = 4.853E-10   )
vd vdd gnd 3.3
v2 CLKvc gnd BIT ({1010} pw=2n lt=.9n ht=.9n on=3.3  off=0 rt=0.1n ft=0.1n delay=0)
v1 CLK gnd BIT ({1010} pw=2n lt=1.3n ht=.5n on=3.3  off=0 rt=0.1n ft=0.1n )
.tran .1n 15n start=0
.print v(CLK,gnd) v(CLKVC,gnd) v(DOWN,gnd)  v(UP,gnd)
M1 N6 N9 Gnd Gnd NMOS L=350n W=240n
M2 UPBAR CLK N5 Gnd NMOS L=350n W=240n
M3 N5 N6 Gnd Gnd NMOS L=350n W=240n
M4 N3 N9 Gnd Gnd NMOS L=350n W=240n
M5 DOWNBAR CLKvc N7 Gnd NMOS L=350n W=240n
M6 N7 N3 Gnd Gnd NMOS L=350n W=240n
M7 Gnd DOWNBAR N9 Gnd NMOS L=350n W=240n
M8 UP UPBAR Gnd Gnd NMOS L=350n W=240n
M9 Gnd UPBAR N9 Gnd NMOS L=350n W=240n
M10 DOWN DOWNBAR Gnd Gnd NMOS L=350n W=240n
M11 UPBAR N6 Vdd Vdd PMOS L=350n W=240n
M12 N2 CLK Vdd Vdd PMOS L=350n W=240n
M13 N6 N9 N2 Vdd PMOS L=350n W=240n
M14 DOWNBAR N3 Vdd Vdd PMOS L=350n W=240n
M15 N1 CLKvc Vdd Vdd PMOS L=350n W=240n
M16 N3 N9 N1 Vdd PMOS L=350n W=240n
M17 N9 Gnd Vdd Vdd PMOS L=350n W=240n
M18 UP UPBAR Vdd Vdd PMOS L=350n W=720n
M19 DOWN DOWNBAR Vdd Vdd PMOS L=350n W=720n
```

NETLIST FOR VCO

```
* SPICE netlist written by S-Edit Win32 8.10
.power vd  0
.power v1
.MODEL NMOS NMOS                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 7.6E-9
+XJ     = 1E-7          NCH     = 2.3579E17     VTH0    = 0.5085347
+K1     = 0.5435268     K2      = 0.0166934     K3      = 2.745303E-3
+K3B    = 0.6056312     W0      = 1E-7          NLX     = 2.869371E-7
+DVT0W  = 0             DVT1W   = 0             DVT2W   = 0
+DVT0   = 1.7544494     DVT1    = 0.4703288     DVT2    = -0.0394498
+U0     = 489.0696189   UA      = 5.339423E-10  UB      = 1.548022E-18
+UC     = 5.795283E-11  VSAT    = 1.191395E5    A0      = 0.8842702
+AGS    = 0.1613116     B0      = 1.77474E-6    B1      = 5E-6
+KETA   = 5.806511E-3   A1      = 0             A2      = 1
+RDSW   = 1.88264E3     PRWG    = -0.105799     PRWB    = -0.0152046
+WR     = 1             WINT    = 7.381398E-8   LINT    = 1.030561E-8
+XL     = -2E-8         XW      = 0             DWG     = -1.493222E-8
+DWB    = 9.792339E-9   VOFF    = -0.0951708    NFACTOR = 1.2401249
+CIT    = 0             CDSC    = 4.922742E-3   CDSCD   = 0
+CDSCB  = 0             ETA0    = 2.005052E-3   ETAB    = 5.106831E-3
+DSUB   = 0.2068625     PCLM    = 1.9418893     PDIBLC1 = 0.2403315
+PDIBLC2 = 5.597608E-3  PDIBLCB = -4.18062E-4   DROUT   = 0.5527689
+PSCBE1 = 4.863898E8    PSCBE2  = 1.70429E-5    PVAG    = 1.0433116
+DELTA  = 0.01          MOBMOD  = 1             PRT     = 0
+UTE    = -1.5          KT1     = -0.11         KT1L    = 0
+KT2    = 0.022         UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1    = -5.6E-11      AT      = 3.3E4         WL      = 0
+WLN    = 1             WW      = -1.22182E-15  WWN     = 1.137
+WWL    = 0             LL      = 0             LLN     = 1
+LW     = 0             LWN     = 1             LWL     = 0
+CAPMOD = 2             XPART   = 0.4           CGDO    = 1.96E-10
+CGSO   = 1.96E-10      CGBO    = 0             CJ      = 9.384895E-4
+PB     = 0.7644361     MJ      = 0.3394296     CJSW    = 2.885151E-10
+PBSW   = 0.8683237     MJSW    = 0.1808065     PVTH0   = -0.0101318
+PRDSW  = -159.9288563  PK2     = -9.424037E-4  WKETA   = 4.696914E-3
+LKETA  = -6.965933E-3  PAGS    = 0.0718
.MODEL PMOS PMOS                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 7.6E-9
+XJ     = 1E-7          NCH     = 8.52E16       VTH0    = -0.6678491
+K1     = 0.4391761     K2      = -0.0114418    K3      = 30.0028131
+K3B    = -4.8836083    W0      = 4.596602E-6   NLX     = 5.261524E-7
+DVT0W  = 0             DVT1W   = 0             DVT2W   = 0
+DVT0   = 0.9201674     DVT1    = 0.3997143     DVT2    = -0.0131532
+U0     = 146.2715388   UA      = 2.06943E-10   UB      = 1.669107E-18
+UC     = -1.99717E-11  VSAT    = 1.384423E5    A0      = 0.7240259
+AGS    = 0.3333763     B0      = 2.704595E-6   B1      = 5E-6
+KETA   = -8.398465E-3  A1      = 0             A2      = 1
+RDSW   = 3.10035E3     PRWG    = -0.084323     PRWB    = 0.1179404
```

```
+WR    = 1          WINT   = 5.378749E-8   LINT   = 7.000588E-9
+XL    = -2E-8      XW     = 0             DWG    = -1.395323E-8
+DWB   = 1.094885E-8  VOFF  = -0.15        NFACTOR = 1.5460516
+CIT   = 0          CDSC   = 1.413317E-4   CDSCD  = 0
+CDSCB  = 0         ETA0   = 9.22207E-3    ETAB   = 3.283779E-3
+DSUB  = 0.2830114  PCLM   = 8.9992292     PDIBLC1 = 4.496569E-3
+PDIBLC2 = 1.89192E-4  PDIBLCB = -1E-3     DROUT  = 7.092917E-4
+PSCBE1 = 3.471965E10  PSCBE2 = 4.214986E-8  PVAG  = 14.9801196
+DELTA  = 0.01      MOBMOD = 1          PRT    = 0
+UTE   = -1.5      KT1    = -0.11      KT1L   = 0
+KT2   = 0.022     UA1    = 4.31E-9    UB1    = -7.61E-18
+UC1   = -5.6E-11  AT     = 3.3E4      WL     = 0
+WLN   = 1         WW     = -5.22182E-16  WWN  = 1.125
+WWL   = 0         LL     = 0          LLN    = 1
+LW    = 0         LWN    = 1          LWL    = 0
+CAPMOD = 2        XPART  = 0.4        CGDO   = 2.307E-10
+CGSO  = 2.307E-10  CGBO  = 0          CJ     = 1.397333E-3
+PB    = 0.99      MJ     = 0.5501833  CJSW   = 3.961674E-10
+PBSW  = 0.9489964  MJSW  = 0.3790541  PVTH0  = 0.0194875
+PRDSW = 141.3684631  PK2  = 1.139473E-3  WKETA = 6.477447E-3
+LKETA = 4.151675E-3  PAGS = 0.121025   LUA    = 4.853E-10
.param vsweep='2.0'
v1 Nv1 Gnd vsweep
*V1 N1 Gnd   PWL (0 1.6 400N 1.6 900N 1.2 1400N 1.2 1900N 1.6 2400N 1.6)
*V1 N1 Gnd   PWL (0 0 400N 1.6)
*.dc lin source v1 0 2.5 .1
vd Vdd gnd 3.3
.tran .01n  70n start=0n
.print v(Nv1 gnd) v(Nv4 gnd) v(outofdcci, gnd)
*.measure tran frequency trig v(outofdcci) val=1.5 fall=2 targ v(outofdcci) val=1.5 fall=3
*.step vsweep 0.8 2.0 0.2
.SUBCKT pseduunit11 icco innn innp inpn inpp on op Gnd
M1p op innn Gnd op NMOS L=.35u W=1.8u
M2p on innp Gnd on NMOS L=.35u W=1.8u
M3p op inpn icco icco PMOS L=.35u W=.34u
M4p on op icco icco PMOS L=.35u W=.34u
M5p on inpp icco icco PMOS L=.35u W=1.8u
M6p op on icco icco PMOS L=.35u W=1.8u
.ENDS
.SUBCKT cascaded_units11 icco phi_0 phi_90 phi_180 phi_270 Gnd
Xpseduunit_1 icco phi_180 phi_0 phi_135 phi_315 phi_225 phi_45 Gnd pseduunit11
Xpseduunit_2 icco phi_45 phi_225 phi_0 phi_180 phi_90 phi_270 Gnd pseduunit11
Xpseduunit_3 icco phi_270 phi_90 phi_225 phi_45 phi_315 phi_135 Gnd pseduunit11
Xpseduunit_4 icco phi_315 phi_135 phi_270 phi_90 phi_0 phi_180 Gnd pseduunit11
.ENDS
.SUBCKT Module0 icco vcntrl Gnd Vdd
M1 Nv22 vcntrl Gnd Gnd NMOS L=1u W=1.2u
M2 Nv5 vcntrl Gnd Gnd NMOS L=1u W=1.2u
M3 Vdd vcntrl icco Gnd NMOS L=1u W=10u
M4 icco Nv15 Gnd Gnd NMOS L=1u W=6.83u
```

M5 Nv15 Nv15 Gnd Gnd NMOS L=1u W=10.4u
M6 Nv22 Nv22 Vdd Vdd PMOS L=1u W=60u
M7 Nv23 Nv22 Vdd Vdd PMOS L=1u W=60u
M8 Nv5 Nv23 Vdd Vdd PMOS L=1u W=60u
M9 icco Nv5 Nv23 Vdd PMOS L=1u W=60u
M10 Nv15 Nv22 Vdd Vdd PMOS L=1u W=9.5u
.ENDS
* Main circuit: vtol
Xcascaded_units11_1 Nv3 Nv4 Nv5 Nv6 Nv7 Gnd cascaded_units11
XModule0_1 Nv3 Nv1 Gnd Vdd Module0
* End of main circuit: vtol
M15 outofdcci outofdcc Vdd Vdd PMOS L=340n W=480n
M14 outofdcci outofdcc Gnd GNd NMOS L=340n W=240n
vb Nd7 Gnd 1.22
M1d Nd2 Nd7 Gnd Gnd NMOS L=1u W=20u
M2d Nd9 Nv6 Nd5 Gnd NMOS L=350n W=240n
M3d Nd4 Nv4 Nd2 Gnd NMOS L=350n W=240n
Md4 Nd6 Nv6 Nd2 Gnd NMOS L=350n W=240n
M5d Nd8 Nv4 Nd5 Gnd NMOS L=350n W=240n
M6d Nd5 Nd7 Gnd Gnd NMOS L=1u W=20u
M7d outofdcc Nd1 Gnd Gnd NMOS L=350n W=240n
M8d Gnd Nd1 Nd1 Gnd NMOS L=350n W=240n
M9d Vdd Nd6 Nd6 Vdd PMOS L=350n W=240n
M10d Nd4 Nd6 Vdd Vdd PMOS L=350n W=240n
M11d Vdd Nd8 Nd8 Vdd PMOS L=350n W=240n
M12d Nd9 Nd8 Vdd Vdd PMOS L=350n W=240n
M13d Nd1 Nd4 Vdd Vdd PMOS L=350n W=240n
M14d outofdcc Nd9 Vdd Vdd PMOS L=350n W=240n

NETLIST FOR CP

* SPICE netlist written by S-Edit Win32 8.10
.MODEL NMOS NMOS LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 7.6E-9
+XJ = 1E-7 NCH = 2.3579E17 VTH0 = 0.5085347
+K1 = 0.5435268 K2 = 0.0166934 K3 = 2.745303E-3
+K3B = 0.6056312 W0 = 1E-7 NLX = 2.869371E-7
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.7544494 DVT1 = 0.4703288 DVT2 = -0.0394498
+U0 = 489.0696189 UA = 5.339423E-10 UB = 1.548022E-18
+UC = 5.795283E-11 VSAT = 1.191395E5 A0 = 0.8842702
+AGS = 0.1613116 B0 = 1.77474E-6 B1 = 5E-6
+KETA = 5.806511E-3 A1 = 0 A2 = 1
+RDSW = 1.88264E3 PRWG = -0.105799 PRWB = -0.0152046
+WR = 1 WINT = 7.381398E-8 LINT = 1.030561E-8
+XL = -2E-8 XW = 0 DWG = -1.493222E-8
+DWB = 9.792339E-9 VOFF = -0.0951708 NFACTOR = 1.2401249
+CIT = 0 CDSC = 4.922742E-3 CDSCD = 0
+CDSCB = 0 ETA0 = 2.005052E-3 ETAB = 5.106831E-3
+DSUB = 0.2068625 PCLM = 1.9418893 PDIBLC1 = 0.2403315

```
+PDIBLC2 = 5.597608E-3   PDIBLCB = -4.18062E-4   DROUT   = 0.5527689
+PSCBE1  = 4.863898E8    PSCBE2  = 1.70429E-5    PVAG    = 1.0433116
+DELTA   = 0.01          MOBMOD  = 1             PRT     = 0
+UTE     = -1.5          KT1     = -0.11         KT1L    = 0
+KT2     = 0.022         UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1     = -5.6E-11      AT      = 3.3E4         WL      = 0
+WLN     = 1             WW      = -1.22182E-15  WWN     = 1.137
+WWL     = 0             LL      = 0             LLN     = 1
+LW      = 0             LWN     = 1             LWL     = 0
+CAPMOD  = 2             XPART   = 0.4           CGDO    = 1.96E-10
+CGSO    = 1.96E-10      CGBO    = 0             CJ      = 9.384895E-4
+PB      = 0.7644361     MJ      = 0.3394296     CJSW    = 2.885151E-10
+PBSW    = 0.8683237     MJSW    = 0.1808065     PVTH0   = -0.0101318
+PRDSW   = -159.9288563  PK2     = -9.424037E-4  WKETA   = 4.696914E-3
+LKETA   = -6.965933E-3  PAGS    = 0.0718
.MODEL PMOS PMOS                                LEVEL   = 49
+VERSION = 3.1           TNOM    = 27            TOX     = 7.6E-9
+XJ      = 1E-7          NCH     = 8.52E16       VTH0    = -0.6678491
+K1      = 0.4391761     K2      = -0.0114418    K3      = 30.0028131
+K3B     = -4.8836083    W0      = 4.596602E-6   NLX     = 5.261524E-7
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.9201674     DVT1    = 0.3997143     DVT2    = -0.0131532
+U0      = 146.2715388   UA      = 2.06943E-10   UB      = 1.669107E-18
+UC      = -1.99717E-11  VSAT    = 1.384423E5    A0      = 0.7240259
+AGS     = 0.3333763     B0      = 2.704595E-6   B1      = 5E-6
+KETA    = -8.398465E-3  A1      = 0             A2      = 1
+RDSW    = 3.10035E3     PRWG    = -0.084323     PRWB    = 0.1179404
+WR      = 1             WINT    = 5.378749E-8   LINT    = 7.000588E-9
+XL      = -2E-8         XW      = 0             DWG     = -1.395323E-8
+DWB     = 1.094885E-8   VOFF    = -0.15         NFACTOR = 1.5460516
+CIT     = 0             CDSC    = 1.413317E-4   CDSCD   = 0
+CDSCB   = 0             ETA0    = 9.22207E-3    ETAB    = 3.283779E-3
+DSUB    = 0.2830114     PCLM    = 8.9992292     PDIBLC1 = 4.496569E-3
+PDIBLC2 = 1.89192E-4    PDIBLCB = -1E-3         DROUT   = 7.092917E-4
+PSCBE1  = 3.471965E10   PSCBE2  = 4.214986E-8   PVAG    = 14.9801196
+DELTA   = 0.01          MOBMOD  = 1             PRT     = 0
+UTE     = -1.5          KT1     = -0.11         KT1L    = 0
+KT2     = 0.022         UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1     = -5.6E-11      AT      = 3.3E4         WL      = 0
+WLN     = 1             WW      = -5.22182E-16  WWN     = 1.125
+WWL     = 0             LL      = 0             LLN     = 1
+LW      = 0             LWN     = 1             LWL     = 0
+CAPMOD  = 2             XPART   = 0.4           CGDO    = 2.307E-10
+CGSO    = 2.307E-10     CGBO    = 0             CJ      = 1.397333E-3
+PB      = 0.99          MJ      = 0.5501833     CJSW    = 3.961674E-10
+PBSW    = 0.9489964     MJSW    = 0.3790541     PVTH0   = 0.0194875
+PRDSW   = 141.3684631   PK2     = 1.139473E-3   WKETA   = 6.477447E-3
+LKETA   = 4.151675E-3   PAGS    = 0.121025      LUA     = 4.853E-10     )
.power vd
* Main circuit: charge pump
```

```
.tran .1n 80n start =0n
vd vdd gnd 3.3
v1 DNPOS gnd BIT ({01} pw=2n lt=.9n ht=.9n on=3.3 off=0 rt=.1n ft=.1n delay=0)
v2  DNNEG gnd BIT ({10} pw=2n lt=.9n ht=.9n on=3.3 off=0 rt=.1n ft=.1n delay=0)
*v1 DNPOS gnd PULSE (0 3.3 0 0 0 1n 5n)
*v2 DNNEG gnd PULSE (3.3 0 0 0 0 1n 5n)
.print v(cpo,gnd) v(DNPOS, gnd) v(DNNEG ,gnd)
v3 Va gnd 1.22
C1 N42 Gnd 90pF
C2 cpo Gnd 12.75pF
M3 cpo Va N40 Gnd NMOS L=1u W=10u
M4 Vdd DNNEG N43 Gnd NMOS L=1u W=1u
M5 N35 Va N33 Gnd NMOS L=1u W=20u
M6 N38 DNPOS N43 Gnd NMOS L=1u W=1u
M7 N33 N35 Gnd Gnd NMOS L=1u W=50u
M8 N36 UPPOS N37 Gnd NMOS L=1u W=1u
M9 Vdd UPNEG N37 Gnd NMOS L=1u W=1u
M10 N40 N35 Gnd Gnd NMOS L=1u W=23u
M11 N36 N36 Vdd Vdd PMOS L=1u W=5u
M12 N36 N36 Vdd Vdd PMOS L=1u W=5u
M13 N38 N38 Vdd Vdd PMOS L=1u W=500n
M14 N39 N39 Vdd Vdd PMOS L=1u W=5u
```

DJ is linearly additive and always has a specific source. This jitter component has a non-Gaussian probability density function and is always bounded in amplitude. DJ is characterized by its bounded, peak-to-peak, value.

3.1 VCO DESIGN

VCO translates voltage to frequency therefore the effect of noise is pronounced more. Noise coupling with control voltage will directly affect the output frequency of the VCO, the output jitter also increases proportionally with this variation. So VCO is the most critical component of the PLL which affects the jitter performance very much. Hence the design of the low noise VCO is the must for low jitter PLL. The VCO designed here consists of Voltage to current converter followed by current controlled oscillator. The basic idea behind this structure(fig. 3.1) is that, the current signal is less affected by any noise source than voltage, and then voltage to current converter should be designed that it is less affected by noise.

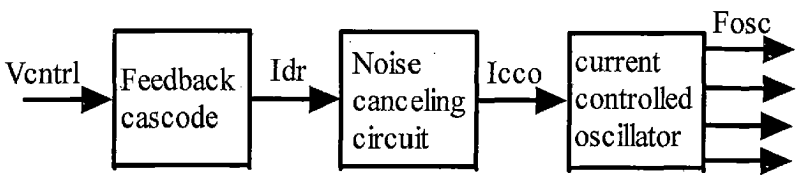

Fig. 3.1Block diagram view of VCO

V to I converter

The schematic of voltage to current converter is shown in the fig.3.2. The gate of the input transistor is controlled by V_{cntrl}, so that it sinks the current depending upon the value of V_{cntrl}. The size of this transistor decides the amount of current that goes to Current controlled oscillator(CCO). So by changing this value K_{VCO} (Gain of VCO) can be changed. The PMOS transistor above the input NMOS transistor mirrors the current to feed-back cascode circuit. Because of this structure whatever size of the PMOS transistor, it will go out of saturation for control voltages near V_{dd}. But if its size is larger it stays in saturation for almost entire rage from $V_{tn} < V_{cntrl} < V_{dd}$. V_{tn} is threshold voltage.So this PMOS transistor and the PMOS transistors in feedback cascode should have larger widths to reduce overdrive voltage. The source follower circuit is off while $V_{cntrl} - V_{cco} < V_{tn}$. Here V_{CCO} is node between V to I converter and CCO. This circuit turns on gradually at high V_{cntrl} and pumps some current to CCO which compensates I_{dr} drop near V_{dd} (I_{dr} is