DESIGN AND SIMULATION OF 4 BIT FLASH ADC IN 70nm TECHNOLOGY

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

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ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices and VLSI Technology)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being presented in the dissertation entitled **"DESIGN AND SIMULATION OF 4 BIT FLASH ADC IN 70nm TECHNOLOGY"** towards the partial fulfillment of the requirement for the award of the degree of **Master of Technology** in **Electronics and Communication Engineering** submitted in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, Roorkee (India) is an authentic record of my own work carried out during the period from July 2006 to June 2007, under the guidance of **Dr. S Dasgupta, Assistant Professor, Department of Electronics and Computer Engineering, IIT Roorkee.**

I have not submitted the matter embodied in this dissertation for the award of any other degree or diploma.

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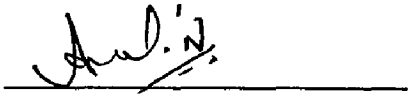

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CERTIFICATE

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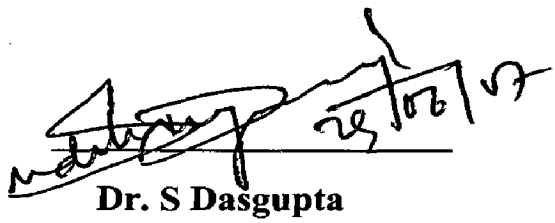

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ABSTRACT

The analog to digital converters are the key components in modern electronic systems. As the digital signal processing industry grows the ADC design becomes more and more challenging for researchers. Nowadays, ADC becomes a part of the system on chip instead of stand alone circuit for data converters. This increases the requirements on ADC design concerning for example speed, power, area, resolution, noise etc. New techniques and methods are developing day by day to achieve high performance ADCs. Of all types of ADCs, the Flash ADC is not only useful for its data conversion rate but also it becomes the part of other types of ADC for example Pipeline and multi bit Sigma Delta ADCs. The main problem with a Flash ADC is its power consumption and area, which doubles with every bit increase in resolution.

In this dissertation, a 4 bit Flash ADC is designed and simulated in 70nm CMOS technology using Tanner spice, which operates with a power supply of 0.7V and has an analog resolution of 33 mV and analog input range of 0.52V.The DNL and INL errors are in the acceptable range of 0.5 LSB.We realize this Flash ADC by designing a sample and hold circuit, and a low offset comparator. A thermometer to binary code converter is also realized.

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CHAPTER 1

INTRODUCTION

Inherently, everything in nature is analog in nature, but the computation is carried in digital. This problem can be solved by converting analog signals into digital signals, this task is carried out by Analog to Digital Converter (ADC). The computed data should again be converted back to analog, this problem is solved by using Digital to Analog Converter (DAC).This process is about converting a signal, which is continuous in amplitude and continuous in time to a signal, which is discrete in amplitude and time domains.

As the frequency operation of the modern gadgets are continuously increasing and are reaching Radio frequency (RF) range. So, we need to use an ADC which has very low conversion time. Among all the ADC architectures, Flash ADC architecture have least conversion time[1] and therefore regarded as fastest ADC.

ADC has both analog and digital components, thus designing and interfacing these modules becomes a challenge. This challenge has given rise to a new design technique, known as Mixed Signal Design, which is often called as Analog and Mixed signal Design. In industry, the established technology for Analog and Mixed Signal Designs is 130nm[4,12]. The problem introduced in this dissertation is to design and simulate 4 bit Flash ADC in 70nm technology. This operates with 0.7V power supply and has an analog resolution of 33mV.

Flash ADC consists of three sections, namely Sample and hold circuit followed by comparator section. In comparator section, the input voltage is compared with the reference voltage. The reference voltage is generated using a voltage divider network. The output from the comparator section is in thermometer code. This is converted to binary code using an encoder[2].Flash ADC has the same conversion time for any number of resolutions. But, its die area and power consumption doubles with the

resolution. In spite of these disadvantages, it is preferred for high speed operation, since it has a single compare cycle.

Organization of the thesis

Chapter 1 introduces Flash ADC architecture and presents the problem.

Chapter 2 describes different ADC specifications which describes its performance and also discusses some of the prominent ADC architectures, compares them with Flash ADC. It discusses its merits and demerits.

Chapter 3 describes the process of sampling, and its necessity. Some of the popular sample and hold(S/H) circuits are presented and the possible errors that can occur and its causes are discussed.

Chapter 4 describes different amplifiers that are used in Analog and Mixed Signal Designs. Its voltage-current characteristics that govern the operation of amplifiers and their gains are discussed.

Chapter 5 describes the components that are used in the simulation of proposed ADC.

Chapter 6 describes the simulation and results, and also discusses the results.

Chapter 7 concludes the dissertation thesis and discusses the scope for future work.

2.1.1. Resolution

It is the number of bits, which are used to express the digital output. For an N bit ADC, the digital resolution is N. The analog resolution[1] is defined as the value of analog input which the LSB represents. It is given by full scale input voltage divided by 2^N. The analog resolution is expressed in V.

$$\text{Analog resolution} = \frac{V_{ref}}{2^N} \tag{2.1}$$

2.1.2. Quantization Error

The analog input signal is quantized using an ideal ADC and then converted back to an analog signal using an ideal DAC the output will look like a staircase as in figure.2.1. The difference between the original and quantized signal is the quantization error. The more bits there are to represent the original signal, the lower the quantization error. Quantization error is a loss of information that can not be recovered or reconstructed. Since the analog input is an infinite valued quantity and the output is a discrete value, an error will be produced as a result of the quantization. Quantization error[1,6], Q_e, is defined as the difference between the actual analog input and the value of the output (staircase) given in voltage.

It is calculated as

$$Q_e = V_{in} - V_{staircase} \tag{2.2}$$

where, the value of the staircase output, $V_{staircase}$,can be calculated by

$$V_{staircase} = D.\ \text{resolution} = D.V_{LSB} \tag{2.3}$$

where, D is the value of the digital output code and V_{LSB} is the value of 1 LSB in volts. We can also easily convert the value of Q_e in units of LSBs. Q_e can be generated by

subtracting the value of the staircase waveform from the input voltage. Ideally, the magnitude of Q_e will be no greater than one LSB and no less than 0. It would be advantageous if the quantization errors were centered about zero that the error would be at most ±l/2 LSBs[6](as opposed to +1LSB). This is easily achieved. Here, the entire transfer curve is shifted to left by l/2 LSB, thus making the codes centered around the LSB increments on x-axis. This drawing illustrates that at best, an ideal linear ADC will have quantization of ± l/2 LSB.

2.1.3. Differential Nonlinearity Error

It represents the nonlinearity of the ADC. It is defined by difference between the actual code width of a nonideal converter and the ideal case[1].

DNL = Actual step width – Ideal step width

It is often expressed in LSBs. Ideally, the DNL is less than ½ LSB.

2.1.4. Missing codes

In ADC, missing codes happens when the DNL is below -1 LSB, then two analog ranges will have the same output code. Thus, one output code gets missed. Ideally, the number of missing codes should be zero.

2.1.5. Integral Nonlinearity Error

It is defined as the difference between the data converter output values and a reference straight line drawn through the first and last output values. INL defines the linearity of the overall transfer curve and can be described by $V_{out} - V_{in}$ at the transition points. Ideally, INL should be less than ½ LSB.

Literature Review

To increase the linearity of flash ADC beyond the matching limit of the single comparator, averaging is used [Klaas Bult et.al [22]]. Multiple gain-stage architectures allow the use of interpolation to reduce the number of front-end amplifiers and thus the input capacitance of the converter. By scaling the amplifiers in the analog preprocessing

chain from front to back also, the overall power consumption can be optimized under the given gain bandwidth constraints. There exist basically two different strategies for implementing a flash ADC employing interpolation and averaging. Resistive interpolation employs averaging resistors between the outputs of adjacent amplifiers. In Kattmann et.al[23], defines interpolation to be a way to generate extra zero crossing points by using the information from neighborhood.

In K. Uyttenhove et.al [24], resistive interpolation is discussed that a resistive ladder is needed, that can keep the reference voltages stable, in spite of the ladder feedthrough. For a Ultra Wideband(UWB) ADC with similar system specifications, a ladder resistance for as low as 250 Ohm have been reported, which adds to the power consumption of ADC. Another issue with the resistive interpolation is that over-range values have to be handled within the system. This requires more comparators, which implies more power.

A common problem of such architectures is the need for overrange comparators to maintain linearity at the edges of the conversion range. Special circuit techniques allow reducing the number of overrange comparators, but they rely on matching the termination resistor with the output resistance of the overrange blocks. Furthermore, an external sample-and-hold circuit is almost always required, which consumes a significant fraction of the total power budget in wide-band applications.

Capacitive interpolation, on the other hand, uses a purely reactive averaging network between the outputs of adjacent amplifiers. A big advantage of capacitive interpolation is that it requires neither power consuming overrange comparators nor any static averaging termination. Also, no external sample-and-hold is required, because the interpolation capacitors at each stage are readily used as sampling capacitors implementing: multistage input-offset-sampling (10s) architecture with distributed front-end sample-and-hold.

In Sandner, C. et al[25], it is shown that for capacitive interpolation, a code-dependence could be observed, if no reset phase is used for the sampling capacitors. A reset-phase free implementation would imply that the previous sample is never removed from the

interpolating capacitors, prior to the arrival of the new sample. But to introduce a reset phase can be a challenge, as the clock frequencies are approaching the limits of the technology. The use of additional power in the drivers for the interpolating capacitors can overcome the problem of code dependence.

In Van de Plassche et.al[1], it is explained that the use of interpolation is beneficial for low-power consumption and for reducing the input capacitive load. The principle can be applied using voltage signals or current signals. However the use of voltage signals is difficult in a CMOS implementation since in order to have interpolation the preamplifiers have to drive a resistance network. The inverting first stage amplifiers drive the interpolating capacitive network of the second stage, here implementing an interpolation factor 2. The interpolation factor at the converter input is given by the total number of frontend amplifiers minus 1.

The total input capacitance of the converter in the sampling phase is given by the sum of the front-end capacitors plus wiring parasitics. One drawback of the capacitive interpolation structure is the capacitive divider formed by the sampling capacitor and the input capacitance of the amplifier during the amplification phase. The overall gain of each stage is given by the intrinsic gain of the amplifier and the capacitive divider ratio.

In order to minimize the total input capacitance of the converter, the sampling capacitors should be chosen as small as possible, for a resolution of 6 bits ultimately limited by capacitor mismatch. For minimum gain loss the amplifiers' input devices should therefore he as small as possible.

Voltage estimator increases the efficiency of two step flash ADC. Behavioral modelling of analog components is also done, the modelling of the components are done in C or FORTRAN [H. Alan Mantooth et. al [26]]. But this approach has a drawback that, the models are unavailable for large analog circuits. The models are also inaccurate for smaller analog models. The languages that are used for modelling also have drawbacks, due to which accurate modelling is not possible.

In a flash ADC, comparators generate an output pattern called a thermometer code. According to the thermometer code, the bubble error corrector followed by the encoder can generate the digital binary outputs. When the comparators' outputs were unknown and passed through the encoder of ADC, the meta-stability errors would occur[Patmann et.al[27]]. The 2^N-1 comparators in flash ADC also cost too large area and lead much power consumption. As the resolution of the ADC increases, the number of comparators increases. At every compare cycle, all the comparators conduct.

This problem can be solved by designing an architecture, in which only half the number of comparators operate at each compare cycle[Tan P. B. Y et.al[28]].The thermometer codes of flash ADC are composed of series 0 and 1 generated by comparators. The bubble error corrector is used to detect and correct possible bubble error codes. The final digital outputs are determined by the interface of 0 and 1 of thermometer codes after passed the encoder.

The conventional multi-step sub range converters perform the conversion operation in sequential steps using low resolution flash ADC's, programmable gain amplifiers, track and hold circuits, a number of DAC's and other circuits[Mayes et.al[29]]. This requirement of larger change in the gain tells upon the speed of conversion owing to the larger settling time of the programmable gain amplifier. The delay time is further increased in the process of storing the intermediate results, digital to analog conversion and final digital error correction operation.

In Park et.al[30], it is shown that the optimum inductance depends on the parasitic capacitance, so that a smaller inductance is required in more advanced CMOS processes. Use of inductors in the comparator load increases the bandwidth of the ADC. To increase the switching of the circuits, a clock signal having the amplitude less than the supply voltage is used. For the switching to be faster, the parasitics should be small. The sample and hold circuit has many parameters that describe its operation.

Due to mismatch, the resistor values deviate from the nominal values resulting in deviation of the reference levels. The transfer function of the ADC thereby becomes nonlinear, which introduces harmonics in the output. Another source of nonlinearity is the input offset error voltage of each comparator, which is different for each comparator due to process variations. However, if DEM is applied the spurious tones in the output due to the nonlinearities can be suppressed [P. Stubberud et.al[31]].

In P. Stubberud et.al[31] , it is explained that the dynamic element matching can be used to compensate for mismatch that yield nonlinearity errors in the transfer function. When using static matching the components are placed close together in certain patterns and made sufficiently large to yield small relative errors. Another approach used in, e.g., current steering digital-to-analog converters (DACs), pipelined ADCs, and flash ADCs, is to use the DEM technique.

If any pair of the 2^N - 1 comparators are allowed to interchange their reference voltages the reference voltages could change by as much as the full-scale voltage VFS every sample. This large voltage fluctuation would limit the speed of the overall converter, since the reference voltages must settle every sample before the output of the ADC can be used. To reduce this settling time we only allow neighboring comparators to interchange their reference voltages. This yield lower reference voltage fluctuations and therefore a shorter settling time [E.Sall et.al[32]]. Restricting the reference voltage interchange to neighboring comparators still reduces the spurious tones to a large extent compared with not using DEM, and it is almost as efficient as when letting any pair of comparators interchange their reference voltages [E.Sall et.al[32]].

The most significant impact of the decreased power supply voltage for analog circuits is the decrease of the signal swing, which leads to the lower signal to noise ratio and dynamic range. The impacts of the deep-sub-micron technology are two folds: the decreased signal swing and better device matching properties.

It is beneficial to move into deep-sub-micron technologies in terms of accuracy and speed. However, the power consumption benefit will be partially cancelled off by the limited signal swing.

In Daegyu Lee et.al[33], various techniques have been devised to expedite encoding, but major schemes are intense on algorithms. Usually these encoders need multiple layers of logic gates. Multiple layers of logic gates can cause enough delay in signal transition, which might diminish the benefits of ultra-fast comparators like TIQ, which has transition delay of two-inverters connected in series.

In M. Chai et.al [34], a robust, fault-tolerant scheme is proposed to achieve high Spurious Free Dynamic Range (SFDR) in an averaging flash A/D converter using comparator chopping. Chopping of all comparators using a novel array of truly binary random number generators can be used. Chopping randomizes the residual offset left after averaging, further pushing the dynamic range of the converter. Power consumption and area are reduced because of the relaxed design requirements for the same linearity.

A new flash ADC is developed by Shih-Chang Hsia et.al[35], which is based on simple CMOS circuit. By adjusting the ratio of channel length and width, the transition threshold of the CMOS inverters is various to detect input analog signal. Then their results are encoded to the digital code. The advantages are that the ADC circuit does not need any resistor and use simple CMOS inverters rather than analog comparators. In the typical flash A/D converter, we require $(2^N - 1)$ comparators if the resolution is N bits. Since each comparator used different reference levels (v1, v2...), we need to use resistors to divide the reference voltage. Thus the number of resistors required is 2^N .In general, the architecture has some drawbacks, as described following.

The converting accuracy is limited at the section resistor. Since the resistor is always implemented with semi-conductor materials, we hardly achieve high accuracy resistor value in a chip due to process deviation. Moreover, the resistor value is in proportion to the line length, thus the resistor is always designed at low value to keep small chip size.

Obviously, the reference voltage must supply enough power driving to reduce the loading affect, since the input current is high in low value resistors. Moreover, the analog comparators must be designed with high gain in order to detect the input voltage in small change and increase the noise margin. Hence the circuit complexity becomes high. The input signal is connected to the input of all comparators in parallel driver since the input capacitor is equal to the summation of the input capacitor of all comparators. In practical applications in a system, the shortcoming of the conventional flash A/D converter is to require large input signal driving, high reference accuracy and high driving reference voltage. This will cause the power dissipation highly.

2.2. ADC Architectures

2.2.1Flash ADC [1,4]

Flash or parallel converters have the highest speed among all type of ADC. They utilize one comparator per quantization level, i.e. $(2^N - 1)$ and 2^N resistors. The reference voltage is divided into 2^N values, each of which is fed into the comparator. The input voltage is sampled and compared with each reference value and results in a thermometer code at the output of the comparator section. A thermometer code will exhibit all zeros for each resistor level if the value of V_{in} is less than the value on the resistor string, and ones if V_{in} is greater than or equal to voltage on the resistor string.

A simple $2^N - 1$: N digital thermometer encoder circuit converts the compared data into an N-bit digital word. The obvious advantage of this converter is the speed with which one conversion can take place. Each clock pulse generates an output digital word. The advantage of having high speed, however, is counterbalanced by the doubling of area with each bit of increased resolution. For example, an 8-bit converter requires 255 comparators, but a 9 bit ADC requires 511.Flash converters have been traditionally limited to 8-bit resolution with conversion speeds of 10 – 40 Ms/s using CMOS technology. The disadvantages of the Flash ADC are the area and power requirements of the $2^N - 1$ comparators. The speed is limited by the switching of the comparators and the digital logic.

Differential comparator is generally used for the operation. Different encoders are used for converting thermometer code to binary, like ROM encoder, FAT 32 tree encoder. Flash ADC is used in other ADCs also like Pipeline ADC, Sigma Delta ADC.

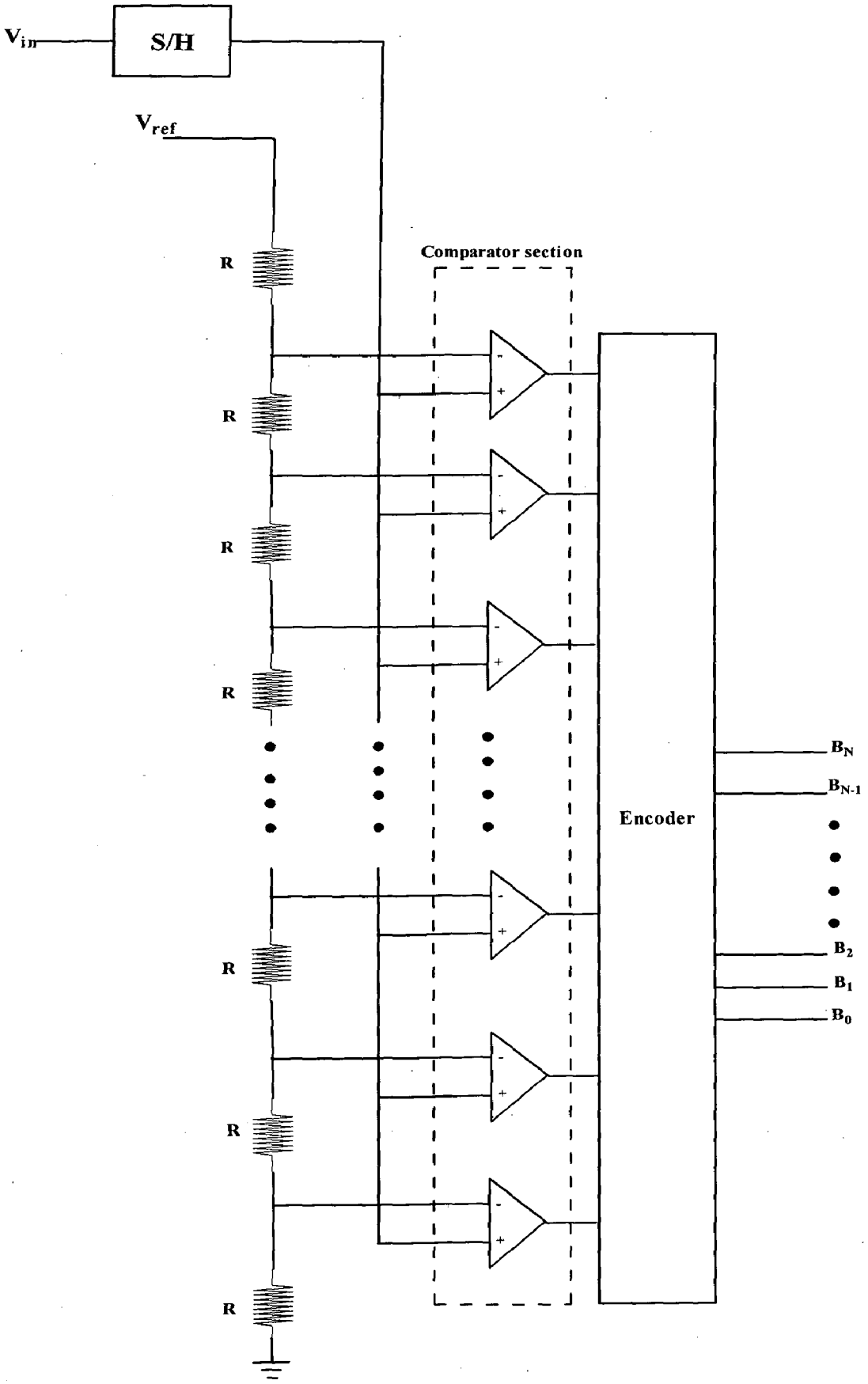


Figure 2.6. Flash ADC architecture

2.2.2. Pipelined ADC

The pipelined analog-to-digital converter is one of the most popular ADC architecture. It can work from few mega samples to more than hundreds of mega samples with resolution from 8 bit to 16 bits. Due to its high resolution and sampling rate it is widely used in medical and communication applications e.g. CCD imaging, ultrasonic medical imaging, digital receiver, base station, digital video (for example, HDTV), xDSL, cable modem, and fast Ethernet. Speed, resolution, power and dynamic performance are greatly improved in Pipeline ADC but SAR and integrating architectures are still used for low sampling rate applications, whereas for high sampling rate Flash ADC is still the choice. The block diagram of Pipelined ADC is shown in the figure below

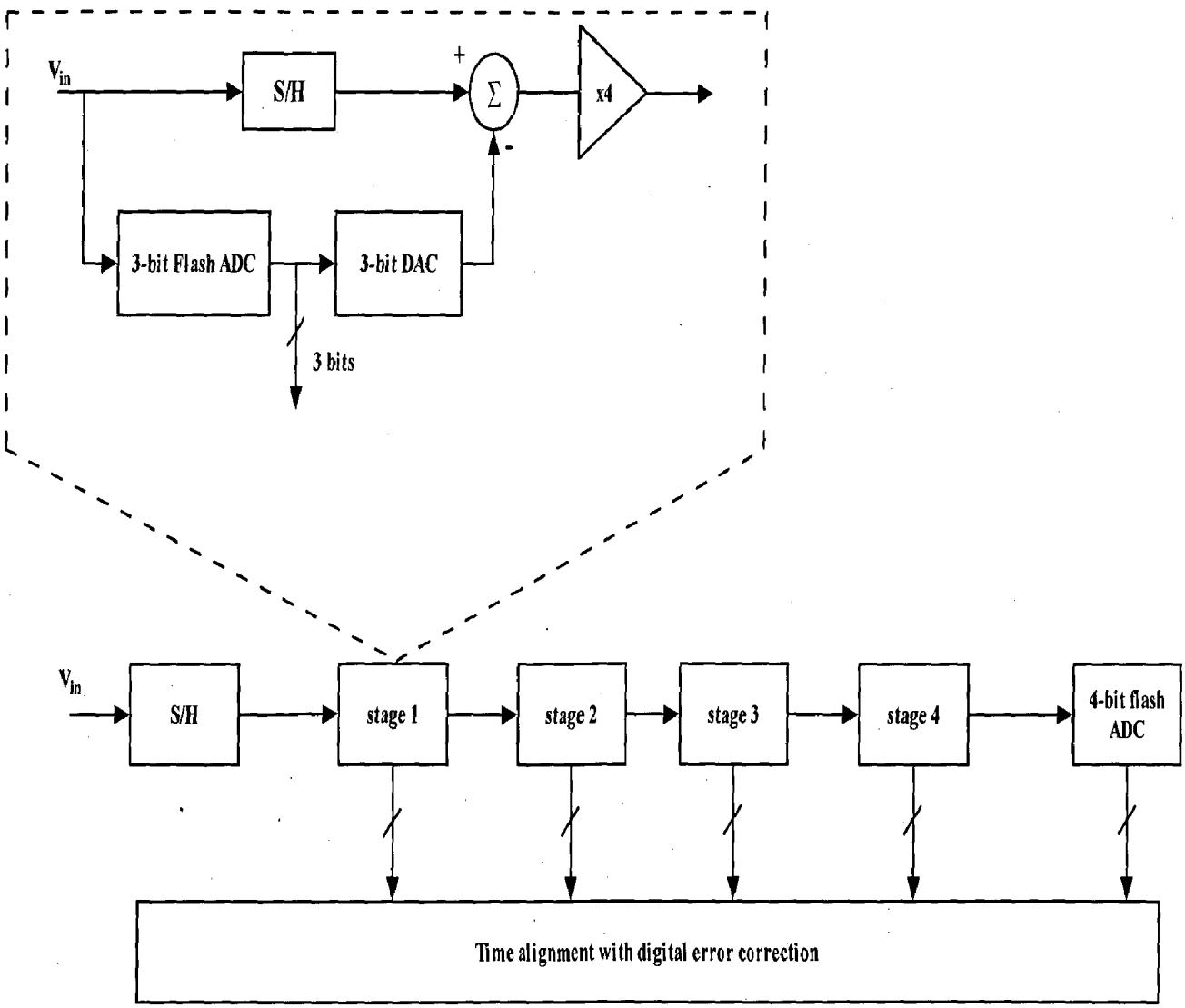


Figure 2.7. Pipelined ADC architecture

Initially sample-and-hold (S/H) circuit samples and holds the input voltage. The flash ADC in the first stage will convert this signal into 3 bit digital output. This 3 bits digital code is applied to DAC and the analog output is subtracted from the original signal, the remainder is then multiplied by 4 and then applied to the next stage. This process will continue till the last stage (stage 4) and every stage provides 3 bits. After last stage the amplified remainder will feed into 4 bit Flash ADC that will generate 4 least significant bits. As every stage generates bits at different instants of time therefore it is required to align all the bits by shift register prior to applying 12-bit digital output to the digital-error-correction logic. During the interval when one stage completes the processing of one sample and passes the magnified remainder to the other stage. The next stages are also performing the same operation because sample and hold circuit is embedded in every stage. This pipelining technique increases the throughput.

2.2.4. Integrating ADCs[4]

The integrating architecture is low speed, low cost, and high resolution, making it ideal for devices like digital multimeters and temperature sensors. An integrating converter integrates the input signal and correlates the integration time with a digital counter. The output of the counter is proportional to the amplitude of the sample. A single-slope converter samples the input and then simultaneously resets the counter and begins integrating a reference voltage. Since the reference voltage is dc, the output of the integrator starts at zero and linearly increases with a slope that depends on the gain of the integrator.

When the integrator output exceeds the sample voltage, a comparator switches state causing the counter output to be latched. The single-slope converter has many disadvantages that make it unappealing when compared to other architectures. Speed is a major concern, the singleslope converter requires 2^N clock pulses to perform a full scale conversion. To accomplish a conversion in a timely manner, the clock driving the digital counter must operate at a frequency much greater than the bandwidth of the input signal.

Another major disadvantage is accuracy; the accuracy of the converter is dependent on the precision of the passive components making up the integrator, the frequency jitter of the clock, and nonlinearities of the integrator's amplifier. One method of eliminating most of this error is to perform a dual integration of both the reference voltage and the input signal. In a dual-slope converter, the input sample (which is assumed to be negative) is integrated for a fixed time dictated by the digital counter.

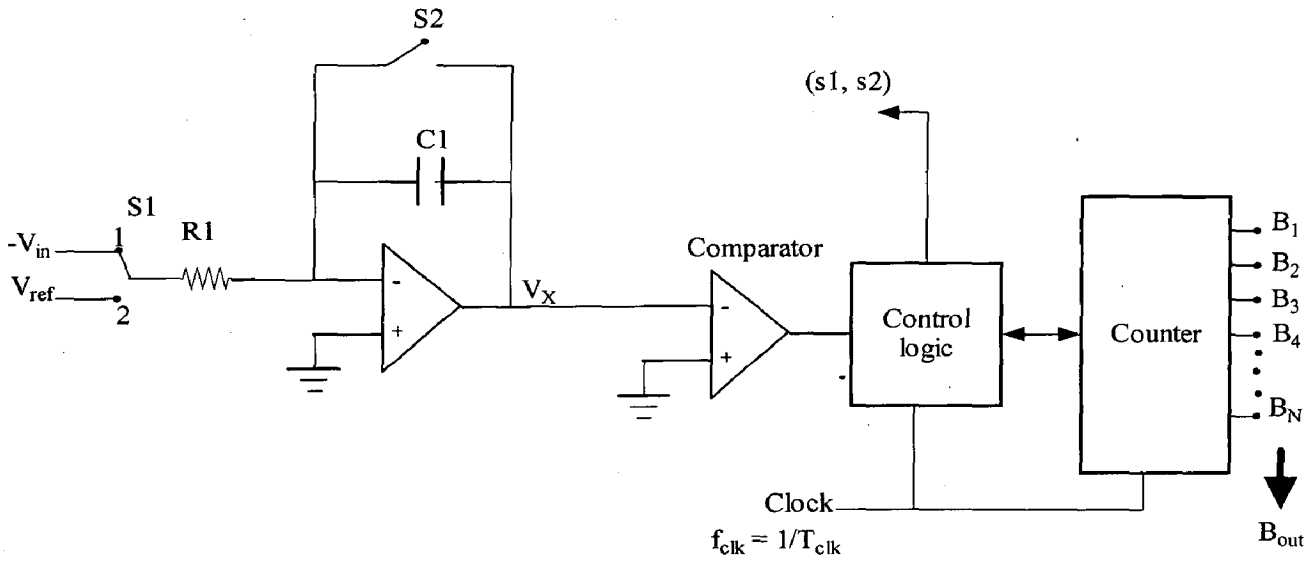


Figure.2.9. Dual slope ADC

When the counter overflows, a switch is thrown, a positive reference voltage is connected to the integrator, and the counter is simultaneously reset. When the integrator output reaches zero (fully discharged) a comparator switches state, thereby latching the counter output. The dual-slope converter is (worst case) twice as slow as the single-slope converter for the same number of bits due to the extra integration. However, the advantage to the dual-slope architecture is that the precision and nonlinearity issues that reduced the accuracy of the singleslope version are cancelled out because the same circuitry is used for both the reference voltage and the sample voltage integration. Figure 2.9 shows a block diagram of a dualslope converter.

2.2.5. Oversampling ADCs[9]

The final architecture is the newest and by far the most complex and is typically found in relatively low-speed, high-resolution applications like digital audio. All of the architectures we've previously discussed are called sampling converters because they sample near the Nyquist frequency (twice the maximum frequency component of the input signal). Oversampling converters, as the name implies, sample at a rate much higher than the input signal bandwidth and are used when high resolutions are required. Oversampling converters bypass the problems of the other converter architectures by using digital processing techniques in place of complex analog components. Also, because of the higher sampling rates, only basic antialiasing circuitry needs to be used and no S/H is required. The input signal bandwidth is so much lower than the sampling frequency that a simple single-pole low-pass filters will prevent aliasing in most applications. Oversampling converters were once slower than most sampling converters, but in recent years, their speed has improved with the advent of better mixed-signal manufacturing processes.

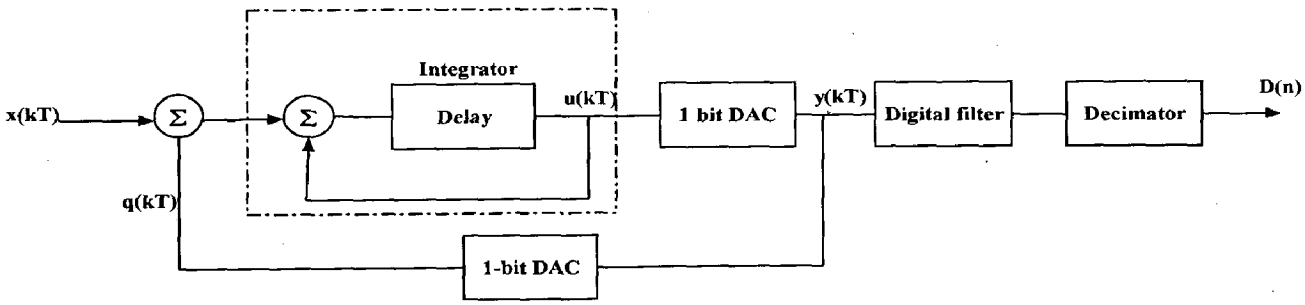


Figure.2.10. Sigma Delta ADC

Two components make up an oversampling converter: a digital filter and a delta-sigma ($\Delta\Sigma$) modulator [also called a sigma-delta ($\Sigma\Delta$) modulator]. The $\Delta\Sigma$ modulator provides quantization in the form of a pulse-density modulated signal. The density of the pulses represents the average value of the signal over a specified period. The more pulses per period (samples), the higher the resolution of the converter. The inner workings of a $\Delta\Sigma$ modulator are very complex; only the fundamentals of operation depicted in figure 2.10 are described. The oversampled analog signal goes through an integrator whose

output drives a comparator (a 1-bit ADC) that, in turn, drives a 1-bit DAC in a feedback loop. Through a series of iterations, the integrator, comparator, DAC, and summing junction produce a serial bitstream that represents the oversampled input voltage. Once digitized, the oversampled signal goes through a digital filter to remove frequency components at or above the Nyquist frequency. A decimator then removes the oversampled data (e.g., if the input is sampled at 64 times the Nyquist frequency, 1 bit will be retained for every 64 received). The final output is a B-bit serial stream (for a B-bit converter).

One big advantage of the oversampling architecture is that the quantization noise is pushed out of the signal bandwidth. This process of noise shaping allows the converter to obtain very high resolutions. If the order of the modulator is increased, the noise is pushed farther away from the input signal spectrum, allowing even higher resolutions but at the expense of exponentially increasing circuit complexity. The accuracy achieved by oversampling converters and their throughput makes them popular choices.

2.3. Architecture Tradeoffs

ADCs can be implemented by employing a variety of architectures. The principal tradeoffs between these alternatives[4] are:

The time it takes to complete a conversion (conversion time). For flash converters, the conversion time does not change with increased resolution. The conversion time for Successive Approximation Register (SAR) or Pipelined converters increases approximately linearly with an increase in resolution. For integrating ADCs, the conversion time doubles with every bit increase in resolution.

Component matching requirements in the circuit. Flash ADC component matching typically limits resolution to around 8-bits. Component matching requirements double with every bit increase in resolution. This applies to Flash, Successive approximation or Pipelined converters, but not integrating converters. For integrating converters, component matching does not increase with an increase in resolution.

Die size, cost and power. For Flash converters, every bit increase in resolution almost doubles the size of the ADC core circuitry. The power also doubles. In contrast, a SAR, Pipelined, or sigma-delta ADC die size will increase linearly with an increase in resolution, and an integrating converter core die size will not materially change with an increase in resolution (Figure 2.12). An increase in die size increases cost.

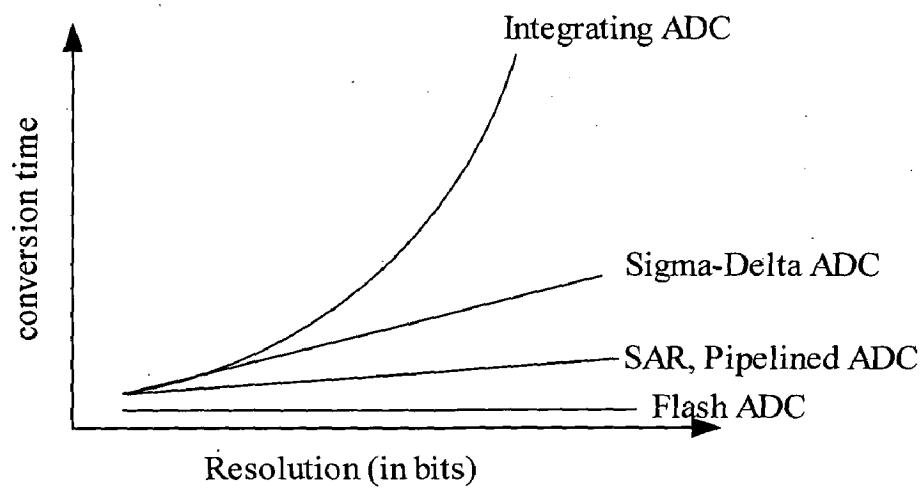


Figure 2.11. Tradeoff between conversion time and resolution in ADCs

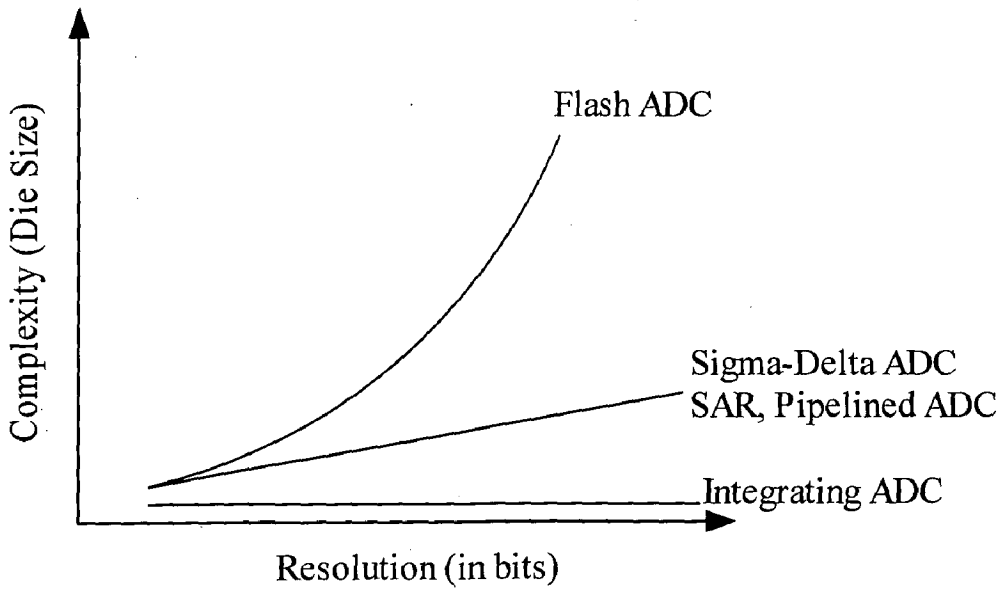


Figure 2.12. Tradeoff between complexity and resolution in ADCs.

2.3.1. Flash vs. Successive Approximation Register (SAR) ADC

In a SAR converter, the bits are decided by a single high-speed, high-accuracy comparator one bit at a time (from the MSB down to the LSB), by comparing the analog input with a DAC whose output is updated by previously decided bits and thus successively approximates the analog input. This serial nature of the SAR limits its speed to no more than a few Msps, while Flash ADCs exceed them.

SAR converters are available in resolutions up to 16-bits. Flash ADCs are typically limited to around 8-bits. The slower speed also allows the SAR ADC to be much lower in power The SAR architecture is also less expensive. Package sizes are larger for Flash converters. In addition to a larger die size requiring a larger package, the package needs to dissipate a lot of power and needs many pins for power and ground signal integrity.

2.3.2. Flash vs. Pipelined ADC

A Pipelined ADC employs a parallel structure in which each stage works on one to a few bits of successive samples concurrently. This improves speed at the expense of power and latency. However, each pipelined stage is much slower than a flash section. The pipelined ADC requires accurate amplification in the DACs and interstage amplifiers, and these stages have to settle to the desired linearity level. By contrast, in a flash ADC, the comparator only needs to be low offset and be able to resolve its inputs to a digital level (i.e., there is no linear settling time involved). However, some flash converters require preamplifers to drive the comparators. Gain linearity needs to be carefully specified.

Pipelined converters are capable of conversion speeds of around 100Msps at 8 to 14-bit resolutions. For a given resolution, Pipelined ADCs are around 10 times slower compared to flash converters of similar resolution. Pipelined converters are possibly the optimal architecture for ADCs that need to sample at rates up to around 100Msps with resolution at 10-bits and above. At resolutions of up to 10-bits, and conversion rates above a few hundred Msps, flash ADCs dominate. Interestingly, there are some situations where flash ADCs are hidden inside a converter employing architecture to increase its speed.

2.3.3. Flash vs. Integrating ADC

Single, dual and multi-slope ADCs can achieve high resolutions of 16-bits or more are relatively inexpensive and dissipate less power. These devices support very low conversion rates, typically less than a few hundred samples per second. Most applications are for monitoring DC signals in the instrumentation and industrial markets. This architecture competes with sigma-delta converters.

2.3.4. Flash vs. Sigma-Delta ADC

Flash ADCs do not compete with this architecture because currently the achievable conversion rates differ by up to two orders of magnitude. The sigma-delta architecture is suitable for applications with much lower bandwidth[9,15], typically less than 1MHz, with resolutions in the 12 to 16-bit range. These converters are capable of the highest resolution possible in ADCs. They require simpler anti-alias filters (if needed) to bandlimit the signal prior to conversion.

They trade speed for resolution by oversampling, followed by filtering to reduce noise. However, these devices are not always efficient for multi-channel applications. This architecture can be implemented by using sampled data filters (also known as modulators) or continuous time filters. For higher frequency conversion rates the continuous time architecture is potentially capable of reaching conversion rates in the hundreds of Msps range with low resolution of 6 to 8-bits.

CHAPTER 3

SAMPLE AND HOLD CIRCUIT

In Analog to Digital conversion, continuous amplitude continuous time analog signal is first converted into continuous amplitude discrete time signal, this process is called as sampling. Quantization cannot be performed by ADC architecture in an infinitesimal amount of time. Thus, the amplitude of the discrete-time signal must be held constant for a sufficient amount of time after being sampled. This is accomplished by a sample and hold(S/H) circuit.

S/H circuit is an important analog building block, especially in data converter systems. S/H circuits are also often referred to as "track-and-hold" circuits. Normally, these two terms are synonymous except for a few particular switched-capacitor S/H circuits that do not have a phase where the output signal is tracking the input signal. In many cases, the use of a S/H circuit at the front of the data converter can greatly minimize errors due to slightly different delay times in the internal operation of the converter.

The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits. The simplest S/H circuit in MOS technology is shown in figure 3.3, where V_{in} is the input signal, M1 is a MOS transistor operating as the sampling switch, C_{hold} is the hold capacitor and V_{out} is the resulting S/H output signal.

The behavior of the S/H is analogous to that of a camera. Its main function is to "take a picture" of the analog signal and hold its value until the ADC can process the information. It is important to characterize the S/H circuit when performing data conversion. Ignoring this component can result in serious error, for both speed and accuracy can be limited by the S/H. Here, the analog signal is instantly captured and held until the next sampling period. However, a finite amount of time is required for the

sampling to occur. During the sampling period, the analog signal may continue to vary; thus, another type of circuit is called a track-and-hold, or T/H. Here, the analog signal is "tracked" during the time required to sample the signal. It can be seen that S/H circuits operate in both static (hold mode) and dynamic (sample mode) circumstances.

3.1 The MOSFET Switch

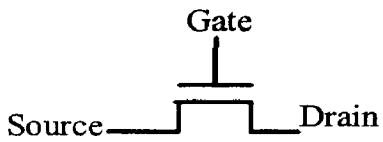


Figure 3.1. A MOSFET used as a switch

A fundamental component of any dynamic circuit (analog or digital) is the switch (figure. 3.1). An important attribute of the switch, in CMOS is that under dc conditions the gate of the MOSFET does not draw a current. Therefore, neglecting capacitances from the gate to the drain/source, we find that the gate control signal does not interfere with information being passed through the switch. Figure 3.2 shows the small-signal resistance of the switches plotted against drain-source voltage. The benefits of using the CMOS transmission gate are seen from this figure, namely, lower overall resistance. Another benefit of using the CMOS TG is that it can pass logic high or a logic low without a threshold voltage drop. The largest voltage an n-channel switch can pass is V_{DD} - V_{THN}, while the lowest voltage a p-channel switch can pass is V_{THP}.

In most circuits, a capacitor is used to store the analog voltage and an electronic switch or gate is used to alternately connect and disconnect the capacitor from the analog input. The rate at which this switch is operated is the sampling rate of the system.

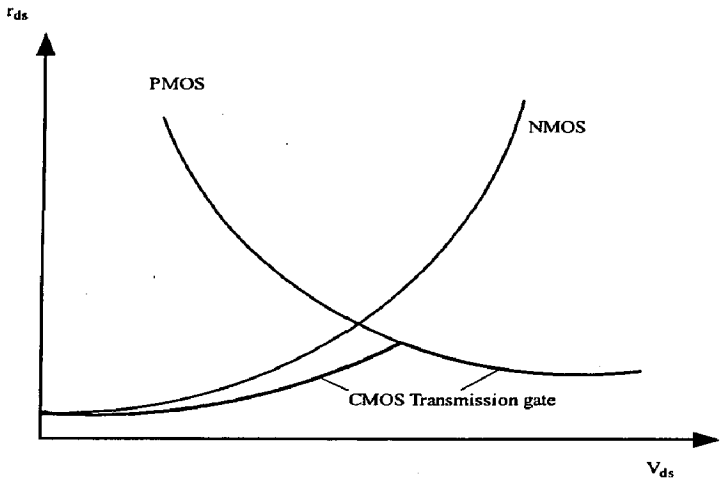


Figure 3.2. Small signal resistances of switches[15]

The necessity of such a circuit is easy to see if one considers what would happen if it were not present. In some kinds of ADC for example, the input is often compared to a voltage generated internally from a digital-to-analog converter. The circuit tries a series of values, and stops converting once the voltages are "the same" within some defined error margin. If the input value was permitted to change during this comparison process, the resulting conversion would be inaccurate, and possibly completely unrelated to the true input value. Such successive approximation ADCs will often incorporate internal S/H circuitry.

In the highest speed, moderate-resolution (8-10 bit) fully parallel (flash) converters, the use of an input S/H circuit avoids sensitivity of the conversion to mismatches in clock distribution to the large number of comparators, mismatches in delay through comparator input stages, and RC delays in the input resistor ladder. In multistep converter architectures, the need for an input S/H function is even more important because of the delays associated with quantizing the input in two or more stages. As yet, monolithic implementations of S/H systems that meet the stringent requirements for high-speed systems are complex in design and are usually fabricated in hybrid technologies.

S/H circuits are often used when multiple samples need to be measured at the same time. Each value is sampled and held, using a common sample clock. In order that the input

voltage is held constant for all practical purposes, it is essential that the capacitor has very low leakage, and that it is not loaded to any significant degree which calls for a very high input impedance.

3.2. Open Loop and Closed Loop Topologies

Two basic circuit configurations commonly used to implement S/H circuits are the open-loop and closed-loop topologies shown in figures 3.3 and 3.4, respectively. The open-loop architecture potentially offers the fastest implementation of the sampling function[5,7]. In its simplest form, an open-loop S/H circuit consists of a switch, shown implemented with MOS pass transistor M1, which samples the input onto a hold capacitance C_{hold}.

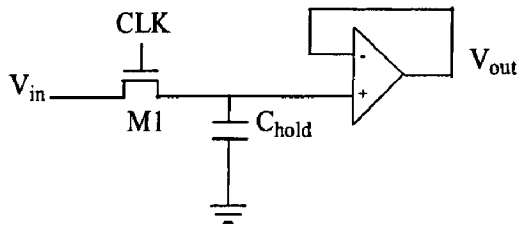


Figure.3.3. Open loop S/H circuit[1]

A high-input-impedance unity-gain amplifier buffers the hold capacitance and provides a low-impedance output node that drives the succeeding circuitry. During the sample mode, the sampling switch M1 is closed and the voltage across capacitor charges to V_{in}. However, in the transition from the sample mode to the hold mode, the turn-off of the sampling switch results in charge injection effects that introduce a pedestal error at the output. In designs where a MOS transistor functions as the sampling switch, input-dependent charge injection associated with the fast turn-off of the switch is often the principal source of sampling error. This pedestal error results in gain error and introduces nonlinearity that distorts the sampled signal. Open-loop architectures potentially provide the fastest possible sampling. The performance of a monolithic open-loop circuit may be severely limited by the characteristics of a MOS sampling switch pedestal error induced by charge injection in the switch, and is likely to limit the achievable precision.

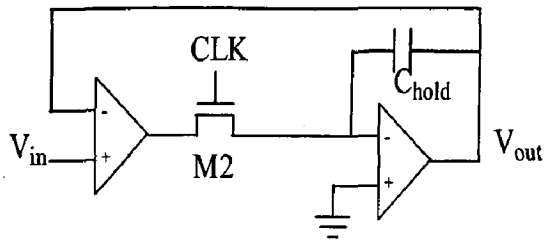


Figure.3.4. Closed loop architecture[18]

Closed-loop architectures avoid input-dependent charge injection during turn-off of the sampling switch. In this circuit, the sampling switch is always at virtual ground during sampling. This ensures that the charge injection and corresponding hold pedestal are independent of the input. However, the use of a closed-loop configuration entails a trade-off between speed and precision governed by the gain and bandwidth of the loop transfer function. Since the feedback loop in figure 3.4 encompasses two high-gain stages and an adequate phase margin is required for good settling characteristics, the operating bandwidth of this configuration may be low. Potential disadvantages of a closed-loop approach thus typically include long acquisition time, limited input bandwidth, and increased design complexity. Unfortunately, in reality, the performance of this S/H circuit is not as ideal two major types of errors, charge injection and clock feedthrough are associated with this S/H implementation.

3.3. Charge Injection

When a MOS switch is on, it operates in the triode region and its drain-to-source voltage, V_{DS}, is approximately zero. During the time when the transistor is on, it holds mobile charges in its channel. Once the transistor is turned off, these mobile charges must flow out from the channel region and into the drain and the source junctions as depicted.

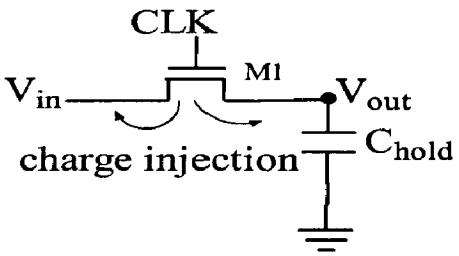


Figure 3.5.Channel injection in MOSFETs

For the S/H circuit in figure 3.5, if the MOS switch, M1, is implemented using an NMOS transistor, the amount of channel charge, Q_{ch}, this transistor can hold while it is on is given[18] by equation 3.1,

$$Q_{ch} = -WLC_{OX}(V_{DD} - V_{tn} - V_{in}) \tag{3.1}$$

where, W and L are the channel width and channel length of the MOS transistor, C_{ox} is the gate oxide capacitance, and V_{tn} is the threshold voltage of the NMOS device. When the MOS switch is turned off, some portion of the channel charge is released to the hold capacitor, C_{hold}, while the rest of the charge is transferred back to the input, V_{in}. The fraction, k, of the channel charge that is injected onto C_{hold} is given by equation 3.2,

$$\Delta Q_{ch} = kQ_{ch} = -kWLC_{OX}(V_{DD} - V_{tn} - V_{in}) \tag{3.2}$$

As a result, the voltage change at V_{out} due to this charge injection is given by equation 3.3,

$$\Delta V_{out} = \frac{\Delta Q_{ch}}{C_{hold}} = \frac{-kWLC_{OX}(V_{DD} - V_{tn} - V_{in})}{C_{hold}} \tag{3.3}$$

If half of the charge injects into the load, then k=1/2 and since, V_{tn} is given by

$$V_{tn} = V_{tn0} + \gamma(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}) \tag{3.4}$$

Notice that ΔV_{out} is linearly related to V_{in} and V_{tn}. However, V_{tn} is nonlinearly related to V_{in}. Therefore, charge injection introduces nonlinear signal-dependent error into the S/H circuit.

3.4 Clock Feedthrough

Clock feedthrough is due to the gate-to-source overlap capacitance of the MOS switch. For the S/H circuit of figure 3.3, the voltage change at V_{out} due to the clock feedthrough is given by equation 3.5,

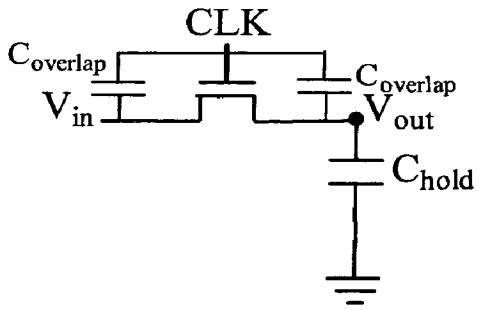


Figure 3.6. Clock feedthrough in MOSFETs

Where, $C_{overlap}$ is the parasitic capacitance. The error introduced by clock feedthrough is usually very small compare to charge injection. Also, notice that clock feedthrough is signal-independent[5,7] which means it can be treated as signal offsets that can be removed by most systems. Thus, clock feedthrough error is typically less important than charge injection.

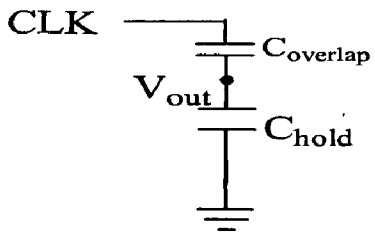


Figure 3.7. Capacitive voltage divider

From the capacitive network shown above, the expression for ΔV_{out} is given by

$$\Delta V_{out} = \frac{-C_{overlap} V_{DD}}{C_{overlap} + C_{hold}} \tag{3.5}$$

Charge injection and clock feedthrough are due to the intrinsic limitations of MOS transistor switches. These two errors limit the maximum usable resolution of any particular S/H circuit, and in turn, limit the performance of the whole system. New S/H techniques are developed to reduce these errors.

3.5. Reduction of Charge Injection and Clock Feedthrough

Many methods have been reported that reduce the effects of charge injection and capacitive feedthrough. One of the most widely used is the dummy switch[8], as seen in figure.3.8. Here, a switch with its drain and source shorted is placed in series with the desired switch M1. Notice that the clock signal controlling the dummy switch is the complement of the signal controlling M1, and in addition, should also be slightly delayed.

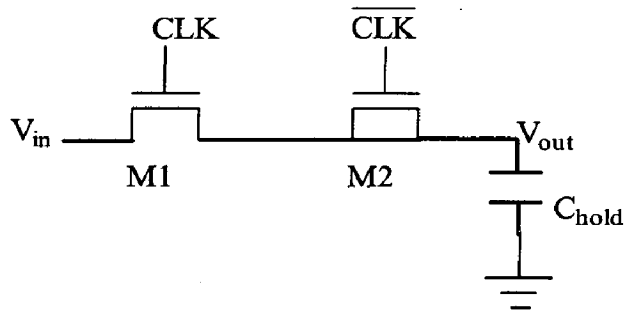


Figure.3.8. Dummy switch used to minimize charge injection

When M1 turns off, half the channel charge is injected toward the dummy switch, thus explaining why the size of M2 is one-half that of M1. Although M2 is effectively shorted, a channel can still be induced by applying a voltage on the gate. Therefore, the channel injected by M1 is essentially matched by the charge induced by M2, and the overall charge injection is canceled. Note what happens when M2 turns off. It will inject half of

its charge in both directions. However, since the drain and source are shorted and M1 is on, all the charge from M2 will be injected onto the low-impedance, voltage driven source which is also charging C_{hold}. Therefore, M2 charge injection will not affect the value of voltage on C_{hold}.

Another method used to counteract charge injection and clock feedthrough is to replace the switch with a CMOS transmission gate (TG). This will result in lower changes in V_{out}, because the complementary signals used will act to cancel each other. However, this approach requires precise control on the complementary clocks (the clocks must be switched at exactly the same time and assumes that the input signal, V_{in} will be small, since the symmetry of the turn-on and turn-off waveforms are dependent on the input signal. Hold pedestal error occurs because of charge injection and clock feedthrough, droop occurs because of leakage current.

CHAPTER 4

BASIC CIRCUITS OF FLASH ADC DESIGN

4.1. Common-Source Amplifier

Common source amplifier gives the highest gain among the three configurations, namely, common drain, common gate and common source.This amplifier is used when high input impedance is required. Simple current mirrors are used in a single-stage amplifier with an active load, as shown in figure[9] below.

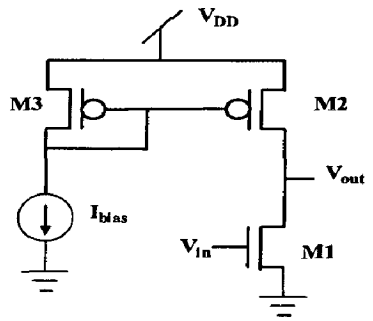


Figure.4.1. Current mirror with active load

Here, an n-channel common-source amplifier has a p-channel current mirror used as an active load to supply the bias current for the drive transistor. By using an active load, a high-impedance output load can be realized without using excessively large resistors or a large power-supply voltage. As a result, for a given power-supply voltage, a larger voltage gain can be achieved using an active load than would be possible if a resistor were used for the load. For example, if a 1 MΩ load were required with a 100 μA bias current, a resistive-load approach would require a power-supply voltage of 1 MΩ x 100 μA = 100 V. An active load makes use of the nonlinear, large-signal transistor equations to create simultaneous conditions of large bias currents and large small signal resistances.

A small-signal equivalent circuit for low-frequency analysis of the common-source amplifier of figure. 4.1 is shown in figure. 4.2. V_{in} and R_{in} are the Thevenin equivalent of

the input source. It is assumed that the bias voltages are such that both transistors are in the active region.

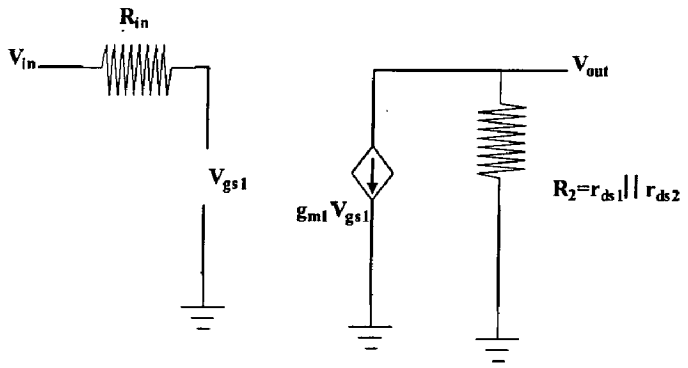


Figure.4.2. Small signal equivalent of common source amplifier

The output resistance, R_2, is made up of the parallel combination of the drain-to-source resistance of M1, that is, r_{ds1}, and the drain-to-source resistance of M2, that is, r_{ds2}. The voltage-controlled current source modelling the body effect has not been included since the source is at a small-signal ground, and, therefore, this source always has zero current.

Using small-signal analysis, we have $v_{gs1} = v_{in}$ and, therefore,

$$A_V = \frac{V_{out}}{V_{in}} = -g_{m1}R_2 = -g_{m1}(r_{ds1} \,||\, r_{ds2}) \tag{4.1}$$

Depending on the device sizes, currents, and the technology used, a typical gain for this circuit is in the range of -10 to -100. To achieve similar gains with resistive loads, much larger power-supply voltages must be used. This resistive-load approach also greatly increases the power dissipation. However, it should be mentioned here that for low-gain, high-frequency stages, it may be desirable to use resistor loads (if they do not require much silicon area) because they often have less parasitic capacitances associated with them. They are also typically less noisy than active loads.

4.2. Differential amplifier

The differential amplifier is among the most important circuit inventions, dating back to vacuum tube era. Offering many useful properties, differential operation has become dominant choice in today's high-performance analog and mixed-signal circuits.

Amplifiers can be used for high gain, but the dc gain cannot be obtained by amplifiers. For this special purpose, an amplifier was designed which could amplify the dc voltage also. A single ended input has low noise performance than the differential one. so, differential amplifiers are gaining popularity.

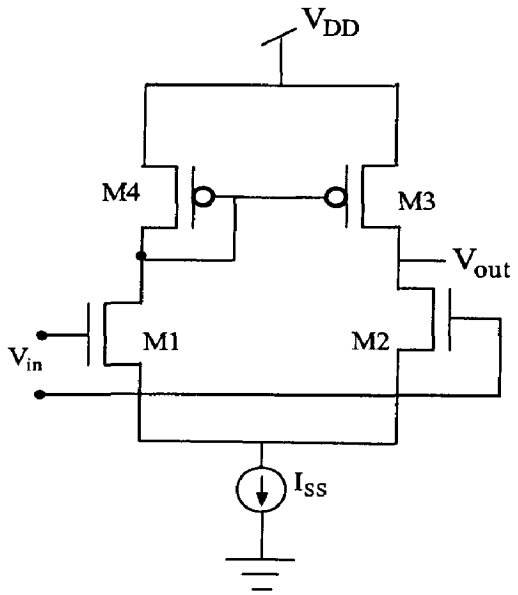


Figure.4.3. Differential amplifier[8]

4.2.1. Single-ended and differential operation

A single-ended signal is defined as one that is measured with respect to a fixed potential, usually the ground. A differential signal is defined as one that is measured between two nodes that have equal and opposite signal excursions around a fixed potential. In the strict sense, the two nodes must also exhibit equal impedances to that potential. The "center" potential in differential signaling is called the "common-mode" (CM) level.

An important advantage of differential operation over single-ended signaling is higher immunity to "environmental" noise. Differential amplifier rejects common mode noise and increases the output voltage range. Gain also doubles for differential output.

While it may seem that differential circuits occupy twice as much area as single-end alternatives, in practice this is a minor drawback. Also, the suppression of nonideal effects by differential operation often results in a smaller area than that of a brute-force single-end design. Furthermore, the numerous advantages of differential operation by far outweigh the possible increase in the area.

If both the inputs are at constant level, then the current I_{SS} divide equally between two transistors. If the inputs are unequal, then current through the transistor are different. The overall gain of differential amplifier is given by

$$A_V = g_{m1}(r_{d3} \| r_{d4}) \tag{4.2}$$

And the maximum differential input is given by

$$V_{DIMAX} = \sqrt{\frac{2I_{SS}}{\beta}} \tag{4.3}$$

4.3. Source follower

Source follower is also called as common drain amplifier. This amplifier is used for impedance matching purpose, this amplifier has a voltage gain of maximum of unity , but has current gain greater than unity. This amplifier is generally used in the second stage of operational amplifiers. The circuit diagram of source follower[9] is shown below and its gain is given by the equation below.

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} \tag{4.4}$$

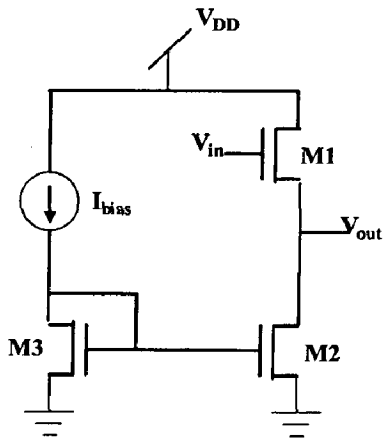


Figure.4.4. Source Follower

4.4. Current mirror

We need current sources for the operation of the circuits, but practically we do not have current sources. So, to solve this problem we use current mirror. In current mirrors, reference current is established and it is reflected accordingly to other branches. Ideally, the output resistance of current mirror is infinity, due to finite output impedance of MOSFETs, the current mirror has finite output impedance.

A simple current mirror[6] is shown below

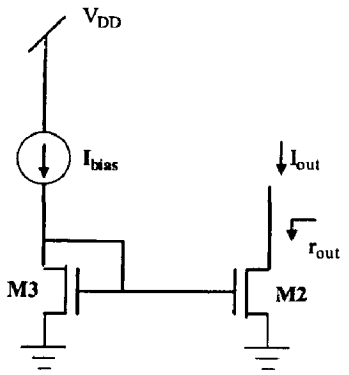


Figure.4.5. Simple current mirror

The output impedance is given by

$$r_{out} = r_{ds2} \tag{4.5}$$

CHAPTER 5

PROPOSED FLASH ADC

Flash ADC consists of three section namely, S/H circuit followed by comparator section, which feeds the encoder. The S/H circuit tracks the input and holds it for the comparator input. The comparator gets two inputs namely, sampled value of input and reference voltage. It compares these two inputs and gives an output of logic one, when sampled value of input voltage is greater than reference voltage. The reference voltages are generated using a voltage divider network. The output of comparator section will be in thermometer code, but the final output is required in binary form. Encoder is used to convert thermometer code into binary code. Two stage op amp is used to realize an op amp.

5.1. S/H circuit

The S/H function is realized by designing an integrator circuit. It consists of two resistors one capacitor and an op amp. The circuit of S/H is shown below.

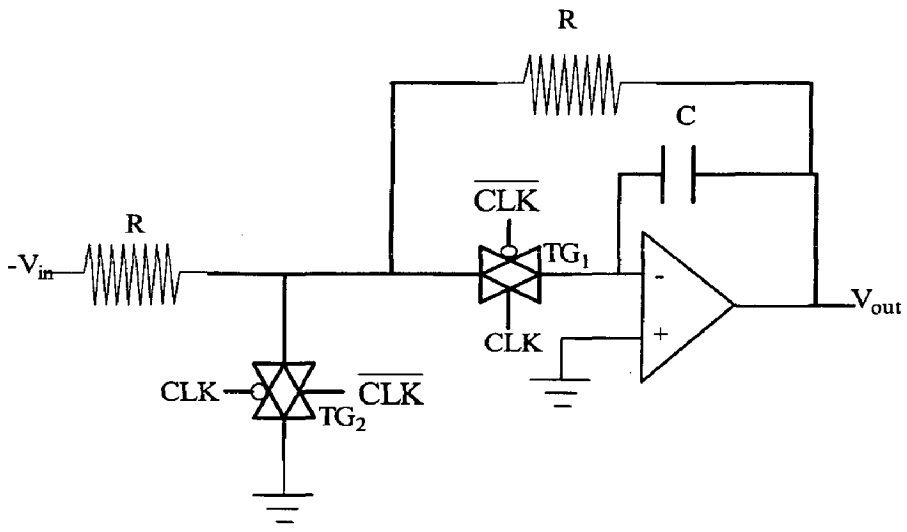


Figure 5.1. Proposed S/H circuit

When the CLK signal is high, then the TG_1 switches on and TG_2 switches off. The equivalent circuit diagram is given in the figure below.

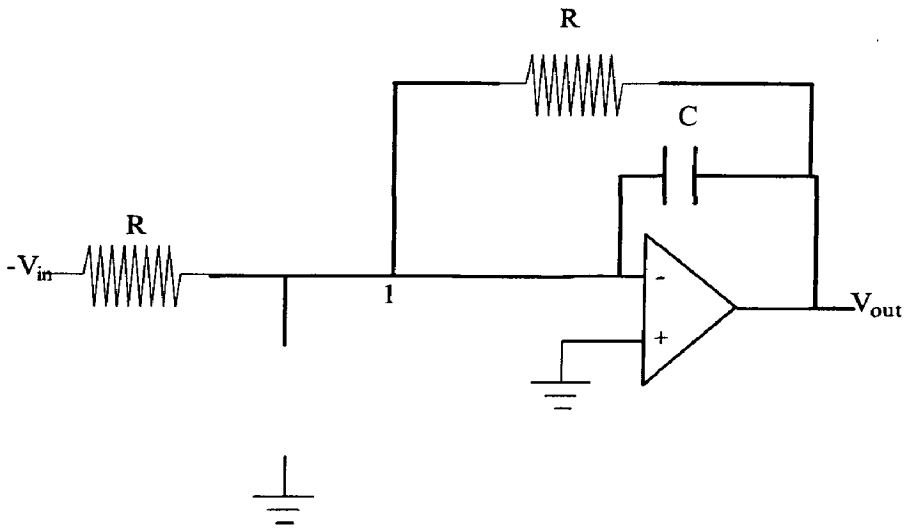


Figure. 5.2. Equivalent circuit of S/H, when CLK is high.

$$V_{out}=\frac{1}{RC}\int_0^t v_{in}dt \qquad (5.1)$$

For T = 1/RC, R and C are chosen such that T=1, when CLK is high, the circuit acts as the low pass filter and when CLK is at logic zero, then the output remains constant.

5.2. Comparator

Comparator circuit plays an important role in analog to digital conversion. As already stated in chapter 1, analog to digital conversion is converting a signal, which is continuous amplitude and time to a signal which is discrete in amplitude and time. The conversion of a continuous amplitude signal to discrete amplitude signal is done by comparator.

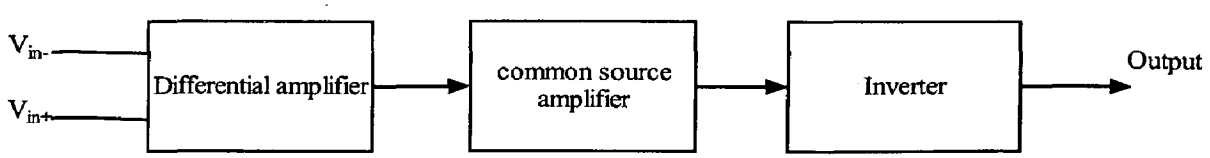


Figure.5.3. Block diagram of comparator

Comparator consists of three blocks, a differential amplifier followed by a common source amplifier and an inverter. Differential amplifier compares its two inputs, the output voltage is taken at node 1, when the input at V_{in-} increases the output decrease and when V_{in+} is greater than V_{in-}, then output voltage increases. The output voltage is proportional to the difference in input. This output voltage is amplified using common source amplifier which represents the output in the range of 0 to 0.7 V. An inverter circuit is used for decision making. When the output from common source amplifier is lager than 0.35V, inverter gives logic low, i.e. 0V and when the output of common source amplifier is less than 0.35V. It gives logic 1 output. Thus this circuit compares two voltages and gives the logic output accordingly.

The circuit diagram of comparator is shown in figure 5.3. To insure that no systematic input offset voltage exists, when the differential input voltage is zero. The output voltage of the first stage, V_{GS7} should be that which is required to make I_{D7} equal to its bias current, I_{D6}. Specifically the value of V_{GS7} should be given by

$$V_{GS7}=\sqrt{\frac{2I_{D6}}{\mu_n C_{ox}(W/L)_7}}+V_{tn} \qquad (5.1)$$

When the differential input voltage is zero, the drain voltages of both Q_3 and Q_4 are equal by arguments of symmetry. Therefore, the output voltage of the first stage, V_{GS7}, is given by

$$V_{GS7}=V_{DS3}=V_{GS4} \qquad (5.2)$$

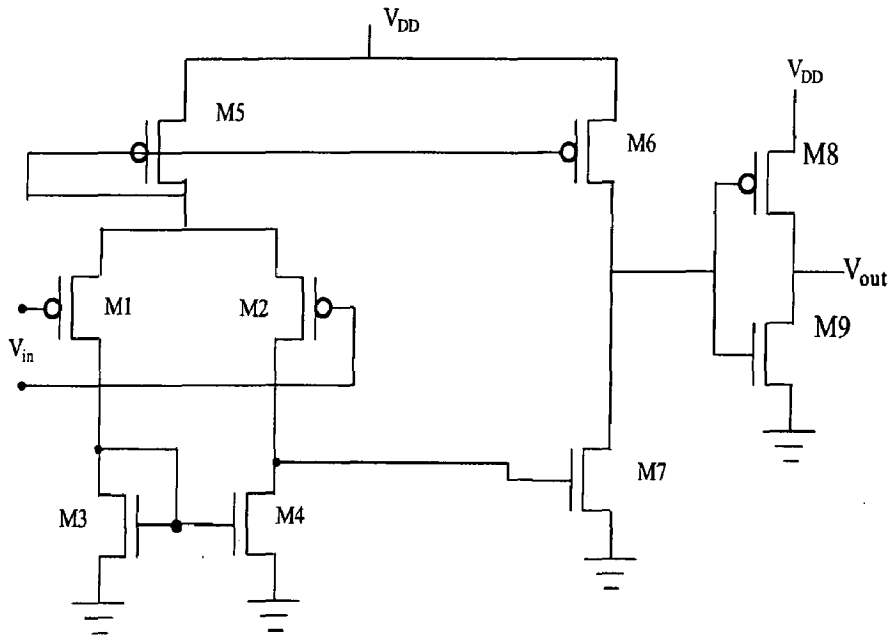


Figure.5.4. Comparator circuit

This value is the voltage necessary to cause I_{D7} to be equal to I_{D6}.However, the gate source voltage of Q_4 is given by

$$V_{GS4}=\sqrt{\frac{2I_{D4}}{\mu_n C_{ox}(W/L)_4}}+V_{tn} \tag{5.3}$$

So equating (5.1) and (5.3) to satisfy (5.2) results in

$$\sqrt{\frac{2I_{D4}}{\mu_n C_{ox}(W/L)_4}}=\sqrt{\frac{2I_{D7}}{\mu_n C_{ox}(W/L)_7}} \tag{5.4}$$

or,

$$\frac{I_{D4}}{(W/L)_4}=\frac{I_{D7}}{(W/L)_7} \tag{5.5}$$

This equality, when the current density of Q_4 is equal to the current density of Q_7, states that they both have the same effective gate-source voltages.

Since,

$$\frac{I_{D6}}{I_{D4}} = \frac{I_{D6}}{I_{D5}/2} = \frac{(W/L)_6}{(W/L)_5/2} \tag{5.6}$$

We see that the necessary condition to ensure that no input offset voltage is present is

$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5} \tag{5.7}$$

On taking l=70nm and V_{DD} as 0.7V. We get the maximum differential input voltage of 0.52V from the equation (4.3). This analysis ignores the voltage drop of the level-shifter output stage and channel length modulation. These effects cause only minor voltages and an offset voltage on the order of 10mV is obtained.

5.3. Encoder

Encoder converts the thermometer code into binary. The code is called thermometer code, because if one bit is at logic high, then all its lower bits are also at logic high.

The expression for conversion is given by

$B_3 = O_8$

$B_2 = O_4 \oplus O_8 \oplus O_{12}$

$B_1 = O_2 \oplus O_4 \oplus O_8 \oplus O_{10} \oplus O_{12} \oplus O_{14}$

$B_0 = (O_1 \oplus O_2)+(O_3 \oplus O_4)+(O_5 \oplus O_6)+(O_7 \oplus O_8)+(O_9 \oplus O_{10})+(O_{11} \oplus O_{12})+(O_{13} \oplus O_{14}) + O_{15}$

The ex-or gates and or gates are realized in CMOS technology.

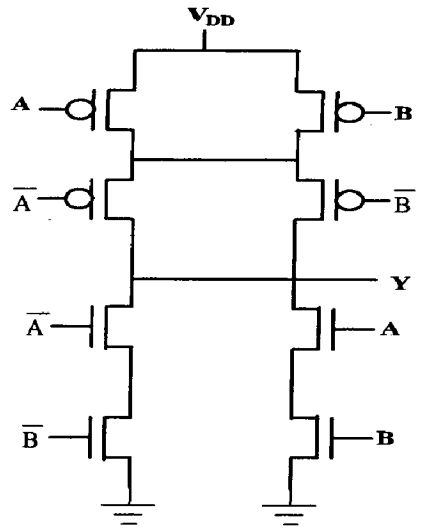


Figure.5.5. CMOS Ex-OR gate

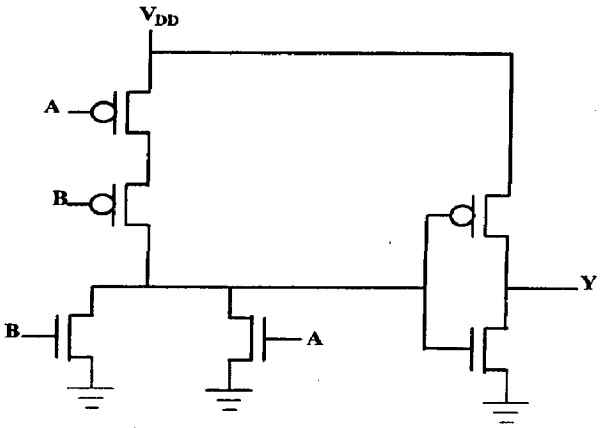


Figure.5.6. CMOS OR gate

Ex-OR gate has four inputs A, B, $\overline{A}$ and $\overline{B}$. Output is high when the inputs are complementary. When both the inputs are at same logic level, the output is at logic low. OR gate has two inputs A and B, the output is at logic 1, when atleast one of the inputs are at logic 1, else the output is at logic zero.

CHAPTER 6

SIMULATION RESULTS AND DISCUSSION

4 bit Flash ADC was designed and simulated in 70nm technology using Tanner spice. A 0.7V power supply was used and the maximum analog input was 0.52V, the results of S/H circuit, comparator and complete 4 bit flash ADC are presented. Proposed ADC dissipates a power of 10.3mW and has a conversion time of 0.99ns.

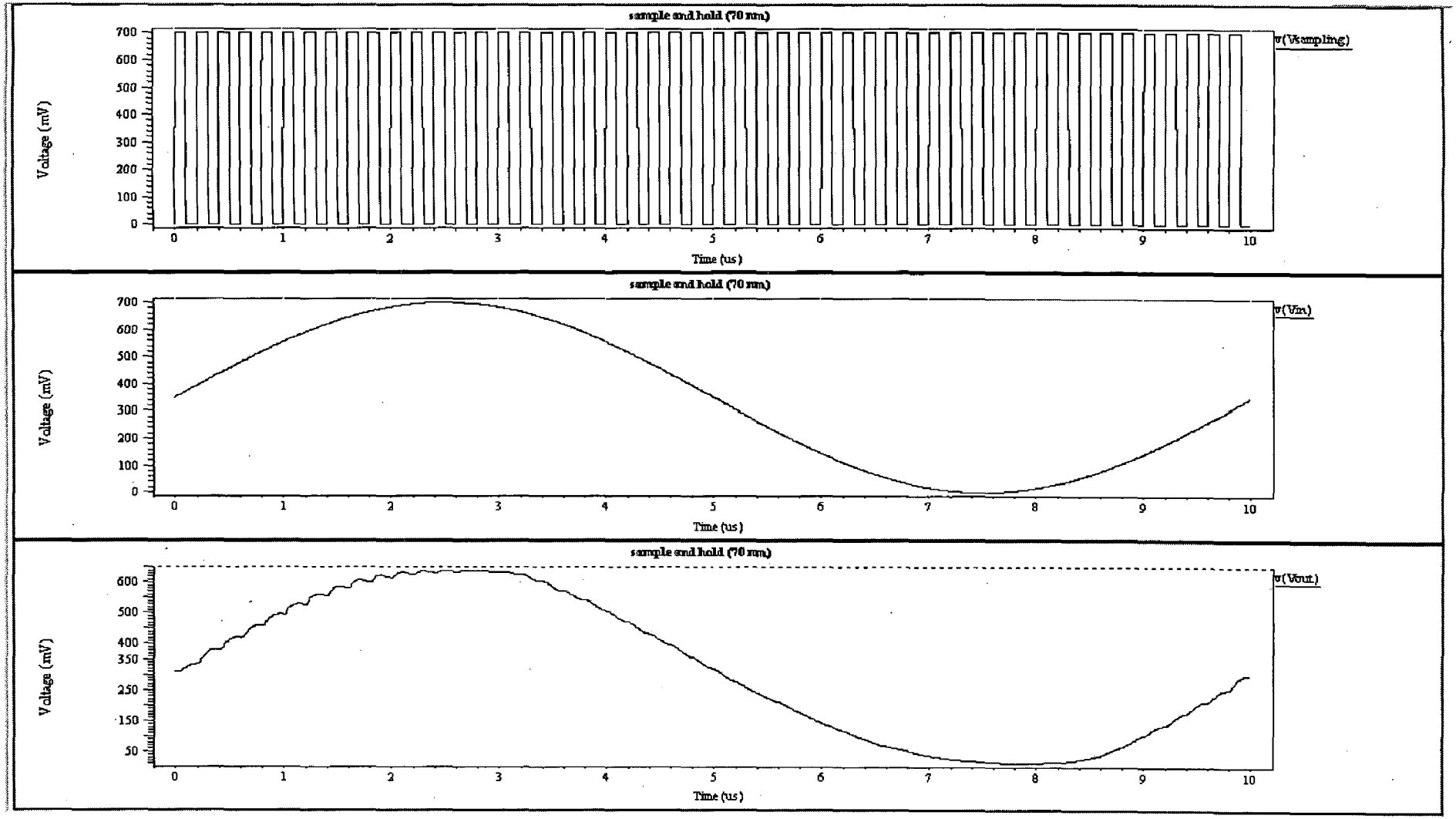
6.1. S/H circuit

S/H circuit was used for taking the sample of the waveform at regular intervals of time. The output of sample and hold circuit should follow the input signal, when the clock signal is high and the input voltage should be held constant, when the clock signal is low. The output waveform of S/H circuit is shown in waveform no.6.1. A sinusoidal input signal is applied, which has a frequency of 100kHz and peak to peak amplitude of 0.52V, the frequency of sampling signal is 100MHz, whose amplitude is $0.7V_{p-p}$. The output signal follows the input signal when the sampling signal is high, when the sampling signal is low, the output waveform is held at the input voltage.

The hold pedestal and droop rate obtained are 2.93mV and 0.8mV/μs respectively, these are obtained because of charge injection and clock feedthrough errors. Comparisons of these values are done with the available literature in the table below and hence the better performance of this circuit can be verified.

	[21]	This design
Hold Pedestal	4.8mV	2.93mV
Droop rate	1.0mV/μs	0.8mV/ μs

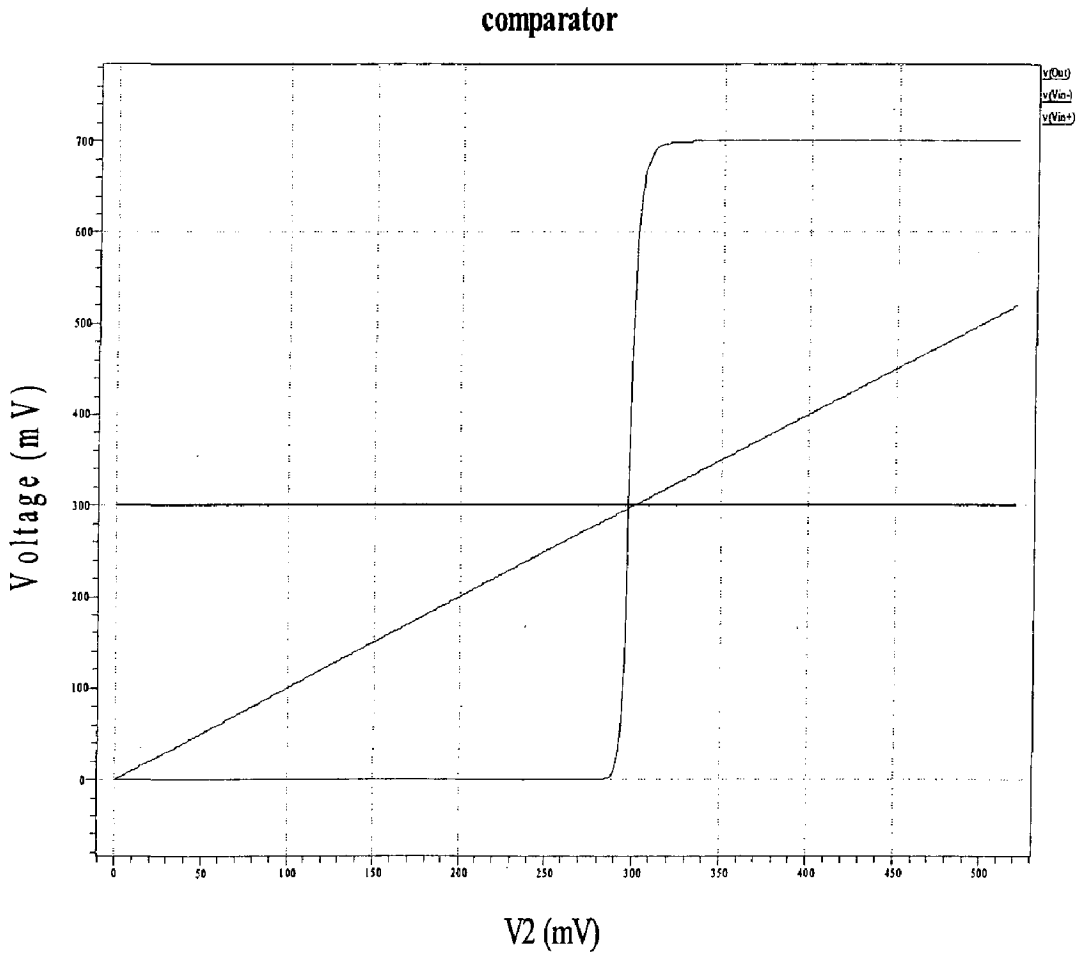
Table 6.1. Comparison of S/H parameters



Waveform no .6.1. Output of S/H Circuit

6.2. Comparator output

A comparator has two inputs, namely, sampled value of input voltage and reference voltage. It gives an output of logic high when input voltage is greater than the reference voltage. The input voltage is varied from 0 to 0.52 V. The reference voltage is fixed at 0.3 V. When the input voltage exceeds 0.3 V, the comparator should give high output. The finite offset voltage appears because of channel length modulation. The output of comparator is shown in waveform no.6.2 .The offset voltage of comparator is 8mV.



Waveform 6.2. Output waveform of comparator

6.3. 4 bit Flash ADC output

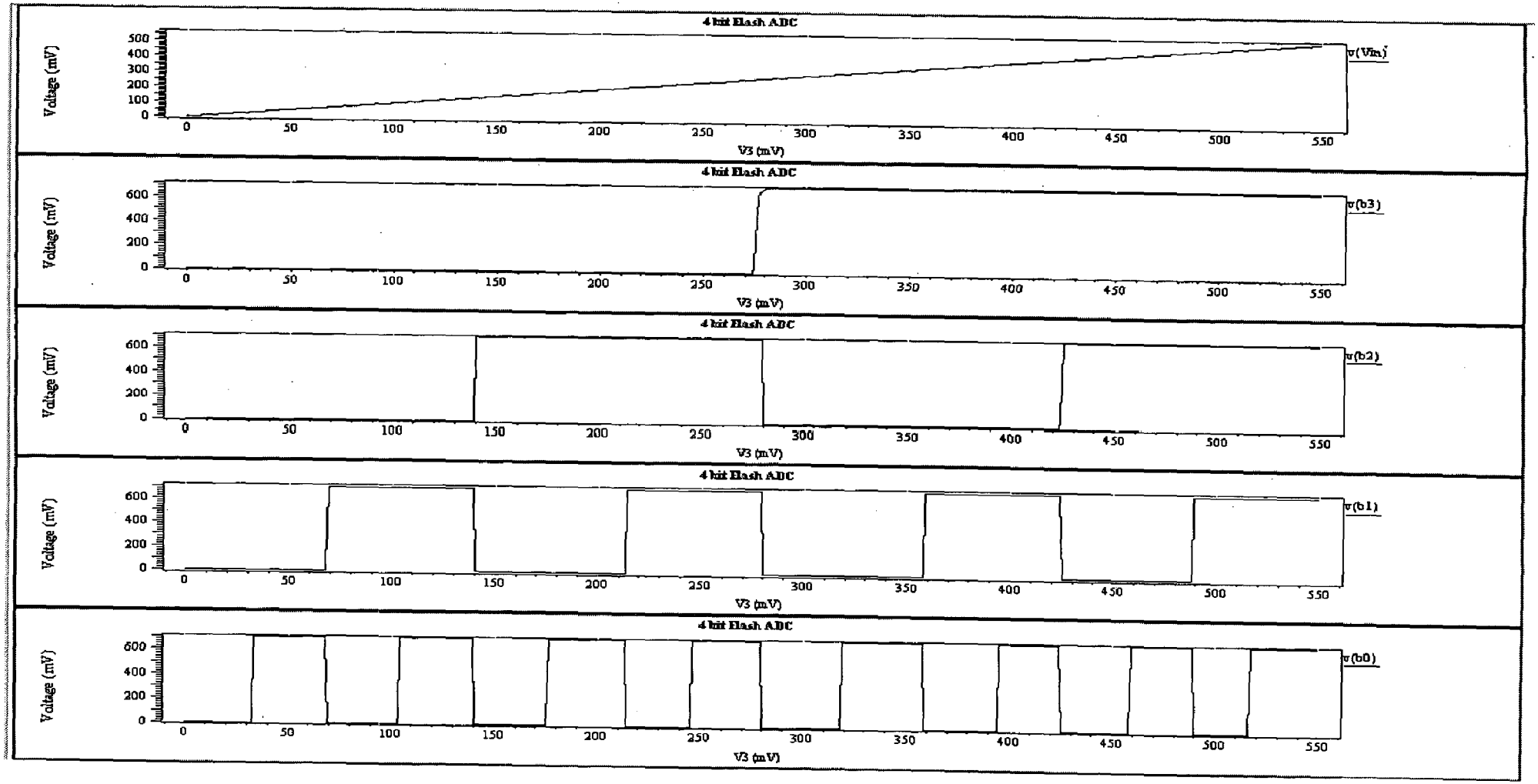
ADC converts an analog signal to digital code. In this thesis, the final output code is in binary. Since the resolution of ADC is 4, the full scale analog input is divided into 2^4 levels, i.e. 16 levels. The 4 bit binary code starts with 0000 and ends with 1111. An ideal 4 bit flash ADC should provide the codes from 0000 to 1111 for full scale input range. The output of Flash ADC is in accordance with the expected value and can be verified from the waveform 6.3. The staircase output waveform can also be verified from waveform 6.4. The performance parameters of proposed ADC can be verified, from the table below.

The simulation results are summarized in the table below:

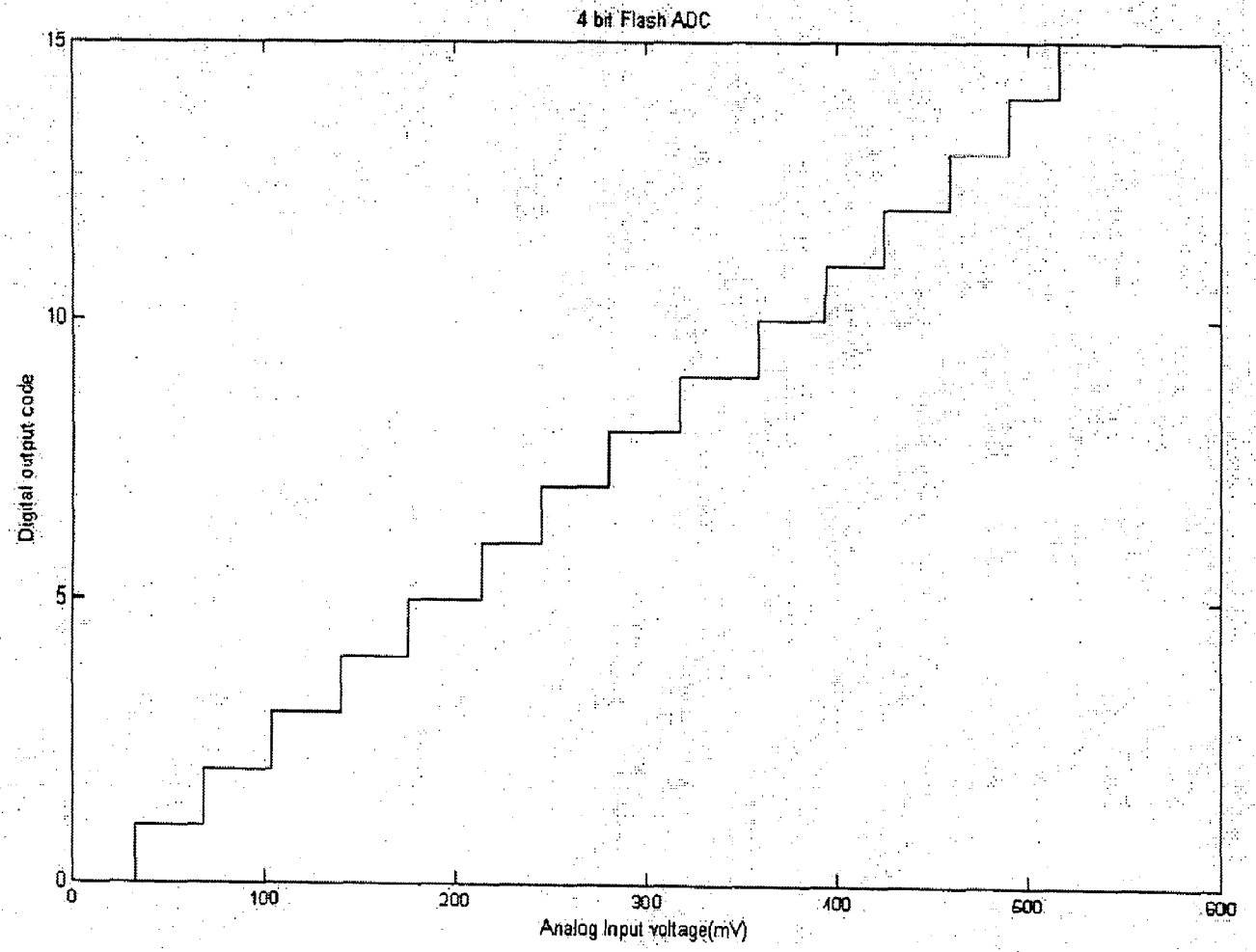
Parameters	Expected	Observed
Analog resolution	32.5mV	33mV
DNL Error	<0.5 LSB	0.2 LSB
INL Error	<0.5 LSB	0.4 LSB
Offset error	0	0
Missing code	0	0

Table 6.2. Comparison of ADC parameters

Thus the output of 4 bit flash ADC is in accordance with the expected values.



Waveform no.6.3. Output of 4 bit flash ADC



Waveform 6.4.Ouput of 4 bit flash ADC in Staircase form

CHAPTER 7

CONCLUSION AND FUTURE WORK

A 4 bit Flash ADC was designed and simulated in 70nm technology using tanner spice. 0.7V power supply was used. Maximum analog input range is 0.52V, since differential amplifier has a maximum limit on differential input. Zero missing codes are obtained indicates that output is almost ideal. DNL and INL errors are 0.26 LSB and 0.4 LSB respectively, are in the acceptable range of 0.5 LSBs, this error has occurred, because of channel length modulation. ADC has conversion time of 0.99ns and has a power dissipation of 10.6mW.

S/H circuit is realized and maximum sampling rate of 100MHz is obtained. The hold pedestal and droop rate are 2.93mV and 0.8mV/μs respectively. These errors are caused due to charge injection and clock feedthrough. Comparator is also realized and its offset voltage is 8mV.

Scope for Future Work

1. Flash ADC was designed in 70nm technology, it can be designed in 32nm technology.
2. The design can be done considering the channel length modulation parameter λ.
3. Layout of the Flash ADC can be done.
4. Bandgap current source can be designed for current sources.

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PUBLICATION

Anil N, A.K.Saxena, and S Dasgupta, "70nm low power low hold pedestal sample and hold circuit", Proceedings of the IEEE-ACVIT November 2007-(In Progress)

APPENDIX A

SPICE CODE FOR FLASH ADC

```
.probe
.options probefilename="diiferential.dat"
+ probesdbfile="C:\Documents and Settings\Anil\Desktop\lab work\diiferential.sdb"
+ probetopmodule="Module2"
```

A.1 Code for comparator

```
.SUBCKT offset_comp Out Vin+ Vin- Gnd Vdd
M1 Gnd c1 c1 Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M2 c3 c1 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M3 N9 N7 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M4 N10 N9 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M5 N11 N10 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M6 Out N6 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M7 N6 N11 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M8 c1 Vin- N5 N5 PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M9 N5 Vin+ c3 N5 PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M10 N5 N7 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M11 N9 c3 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M12 N10 N9 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M13 N11 N10 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M14 Out N6 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M15 N6 N11 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
R16 Vdd N7 1k TC=0.0, 0.0
R17 N7 Gnd 1.5k TC=0.0, 0.0
.ENDS
```

A.2 Code for comparator section

```
.SUBCKT comparator section Out1 Out2 Out3 Out4 Out5 Out6 Out7 Out8 Out9 Out10
+ Out11 Out12 Out13 Out14 Out15 Vin Vref Gnd Vdd
Xoffset_comp_1 Out14 Vin N3 Gnd Vdd offset_comp
Xoffset_comp_2 Out13 Vin N4 Gnd Vdd offset_comp
Xoffset_comp_3 Out11 Vin N6 Gnd Vdd offset_comp
Xoffset_comp_4 Out12 Vin N5 Gnd Vdd offset_comp
Xoffset_comp_5 Out10 Vin N7 Gnd Vdd offset_comp
Xoffset_comp_6 Out9 Vin N8 Gnd Vdd offset_comp
Xoffset_comp_7 Out8 Vin N9 Gnd Vdd offset_comp
Xoffset_comp_8 Out7 Vin N10 Gnd Vdd offset_comp
Xoffset_comp_9 Out15 Vin N2 Gnd Vdd offset_comp
Xoffset_comp_10 Out6 Vin N11 Gnd Vdd offset_comp
Xoffset_comp_11 Out5 Vin N12 Gnd Vdd offset_comp
Xoffset_comp_12 Out4 Vin N13 Gnd Vdd offset_comp
```

```
Xoffset_comp_13 Out3 Vin N14 Gnd Vdd offset_comp
Xoffset_comp_14 Out2 Vin N15 Gnd Vdd offset_comp
Xoffset_comp_15 Out1 Vin N16 Gnd Vdd offset_comp
R1 N15 N16 50 TC=0.0, 0.0
R2 N14 N15 50 TC=0.0, 0.0
R3 N13 N14 50 TC=0.0, 0.0
R4 N11 N12 50 TC=0.0, 0.0
R5 N12 N13 50 TC=0.0, 0.0
R6 N16 N1 50 TC=0.0, 0.0
R7 N4 N5 50 TC=0.0, 0.0
R8 Vref N2 50 TC=0.0, 0.0
R9 N3 N4 50 TC=0.0, 0.0
R10 N2 N3 50 TC=0.0, 0.0
R11 N9 N10 50 TC=0.0, 0.0
R12 N8 N9 50 TC=0.0, 0.0
R13 N7 N8 50 TC=0.0, 0.0
R14 N6 N7 50 TC=0.0, 0.0
R15 N5 N6 50 TC=0.0, 0.0
R16 N10 N11 50 TC=0.0, 0.0
v17 N1 Gnd 0.06751

.ENDS

* No Ports in cell: PageID_Tanner
* End of module with no ports: PageID_Tanner
```

A.3 Code for xor

```
.SUBCKT XOR2 A B Out Gnd Vdd
M1 N38 B Gnd Gnd NMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
M2 N38 A Gnd Gnd NMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
M6 Out B N7 Gnd NMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
M5 N7 A Gnd Gnd NMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
M9 Out N38 Gnd Gnd NMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
* Page Size:  5x7
* S-Edit  2-Input XOR Gate (TIB)
* Designed by: J. Luo  May 28, 2007  11:59:42
* Schematic generated by S-Edit
* from file C:\Documents and Settings\Anil\Desktop\lab work\diiferential / module
XOR2 / page Page0
M3 N38 B N36 Vdd PMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
```

```
M4 N36 A Vdd Vdd PMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
M7 N20 A Vdd Vdd PMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
M10B Out N38 N20 Vdd PMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
M8 N12 B Vdd Vdd PMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
M10 Out N38 N12 Vdd PMOS W='22*l' L='2*l' AS='66*l*l' AD='66*l*l' PS='24*l'
PD='24*l' M=1
.ENDS
```

A.4 Code for encoder

```
.SUBCKT b1 A2 A4 A6 A8 A10 A12 A14 b1 Gnd Vdd
XXOR2_1 N3 N2 N8 Gnd Vdd XOR2
XXOR2_2 N6 A14 N7 Gnd Vdd XOR2
XXOR2_3 A10 A12 N6 Gnd Vdd XOR2
XXOR2_4 A6 A8 N2 Gnd Vdd XOR2
XXOR2_5 A2 A4 N3 Gnd Vdd XOR2
XXOR2_6 N8 N7 b1 Gnd Vdd XOR2
.ENDS

.SUBCKT b2 A4 A8 A12 b2 Gnd Vdd
XXOR2_1 N4 A12 b2 Gnd Vdd XOR2
XXOR2_3 A4 A8 N4 Gnd Vdd XOR2
.ENDS

.SUBCKT Or A B Out Gnd Vdd
M1 N3 A Gnd Gnd NMOS L=70n W=22u AD=66p PD=24u AS=66p PS=24u
M2 Gnd B N3 Gnd NMOS L=70n W=22u AD=66p PD=24u AS=66p PS=24u
M3 Out N3 Gnd Gnd NMOS L=70n W=22u AD=66p PD=24u AS=66p PS=24u
M4 N3 B N2 N2 PMOS L=70n W=22u AD=66p PD=24u AS=66p PS=24u
M5 N2 A Vdd Vdd PMOS L=70n W=22u AD=66p PD=24u AS=66p PS=24u
M6 Out N3 Vdd Vdd PMOS L=70n W=22u AD=66p PD=24u AS=66p PS=24u
.ENDS

.SUBCKT b3 A8 b3 Gnd Vdd
XOr_1 A8 A8 b3 Gnd Vdd Or
.ENDS

.SUBCKT encoder1 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 b0
Gnd Vdd
XOr_1 N1 N2 N7 Gnd Vdd Or
XOr_2 N4 N16 N10 Gnd Vdd Or
XOr_3 N22 N19 N30 Gnd Vdd Or
XOr_4 N30 N31 N25 Gnd Vdd Or
```

```
XOr_5 N7 N10 N3 Gnd Vdd Or
XOr_6 N3 N25 b0 Gnd Vdd Or
XOr_7 N5 A15 N31 Gnd Vdd Or
XXOR2_1 A7 A8 N16 Gnd Vdd XOR2
XXOR2_2 A11 A12 N19 Gnd Vdd XOR2
XXOR2_3 A13 A14 N5 Gnd Vdd XOR2
XXOR2_4 A3 A4 N2 Gnd Vdd XOR2
XXOR2_5 A1 A2 N1 Gnd Vdd XOR2
XXOR2_6 A5 A6 N4 Gnd Vdd XOR2
XXOR2_7 A9 A10 N22 Gnd Vdd XOR2
.ENDS

.SUBCKT Encoder_final A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
b0 b1
+ b2 b3 Gnd Vdd
Xb1_1 A2 A4 A6 A8 A10 A12 A14 b1 Gnd Vdd b1
Xb2_1 A4 A8 A12 b2 Gnd Vdd b2
Xb3_1 A8 b3 Gnd Vdd b3
Xencoder1_1 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 b0 Gnd Vdd
+ encoder1
.ENDS
```

A.5. Code for 4 bit flash ADC

```
* Main circuit: Module2
Xcomparator_section_1 N15 N14 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4 N3 N2 N1
vin
+ Vref Gnd Vdd comparator_section
XEncoder_final_1 N15 N14 N13 N12 N11 N10 N9 N8 N7 N6 N5 N4 N3 N2 N1 b0 b1
b2 b3
+ Gnd Vdd Encoder_final
* End of main circuit: Module2
.param l=35n
V1 Vdd gnd 0.7
V2 Vref gnd 0.7

.include "D:\spice\anil\models\70nm.md"

.dc lin source V3 0 0.55 0.001
*V3 Vin gnd BIT ({10101011} pw=200n lt=100n ht=100n on=0.35 off=0.05)
V3 vin gnd


.power V1 0 100n
.tran 10n 1000n
.print dc  V(b0) V(b1) V(b2)  V(b3) V(Vin)
```

Code for sample and hold circuit

```
* Waveform probing commands
.probe
.options probefilename="differential.dat"
+ probesdbfile="C:\Documents and Settings\Anil\My
Documents\dissertation\diiferential.sdb"
+ probetopmodule="offset comp"

* Main circuit: offset comp
M1 Gnd c1 c1 Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M2 c3 c1 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M3 N9 N7 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M4 N10 N9 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M5 N11 N10 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M6 Out N6 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M7 N6 N11 Gnd Gnd NMOS L=70n W=10.5u AD=66p PD=24u AS=66p PS=24u
M8 c1 Vin- N5 N5 PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M9 N5 Vin+ c3 N5 PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M10 N5 N7 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M11 N9 c3 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M12 N10 N9 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M13 N11 N10 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M14 Out N6 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
M15 N6 N11 Vdd Vdd PMOS L=70n W=21u AD=66p PD=24u AS=66p PS=24u
R16 Vdd N7 1k TC=0.0, 0.0
R17 N7 Gnd 1.65k TC=0.0, 0.0
* End of main circuit: offset comp

V1 Vdd gnd 0.7
V2 vin+ gnd
V3 Vin- gnd 0.3
.include "D:\models\70nm.md"
.dc lin source V2 0 0.52 0.001
.print dc V(Vin+) V(Vin-) V(Out)
```