DESIGN OF A NEW DIGITAL PLL FREQUENCY SYNTHESIZER IN 0.18 μm CMOS TECHNOLOGY WITH LOW LOCKING TIME

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

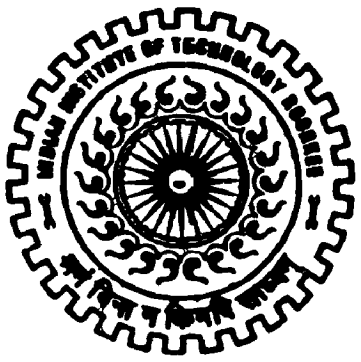
in

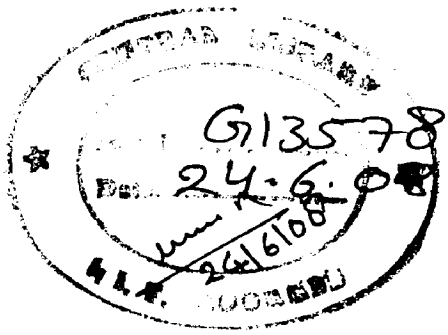
ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices and VLSI Technology)

By

VINIT AGRAWAL





DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE - 247 667 (INDIA)

JUNE, 2007

CANDIDATE'S DECLARATION

I hereby declare that the work, which is presented in this dissertation report, entitled **"Design of a New Digital PLL Frequency Synthesizer in 0.18 μm CMOS Technology With Low Locking Time"**, being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Electronics and Communication Engineering** with specialization in **Semiconductor Devices & VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work carried out from July 2006 to June 2007, under guidance and supervision of **Dr. S. Dasgupta,** Assistant Professor, and **Prof. A.K Saxena**, Professor, Department of electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not submitted for the award of any other Degree or Diploma.

Date 21/06/07
Place: Roorkee

Vinit Agrawal
VINIT AGRAWAL

CERTIFICATE

This is to certify that the statement made by the candidate is correct to the best of our knowledge and belief.

Prof. A. K. Saxena,
Professor, E&CE Department,
Indian Institute of Technology Roorkee,
Roorkee – 247 667, (INDIA)

Date 21/06/07
Place: Roorkee

Dr. S. Dasgupta,
Assistant Professor, E&CE Department,
Indian Institute of Technology Roorkee
Roorkee – 247 667, (INDIA)

Date 21/06/07
Place: Roorkee

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DATE: 21/06/07
PLACE: Roorkee

Vinit Agrawal
VINIT AGRAWAL

ABSTRACT

Frequency Synthesis represents the key aspect of clocking in modern high-speed digital systems and communication. When realized as a phase-locked loop (PLL), frequency synthesizers display high precision and allow simple implementation of programmable frequency switching. In conventional frequency synthesizer operating speed and frequency are limited by frequency divider and voltage-controlled oscillator (VCO). In this thesis, we propose an improved architecture of Digital PLL frequency synthesizer, which has a dual modulus prescaler divider with asynchronous cascaded divided-by-2 circuitry for higher switching speed. The focus is on the circuit configuration and performance parameters of the basic units of the Digital PLL: phase-frequency detector, charge pump, loop filter, voltage controlled oscillator (VCO) and programmable divider.

Simulation results of the Digital PLL with a standard 0.18μm CMOS technology in SPICE illustrate a low locking time. The lock time can be modified by adjusting charge pump current and loop filter capacitor. The PFD (Phase Frequency Detector) circuit is also designed to prevent fluctuation of charge pump circuit under the locked condition. Design of the LPF (Low Pass Filter) involves analysis of loop dynamics of the PLL. Encapsulating various tradeoffs such as lock range, lock time and bandwidth, it is arguably the most challenging block to design. To have linear output frequency tuning range, large capacitance is required (i.e., large area). In order to increase frequency ranges without an increase chip area usage, this work describes a voltage-controlled oscillator (VCO) utilizing a ring of current-starved oscillator which provides linear variation of operating frequency range with supply voltage.

PUBLICATION

[1] Vinit Agrawal, A. K. Saxena and S. Dasgupta, "Design of Digital PLL for High Frequency Clock Generation in Digital Chip Environment", *Proceedings of IEEE ACVIT-07*, November 2007, In Progress.

[2] Vinit Agrawal, A. K. Saxena and S. Dasgupta, "Design of a New Digital PLL Frequency Synthesizer in 0.18 μm CMOS Technology With Low Locking Time", (Communicated).

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1.1 Motivation

With ever increasing performance requirements of microprocessors and communication systems more stringent requirements have been placed on the design of system frequency synthesizers. Today's high-speed frequency synthesizers are often required to operate over a range of frequencies (high frequency for increased performance and low frequency for power saving and operate at low power supplies for both portable and desktop systems). PLL Frequency synthesizers are becoming increasingly useful for clock synthesis and recovery in CPU and other digital chip designs. The digital phase-locked loop (DPLL) is a circuit that is used frequently in high- speed digital systems to generate clock [1]. As shown in Figure-1.1 a reference clock is sent along with the parallel data being communicated. (Only transmit path from chip 1 to chip 2 is shown) since chip to chip communication most often occurs at a lower rate than the on-chip clock rate, the reference clock is divided, but kept in phase with the system clock. In chip 2, the reference clock is used to synchronize all the input flip flop, which can present a significant clock load in the case of wide data busses.

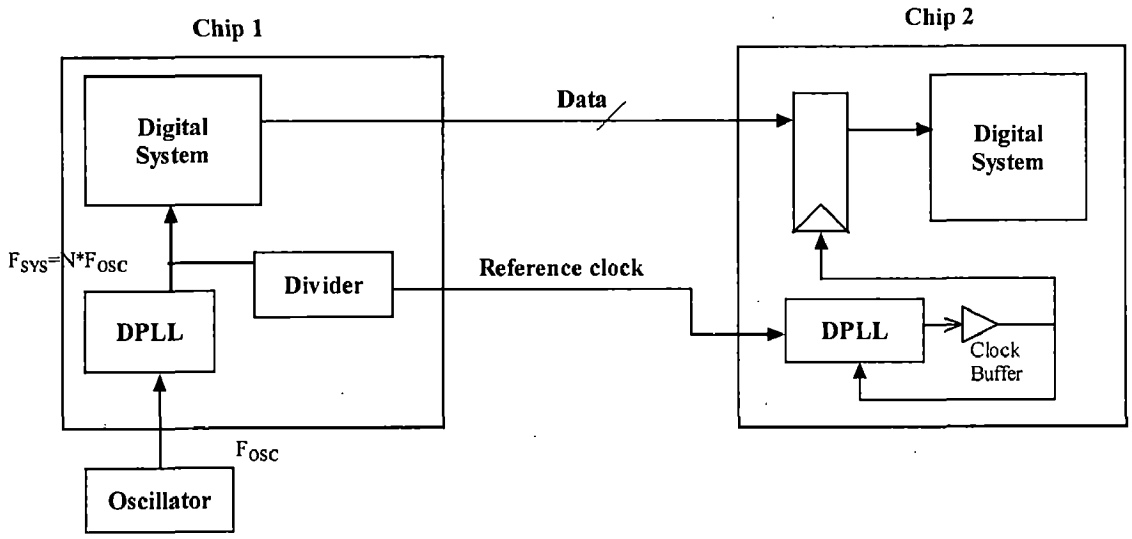


Figure 1.1 Application of Phase locked loop as clock generator

Unfortunately, implementing clock buffers to deal with this problem introduces skew between the data and sample clock. A DPLL Frequency Synthesizer aligns (i.e., de-skews) the output of the clock buffer with respect to the data. In addition, the DPLL

Frequency Synthesizer can multiply the frequency of the incoming reference clock, allowing the core of the second chip to operate at a higher frequency than the input reference clock.

1.2 Background of Phase-Locked Loop

A PLL is a circuit that synchronizes an oscillator's output signal with a reference or input signal in both frequency and phase. The phase error between the oscillator's output signal and the reference signal is constant when the PLL is locked (reference input and oscillator output are synchronized). If a phase error builds up, the feedback control mechanism acts on the oscillator to reduce the phase error to a minimum. The PLL differs from other feedback systems in that it operates on phase deviations rather than signal amplitudes [2]. A basic diagram of PLL is shown in Figure-1.2

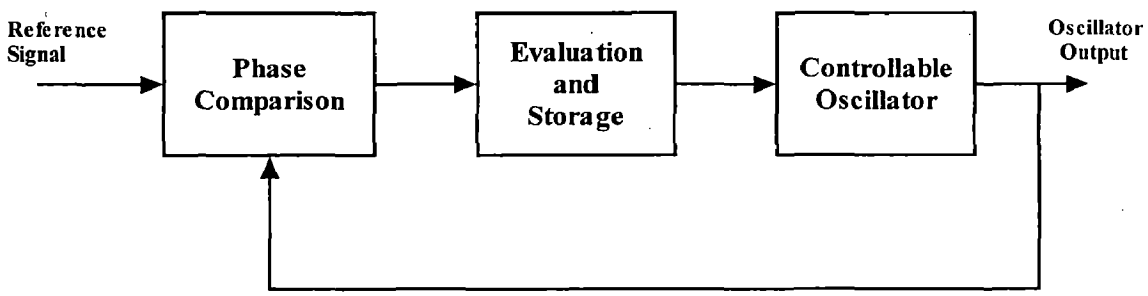


Figure 1.2 Basic Diagram of Phase-locked loop

The function of each block is as follows:

1.2.1 Phase comparison

This block compares the reference phase (and/or frequency) with the phase of the generated signal to generate an error signal proportional to the phase difference. The ideal transfer function of this block is KPD, which is the gain of the phase detector ($V_{error} = K_{PD}.\Delta\phi$). In general, phase detectors (PD) or phase frequency detectors (PFD) are used for detection. The PLL's transient behavior, capture range, and phase-lock characteristics are directly affected by the choice of the phase detector. The main properties that define a phase detector at the higher level are the transfer function, response to unequal input frequencies, and behavior dependencies on input signal amplitudes and duty cycles [2].

1.2.2 Evaluation and Storage

This block provides a control variable from the comparison and modifies its stored value (voltage and current) to apply to the oscillator stage. A low-pass filter (LPF) is commonly employed for smoothing the variations caused by the input noise.

1.2.3 Controllable Oscillator

This nonlinear block generates an oscillation whose frequency is controlled by a lower frequency voltage or current input. The controllable oscillator appears in the form of a voltage-controlled oscillator (VCO) or a current-controlled oscillator (CCO) [3-4].

The first application of a PLL was reported as early as 1932 by deBellescize. Since then, different types of PLLs have been developed. In general, PLLs can be classified into the four categories shown in Table 1 [2] (software PLLs are outside from this table).

Table 1: PLL Implementation

PLL TYPE	COMPARISON	EVALUATION	STORAGE	OSCILLATOR
Linear PLL (LPP)	Analog multiplier	LPF	Analog voltage on filter capacitor	VCO
Charge-pump PLL (CPPLL)	EXOR PD or JKPD	Charge pump and LPF	Analog voltage on filter capacitor	VCO
Digital PLL (DPLL)	PFD	LPF	Analog voltage on filter capacitor	VCO
All-Digital PLL (ADPLL)	EXOR PD or JKPD or PFD	Digital LPF	Digital word	Digitally Controlled Oscillator (DCO)

1.3 Contributions of this thesis

There are many designs in communication that require frequency synthesizer to generate a range of frequencies; such as cordless telephones, mobile radios and other wireless products. The accuracy of the required frequencies is very important in these designs as the performance is based on this parameter. One approach to this necessity could be to use crystal oscillators. It is not only impractical, but is impossible to use an array of crystal oscillators for multiple frequencies. Therefore some other techniques must be used to circumvent the problem. Most of the common frequency synthesizers are based on phase lock loop (PLL) design. Main benefit of using Phase Locked Loop technique in frequency synthesizer is that it can generate frequencies comparable to the accuracy of a

crystal oscillator and compared to direct analog synthesizer and direct digital synthesizer, it has the advantages of simpler design and smaller power consumption [5]. For this reason most of the communication designs make use of a Digital PLL frequency synthesizer.

Considering the scope of this single circuit, this thesis is devoted to the work of a digital PLL frequency synthesizer. In conventional design, the finest frequency resolution equals to the reference frequency. However, in order to fulfill the requirement of stability, the larger loop bandwidth is limited to approximately 1/10 of the reference frequency [6]. As a result, PLL synthesizers with a fine frequency resolution have a small loop bandwidth and thus a low switching speed. Our problem is to design a Digital PLL Frequency Synthesizer with low locking time .In this thesis we propose an improved architecture of Digital PLL frequency synthesizer which offers low locking time and higher loop bandwidth as compared to conventional designs.

Fast switching between different frequencies is also important in Frequency Synthesizer which depends upon design of VCO and programmable divider (in feedback path). For fast switching,

- This work describes a voltage-controlled oscillator (VCO) utilizing a ring of current-starved oscillator which provides linear control over operating frequencies for wide range of power supply voltage. And
- A fixed frequency divider (prescaler) operating at high speed is used before the programmable counter to divide output frequency of VCO. As a result lower input frequency is applied to programmable counter which increases the switching speed between different frequencies.

The focus is on the circuit configuration and performance parameters of the basic units of the Digital PLL: phase-frequency detector (with small dead zone), charge pump, loop filter (second order), voltage controlled oscillator (VCO) and programmable divider. Simulation results of the Digital PLL with a standard 0.18μm CMOS technology in spice illustrate a fast locking time. The lock time can be modified by adjusting charge pump current and loop filter capacitor.

1.4 Thesis Organization

This thesis first investigates fundamental theory behind the Digital phase-locked loop and Characteristics of each blocks of DPLL. In the same chapter we have also discussed about the bandwidth analysis and stability of closed loop. Chapter 3 discusses basic building blocks of frequency synthesizer and proposed an improved architecture of Digital PLL frequency synthesizer. In the same chapter we have also discussed design problems associated with it. In chapter 4, Digital PLL architecture and its implementation at circuit level with a standard 0.18μm CMOS technology in SPICE. The next chapter discusses the various simulation results, stability and output waveforms obtained as a result of Spice implementation. Finally, conclusion and the Scope for future work related to the improved performance of proposed frequency synthesizer are included in Chapter 6.

A Phase Locked Loop or a PLL is a feedback control circuit. As the name suggests, the phase locked loop operates by trying to lock to the phase of a very accurate input signal through the use of its negative feedback path. A basic form of a PLL consists of three fundamental functional blocks namely

- Phase Frequency Detector (PFD)
- Charge pump and Loop Filter
- Voltage controlled Oscillator

Block diagram of digital PLL is shown in Figure 2.1 [7].

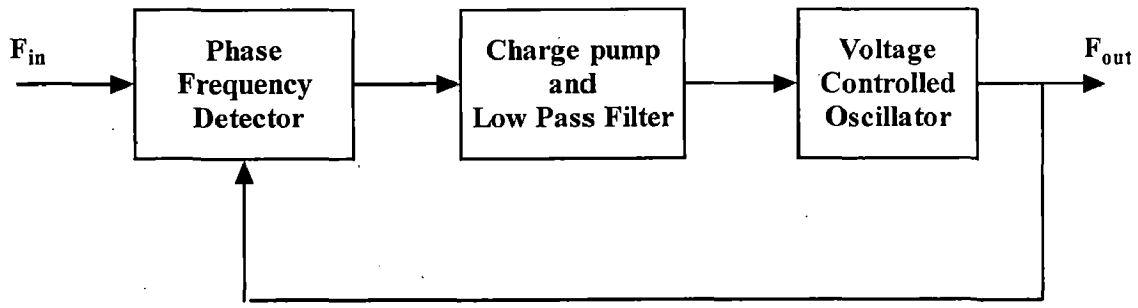


Figure 2.1 Block Diagram of Digital phase-locked loop

The phase detector compares the phase of the output signal to the phase of the reference signal. If there is a phase difference between the two signals, it generates an output voltage, which is proportional to the phase error of the two signals. This output voltage passes through the combination of charge pump and loop filter and then as an input to the voltage controlled oscillator (VCO) controls the output frequency. Due to this self correcting technique, the output signal will be in phase with the reference signal. When both signals are synchronized the PLL is said to be in lock condition. The phase error between the two signals is zero or almost zero at this.

As long as the initial difference between the input signal and the VCO is not too big, the PLL eventually locks onto the input signal. This period of frequency acquisition, is referred as pull-in time, this can be very long or very short, depending on the bandwidth of the PLL. The bandwidth of a PLL depends on the characteristics of the phase detector

(PD), voltage controlled oscillator and on the loop going to look at overall loop operation, let us discuss these main functional blocks in some more detail.

2.1 Phase Detector Overview

The role of a Phase Detector/comparator in a phase-locked loop circuit is to provide an error signal which is some function of the phase error between the input signal and the VCO output signal. Let θ_d represents the phase difference between the input phase and the VCO phase. In response to this phase difference the PD produces a proportional voltage V_d. The relation between voltage V_d, and the phase difference θ_d is shown in Figure 2.2 [7]. The curve is linear and periodic, it repeats every 2π radians. This periodicity is necessary as a phase of zero is indistinguishable from a phase of 2π.

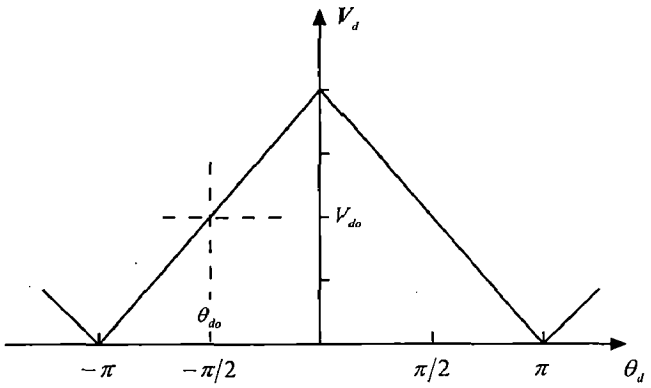


Figure 2.2 Phase Detector characteristics

The slope of the curve gives the gain of PD, and is given by

$$K_d = \frac{dV_d}{d\theta_e} \tag{2.1}$$

In this general model of a phase detector, if no input is applied to PD, (or in other words when phase difference is zero between the two inputs of a PD) it generates a free running voltage V_{do}, which is shown in Figure 2.2. Corresponding to this V_{do}, there is a phase θ_{do} associated with it, which is $\pi/2$ as shown in the Figure 2.2. The common approach is that a phase difference of zero should correspond to the free running voltage V_{do} of the PD. Thus, considering this approach the phase error can be defined as

$$\theta_e = \theta_d - \theta_{do} \tag{2.2}$$

Shifted characteristic of the phase detector is shown in Figure 2.3 [7]

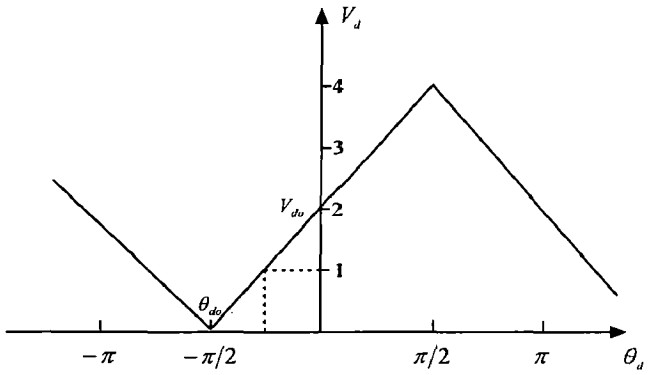


Figure 2.3 Phase Detector's shifted characteristics

The three most important multiplying digital phase detectors are the following.

- The EXOR gate
- JK flip flop
- Phase-Frequency detector (PFD)

The underlying principle behind the operation of each of the phase detectors mentioned is the multiplication of the VCO signal with the input signal, which outputs a dc error signal that is a function of the phase error.

2.2 Charge pump

In the low-pass filter the average value of the PD output is obtained by depositing charge onto a capacitor during each phase comparison and allowing the charge to decay. In a charge pump, on the other hand, there is negligible decay of charge between phase comparison instants. Charge pump consists of two switched current sources driving a capacitor as shown in Figure 2.4 [7-8].

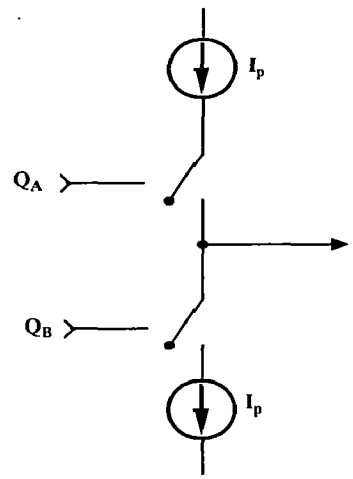


Figure 2.4 Charge pump

Charge pump is used mostly with PFD. In Figure 2.4, let Q_A and Q_B be the UP and DOWN outputs of PFD representing the pulse width by which one input of the PFD leads or lags the other input signal and I_p is the charge pump current.

Each field effect transistor (FET) acts as a simple switch that closes when its input goes high. Hence the output goes high when Q_A goes high, and it is grounded when Q_B goes high. The output current of charge pump, I_{out} is thus a logical function of the PFD state. When PFD is in state 1, I_{out} must be positive, and when PFD is in state 2, I_{out} must be negative. For state 0, I_{out} will be zero. If we plot the average I_{out} vs. phase error θ_e a sawtooth function is obtained as shown in Figure 2.5.

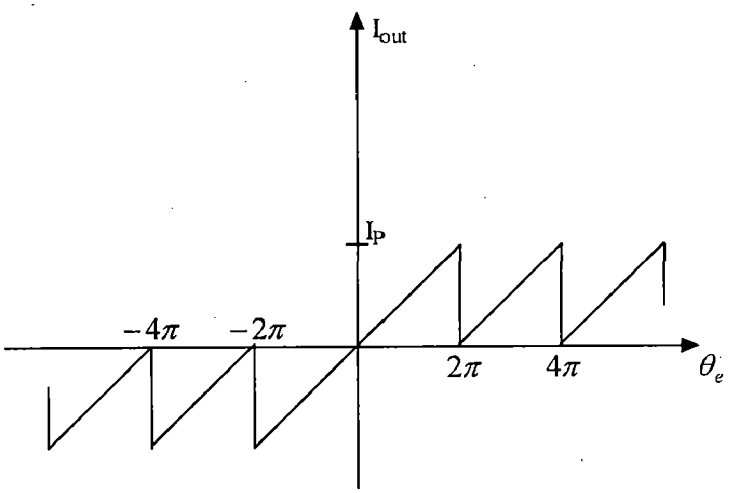


Figure 2.5 Average current vs. phase error plot

The curve is linear between -2π to 2π , and then repeats every 2π. If the phase error θ_e exceeds 2π, the PFD behaves as if the phase error is rotated back to zero. Hence it is a periodic curve with a period of 2π. The gain of Combination of PFD and Charge pump is calculated as

Let us consider the case when the reference clock is leading the feedback clock. The average output current from the charge pump is then given by

$$I_{out} = I_P . \frac{t_{up-active}}{T} \tag{2.3}$$

In which, T is the period of the reference frequency. Therefore, $\frac{t_{up-active}}{T}$ is simply the duty cycle of UP signal. Thus, we have

$$I_{out} = I_P . \frac{\Delta\phi}{2\pi} \tag{2.4}$$

Equation 2.4 can be applied to the cases when the feedback signal is leading the reference clock as well, with both phase error and output current negative. Hence, the transfer function of the PFD and charge pump can be expressed as

$$\frac{I_{out}}{\Delta\phi} = \frac{I_P}{2\pi} \tag{2.5}$$

This is also known as gain of PFD.

$$I_{out} = \frac{(I_p - (-I_p))}{4\pi} * \Delta\phi = K_{PD} * \Delta\phi \tag{2.6}$$

Where K_{PD} is given by

$$K_{PD} = {}^{I_p}\!/_{2\pi} \text{ (Amps/radian)} \tag{2.7}$$

2.3 Loop Filter

The filtering operation of the error voltage (coming out from the Phase Detector) is performed by the loop filter. The output of PD consists of a dc component superimposed with an ac component. The ac part is undesired as an input to the VCO; hence a low pass filter is used to filter out the ac component. Loop filter is one of the most important functional block in determining the performance of the loop. A loop filter introduces poles to the PLL transfer function, which in turn is a parameter in determining the bandwidth of the PLL. Since higher order loop filters offer better noise cancellation [9], a loop filter of order 2 or more are used in most of the critical application PLL circuits.

2.4 Voltage Controlled Oscillator

A VCO is a voltage controlled oscillator, whose output frequency ω_o is linearly proportional to the control voltage V_{CTRL} generated by the Phase detector. This linear relation between the control voltage and the output frequency simplifies the PLL design [7-8]. A typical characteristic of a voltage-controlled oscillator is shown in Figure 2.6. Ideally the slope of the curve is constant. As the control voltage varies from V_1 to V_2 volts, the output frequency of the VCO varies from ω_1 to ω_2.

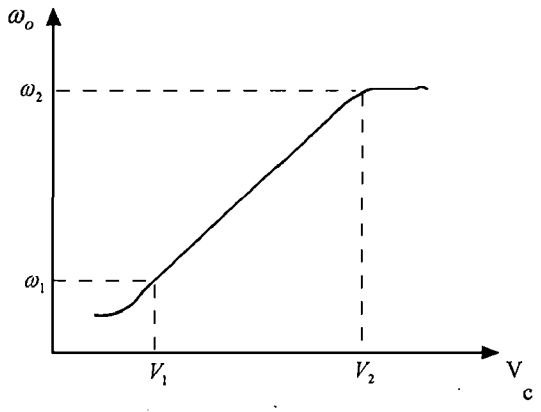


Figure 2.6 VCO Characteristic

Outside this range the curve may not be linear and the VCO performance becomes non-linear Depending on the requirements of the circuit, the range can be selected such that the circuit always remains in its linear range. The slope of the curve is the VCO gain K_{VCO} and is given by

$$K_{VCO} = \frac{d\Delta\omega_o}{dv_c} \tag{2.8}$$

Gain can also be written as:

$$K_{VCO} = 2\pi * \frac{(f_{\max} - f_{\min})}{(V_{\max} - V_{\min})} \text{ (rad/s.V)} \tag{2.9}$$

2.5 PLL Bandwidth and Overall Loop Operation

The bandwidth of a PLL, which determines that how fast a PLL will be in following the input phase, or for how long it will remain in the lock condition, depends on the characteristics of the Phase detector (PD), the voltage controlled oscillator (VCO) and on the Loop filter. Since the bandwidth is associated with the ac model of a PLL, we can form an ac model by eliminating the dc parameters. The liner model is shown in Figure 2.7 [7].

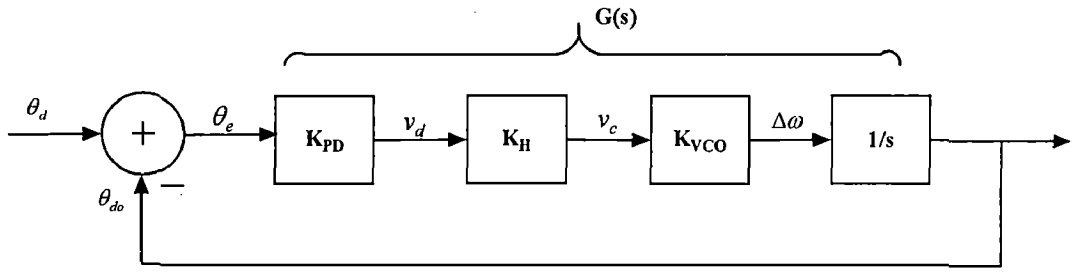


Figure2.7 Linear Model of a PLL

The VCO can be represented by an integrator whose transfer function is 1/ s, where s represents complex frequency. The closed loop transfer function H(s) is

$$H(s) = \frac{\theta_r(s)}{\theta_o(s)} = \frac{G(s)}{1+G(s)} \tag{2.10}$$

$$G(s) = \frac{K_{PD} K_H K_{VCO}}{s} \tag{2.11}$$

The bandwidth ω_{3dB} occurs when $|G(j\omega)| = 1$ from the above equation, this occurs when

$$\omega_{3dB} = K = K_{PD} K_H K_{VCO} \tag{2.12}$$

The bandwidth of the PLL is thus determined by

- Gain K_{PD} of the PFD
- high frequency gain K_H of the loop filter
- Gain K_{VCO} of the VCO

The designs of PD and VCO are usually less flexible. The design of the loop filter is the principle tool in selecting the bandwidth of the PLL. The selection of loop bandwidth forces trade offs in the frequency acquisition speed. Since PLL pull-in speed is a function of the loop bandwidth, the simplest method for improving the lock time is to widen the loop bandwidth. Wider bandwidth improves the lock time but at the same time it degrades the noise characteristics of the loop. So an optimum bandwidth has to be achieved depending on the requirements.

3.1 Introduction

One of the most common use of a PLL is in Frequency synthesizers. The concept of frequency synthesis is not new; it was in existence even in 1930's. But the cost of implementing a frequency synthesizer was so high that it was almost impractical for many designs. A frequency synthesizer generates a range of output frequencies from a single stable reference frequency of a crystal oscillator. Many applications in communication require a range of frequencies or a multiplication of a periodic signal. For example, in most of the FM radios; a phase-locked loop frequency synthesizer technique is used to generate 101 different frequencies. Frequency Synthesizers are also widely used in signal generators and in instrumentation systems, such as spectrum analyzers and modulation analyzers.

The frequency synthesizer's simplified block diagram is shown in Figure 3-1 (a) [9-10]. In the frequency synthesizer, the PLL block is responsible for generating an output signal whose frequency is dependent on the phase relationship between two input signals. The phases of a reference signal, F_{refer_c}, and a feedback signal, F_{feed_c}, are compared in a phase frequency detector (PFD), and the phase difference is then converted by a charge pump and low pass filter (CP/LPF) circuit into a control voltage. This voltage controls the VCO to generate a signal with the desired frequency. A divider is inserted on the feedback path, giving $F_{feed\_c} = F_{out}/M$. Since in the locked condition, F_{refer_c} and F_{feed_c} must be equal, F_{out} is simply equal to the product of F_{refer_c} by M. Shown in Figure 3-1(b) are the simple waveforms with M=4.

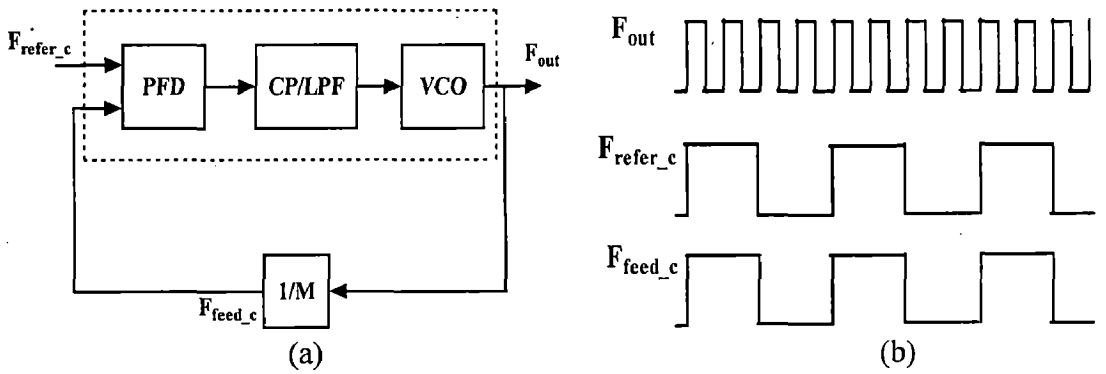


Figure 3.1 (a) Block diagram of Frequency synthesizer (b) Typical waveform with M=4

By changing the multiplication factor, M, signals with desired frequency can be generated.

3.2 Proposed Architecture of frequency synthesizer

In conventional frequency synthesizer, operating speed and frequency are limited frequency divider and voltage controlled oscillator [11]. In this thesis, we propose an improved architecture of digital PLL frequency synthesizer is shown in Figure 3.2. Besides a PLL it also includes a very stable crystal oscillator with a divide by N – programmable divider in the feedback loop. A divider in the feedback path enables the PFD to compare the reference frequency with the divided VCO output frequency. This typical integer-N programmable divider, called dual modulus prescaler and pulse swallow divider, is shown in Fig. 3.2. Dual modulus prescaler divider can change its divider ratio according to the external channel selection input and has asynchronous cascaded divided-by-2 circuitry for higher switching speed [12].

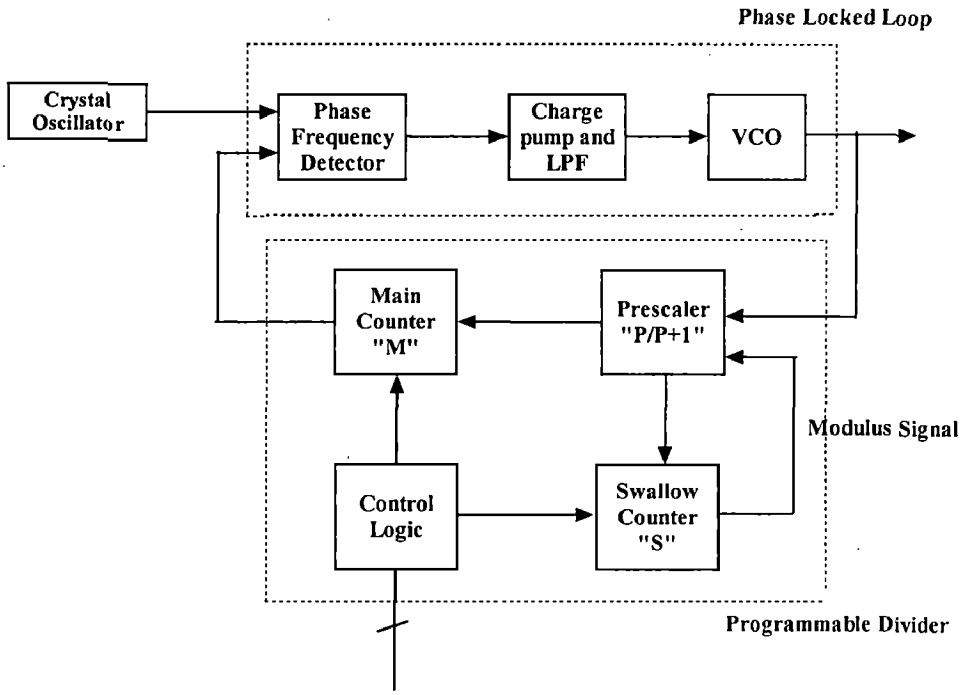


Figure 3.2 Digital PLL Frequency Synthesizer

The prescaler frequency divide ratio is P or P+1, depending on the logic state of the control input. The prescalers reduce the high frequency by division to a lower frequency, so the rest of the circuit sees only a fraction of the high output frequency. For example, if a prescaler of 20 is used at the output of 900 MHz, then the rest of the circuit only sees 45 MHz. In the Figure 3.2 a special low frequency counter is used to control the division

ratio of the prescaler and consists of one programmable counter, (swallow counter S), Main counter M and some control logic. Initially Programmable counter is loaded with the values S, where S $\leq$M and modulus control signal is low, so the prescaler divides by (P +1). The counters are both decremented on every rising edge of the output of Prescaler unit, until the counter S reaches zero.

When S becomes zero, the modulus control signal becomes high and the prescaler start dividing by P until the value of the M counter reaches zero. At this point both the counters are reset and the process begins again. The prescaler thus divides by (P +1) for the count value of the counter S and by (P) for M-S times. This relation can be best explained with the following equation [13].

$$N = [S*(P+1)]+[(M-S)*P] = M*P+S \qquad (3.1)$$

There are some limitations imposed by the architecture of the system on the values of M and S, since two modulus prescaler does not change modulus until counter S reaches zero, therefore count value in counter M should never be less than the value in counter S.

3.2.1 An Example

It will be easy to understand the concepts developed in section 3.2 with a reference example. Consider the following case where the output frequency is 115 MHz and the reference input is 5 MHz. The N is thus required to be 23 and the values of M, S and P are selected to be as 5, 3 and 4 respectively. The method of determining the counter values will be explained in the next section.

Initially the counters M and S will be loaded with the values 5 and 3 respectively. The value of each of these counters will be decremented after each rising pulse of the prescaler output. The more detailed timing consideration can be understood with reference to the example Figure 2.4 The prescaler divides by 5, when the S counter has the values 3, 2, 1 and by 4, when S becomes zero. Thus for the values 2 and 1 of the M counter, it divides by 4. The counter M outputs a pulse to the phase detector, when it becomes zero. Both the counters are reset (when M reaches zero) and the process begins again. So the whole division is 23 as is expected. The output signal is derived from the short pulse used to reset the counters. It is important to note that the prescaler division

ratio is determined by the state of the modulus control on the rising input edge when the prescaler output is about to become high.

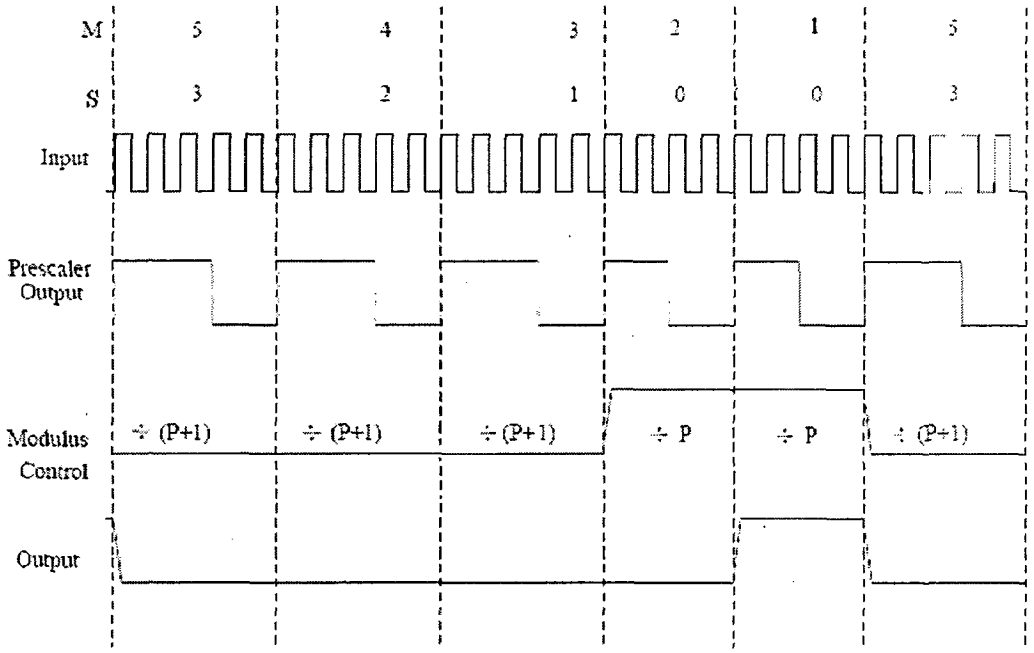


Figure 3.3 Timing diagram of a Two Modulus Prescaler

3.3 Design for Two Modulus Divider

For high speed frequency synthesizer designs incorporate high speed Dual-Modulus dividers. Such circuit divides the input frequency by one of the modules according to a control input. A circuit diagram of a Two Modulus Divider for this design is shown in Figure 3.2. It consists of two Prescalers, a Main counter, A Swallow counter and a control unit. Now In this chapter we will develop the design for these subunits.

As was mentioned earlier, that there are many constraints for the values of the swallow counter S, main counter M and on the values of prescaler required for a particular design. Let us calculate these numbers for this Digital PLL Frequency synthesize.

$$R = \text{Reference frequency} = \text{Step size of the output frequencies} \qquad (3.2)$$

Therefore, from the data provided about the MYDESIGN frequency synthesizer, we have

$$R = 300 \text{ KHz}$$

Then the value of N, the total division number will decide range of possible output frequencies

$$N = 3072\text{-}3103$$

The value of Prescaler can be selected any value, such as 8/9 or 32/33 or 64/65 etc. For instant, 64/65 is selected for this design then the values of M and S can be calculated using the following equations

$$M = truncate\left[\frac{N}{P}\right] = 48 \tag{3.3}$$

We are selecting the value of M which is fixed for the entire range of frequencies. It was the main reason behind selecting the Prescaler values 64/65. (The fix value of M also reduces the complexity of the divider). If possible, one should always try to fix the value of M. The value of S is calculated with the following equation

$$S = N - [M \times P] = N - [48 \times 64] = 0 \text{ to } 31 \tag{3.4}$$

So, if the value of S is 0 the output frequency will be low and if it is 31 then the output frequency will be high. Thus this range of S from 0 to 31 is for the desired output frequencies, but the design is easily expandable for other frequencies outside this range by adding more output lines to program the Swallow Counter. Since we have 5 output lines to program the S counter, therefore a minimum of 0 and a maximum number 31 can be loaded in this counter. By doing this the value of S is still less than the value of M, which meets with the constraint, thus all these numbers are valid. From the value of S, we can also estimate the number of output lines n, required to program the swallow counter S. Since in this case the maximum value of S is 31, we need 5 output lines for interfacing and programming the swallow counter. The design of all of theses sub-functional units will be covered in the chapter

3.4 Prescaler

If the frequency, F_{in}, of an input signal is too high, a divider can be added using an additional programmable counter in the feedback path. As shown in Figure 3.2, the frequency can be divided before the programmable counter using a fixed frequency divider (prescaler) operating at high speed, this lowers the input frequency to the programmable counter. This method is called the prescaler method.

A dual modulus prescaler with asynchronous cascaded divided-by-2 circuitry is a high frequency divider [12], [14], [15]. There are two prescalers in the two modulus divider for this design namely, a divide by 64 and a divide by 65 prescalers. The designed prescalers

are presented in this section and their simulation results for this design will present in the fifth chapter.

3.4.1 Divide by 64

Asynchronous dividers are the simplest form of prescalers. They consist of a series of D flip flops, where each D flip flop's inverted output is connected back to its input, making it a divide by two circuit. If the input is fed into the clock signal of this circuit the output frequency will be half of the input frequency. A circuit configuration of such a circuit and its input output behavior is shown in Figure 3.4.

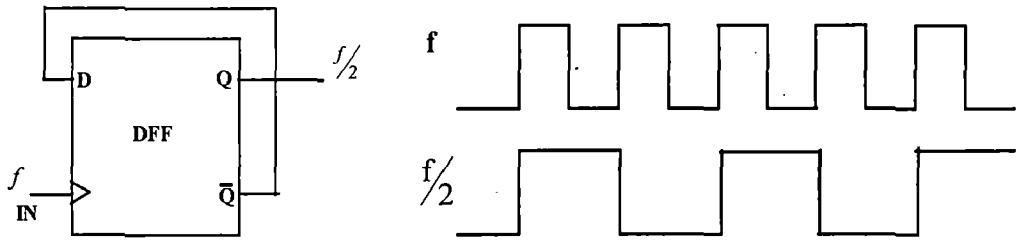


Figure 3.4 (a) Divide by 2 Prescaler (b) Output waveform

A very nice feature of this circuit is that the output is perfectly symmetrical square wave regardless of whether the input square wave is symmetrical or not. By cascading several D flip flops in the same configuration; it is easy to make a divide-by-2N circuit. The non-inverting output of one flip flop can be used as an input to the next flip flop to make it a divide by 4 circuit. Thus to divide an input frequency by 64, we only need to have 6 D flip flops connected in this configuration. The designed circuit for the prescaler 64 is shown in Figure 3.5

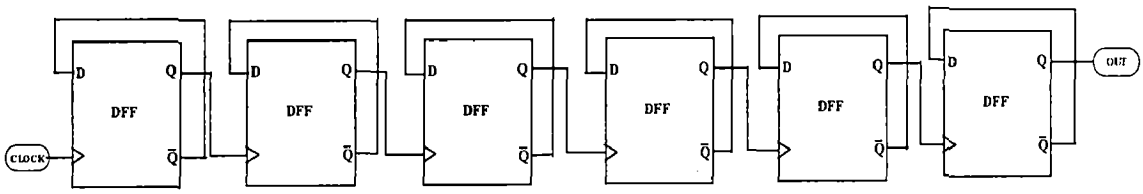


Figure3.5 Divide by 64 Prescaler

3.4.2 Divide by 65

This prescaler is more complicated to implement as compared to a divide by 64 prescaler. The reason is the odd number division. There are two ways to build this circuit, one is completely synchronous and the other is mixed. Since the first method is more complex

as compared to the second one, we will use the second method, which is asynchronous and synchronous mixed design. In this method the circuit is divided into two units. One unit is a divide by 5 circuit and the second one is a divide by 13. The output of first unit will be fed into the second unit, and the whole circuit will be a divide by 65 prescaler circuit. These two circuits are basically ring counters with the number of states corresponding to the division number. For example if we need to divide by 5, the ring counter will have five stages only and will count in a ring fashion. Same is true for a divide by 13 unit, it will have 13 stages and will also count in the ring fashion. The number of flip flops required can be found from the number of stages. So we need 3 D flip flops for the divide by 5 circuit, as it has only five stages and 4 D flip flops for the divide by 13 circuit. All the flip flops are raising edge triggered. The designed prescaler is shown in Figure 3.6 (a) divide by 5 counter and 3.6 (b) divide by 13 counter.

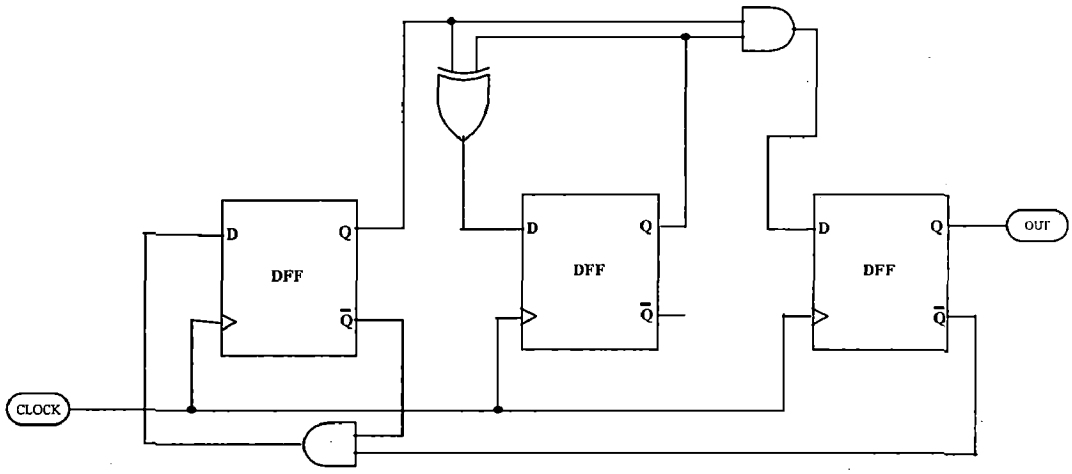


Figure 3.6 (a) Divide by 5 Counter

3.5 Swallow Counter

For programmable divider, there are two kinds of frequency dividers: Swallow counter and programmable divide-by-N counter. Both swallow counter and programmable divide-by N counters are slower because the programming circuit adds additional delay. Swallow counter have higher operating frequency than programmable divide-by-N counters because their programming circuit has smaller loading [16]-[17]. A Swallow counter in two modulus prescaler divider is a programmable down counter. For this Digital PLL frequency synthesizer, Swallow counter needs to count down from the loaded number to zero. It repeats the counting down sequence from the same number until the loaded number is changed externally. It has the option of Load, this is required to

enable the loading into the swallow counter with the division number. To generate 32 different frequencies, the range of numbers that needs to be loaded in the swallow counter is 0 through 31. Thus 5 flip flops are required for the design. Based on the design of the swallow counter up to 32 output frequencies can be synthesized with no extra hardware. The swallow counter is reset through the LOAD value, whenever the Main counter outputs a pulse and we need to begin the counting sequence again. The proposed design of the Swallow counter for this Digital PLL frequency synthesizer is shown in Figure 3.7

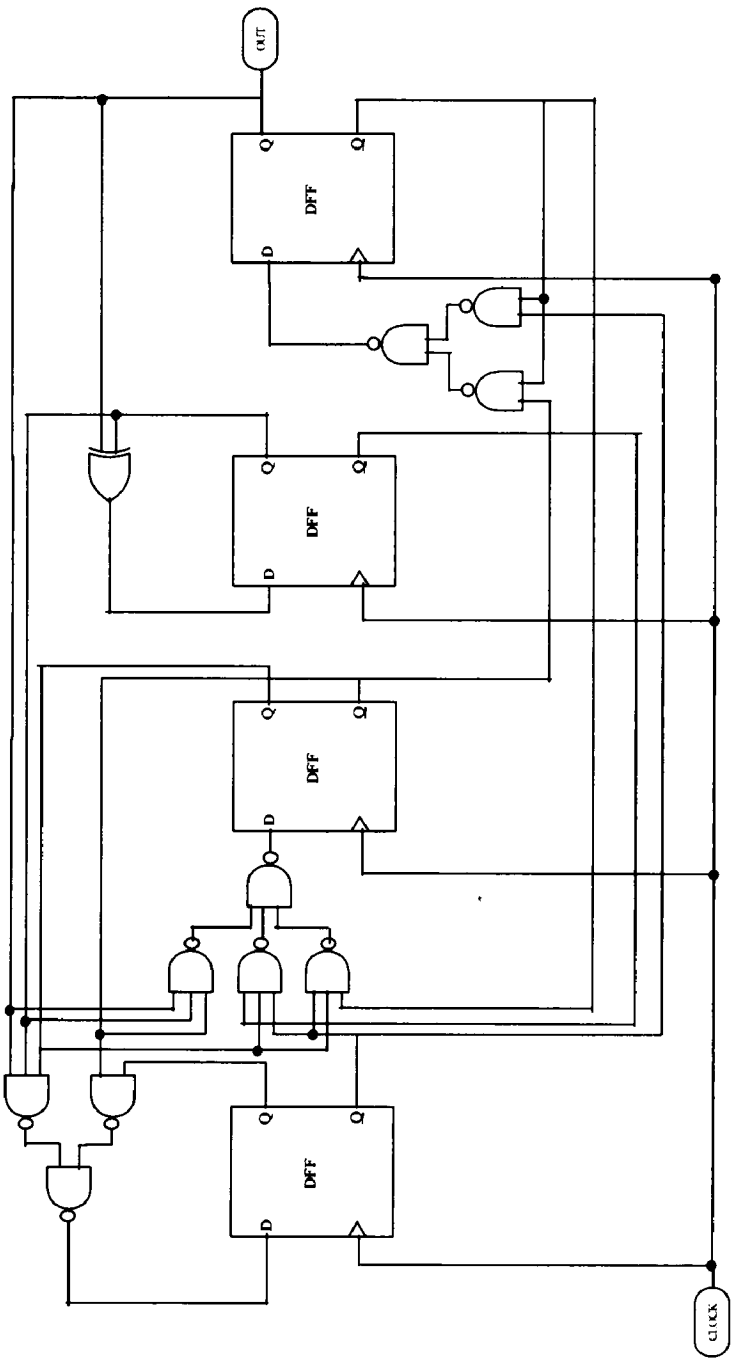


Figure 3.6 (b) Divide by 13 Counter

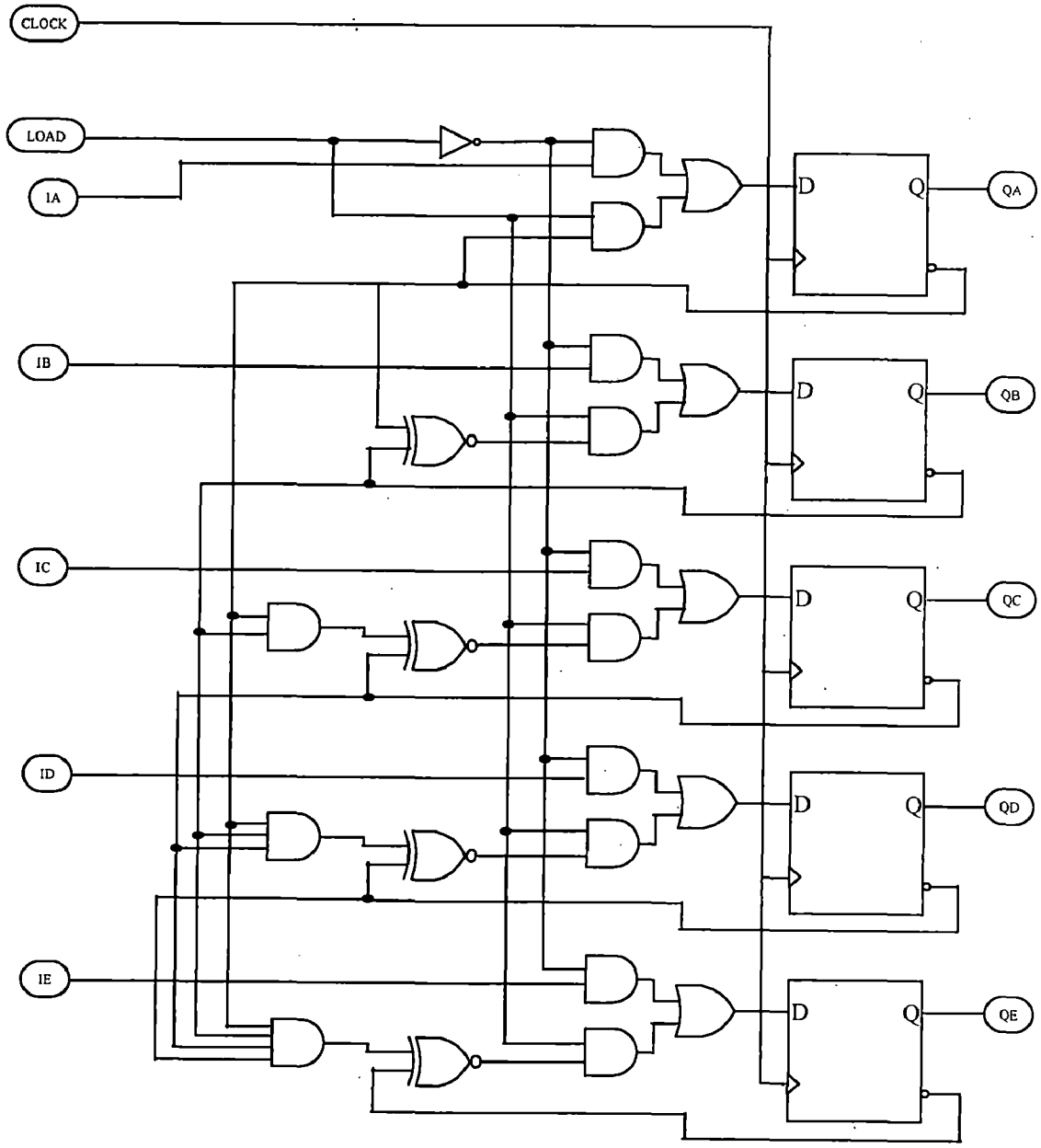


Figure 3.7 Swallow Counter

3.6 Main Counter

The main counter is also a frequency divider circuit, just like the prescalers we discussed before. It divides by 48. The number is 48 for this design and was derived in beginning of this Chapter. The input of the main counter is the output of the prescaler unit. For the division number of 3072, it takes 48 pulses of divide by 64 prescaler (no pulse from divide by 65 prescaler) and yield only one pulse. This pulse is equal to the output of the VCO divided by 3072. In another case suppose total division number is 3080 then main counter takes first 8 pulses of the divide by 65 prescaler and remaining 40 pulses of divide by 64 prescaler and yield only one pulse as previously. The circuit is designed with the same technique as we used for the divide by 65 prescaler [14]-[15]. It first divide the input by 16 and then the second unit divide this output by 3 yielding a total of divide by 48 output. The circuit configuration is shown in Figure 3.8 and its simulation result will present in the fifth chapter.

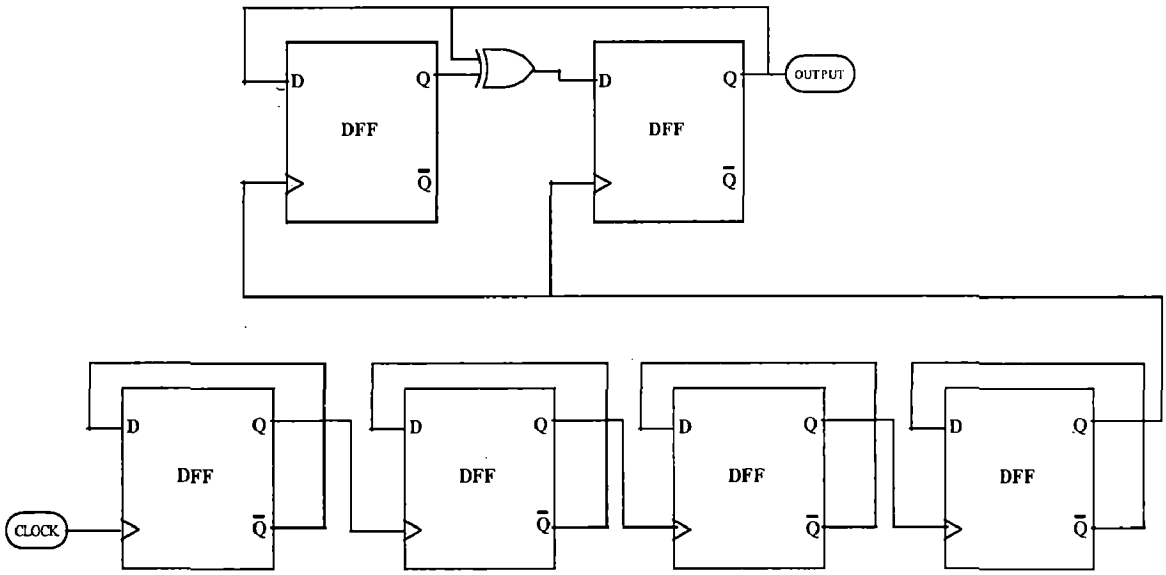


Figure 3.8 Main Counter

3.7 Control Logic

The designed control logic of Two Modulus Divider is shown in Figure 3.9. It consists of two (2 input) multiplexer and some other simple logic design. It will be easy to understand if, we will start from the output of the Swallow Counter. All the outputs (5 in this design) of the Swallow Counter are fed into a OR gate. The output of the OR gate is the control input of MUX2. At the very first cycle, the output of the OR gate is zero so it

enables the loading operation. As soon as the Swallow counter is loaded with a value the output of the OR gate becomes high at next clock cycle, thus disabling the LOAD operation of the Swallow Counter. The high output of the OR gate, because of control input of MUX2 now enables the CLOCK input of the swallow counter. The inverted output of the OR gate also act as a control input for the prescaler units, as is depicted in the Figure 3.9. So whenever the OR gate output is high the Divide by 65 prescaler unit is active and the input is being divided by 65; and the Main counter receives the pulses from the divide by 65 unit. At every pulse to the Main counter, the swallow counter counts down and when it reaches zero, the output of the OR gate becomes zero, and now the divide by 64 prescaler is active and the CLOCK input of the swallow counter is now connected to the output of the Main counter again. Since at the output of the Main counter there is no pulse, because it is still receiving pulses from the divide by 64 prescaler and hasn't yet received 48 pulses the Swallow counter is pause during this time. When the pulses to the Main counter reach 48, the Main counter outputs a pulse and the Swallow counter is once again loaded with the division number and the sequence begins again.

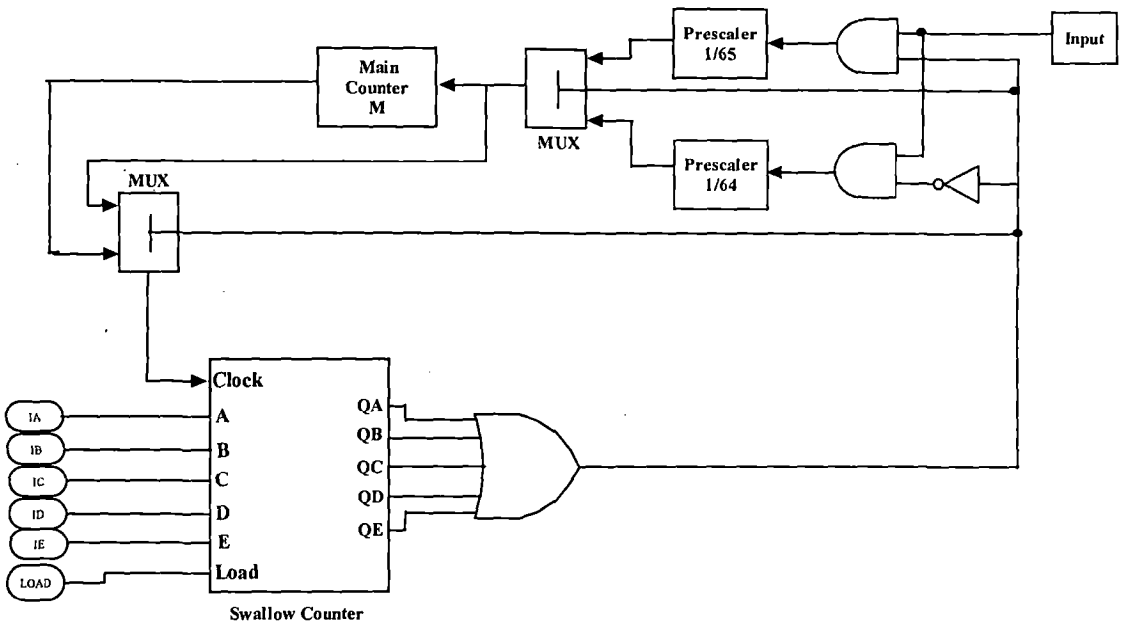


Figure 3.9 Control Logic

4.1 Phase Frequency Detector

PLL performance characteristics may vary depending on the type of phase detector (PD) used. As discussed before in chapter 2, several types exist. For high speed performance, three state - dual D flip-flop PFD is preferred. A phase-frequency detector (PFD) is a block which can detect a phase difference as well as a frequency difference between a reference signal and a feedback signal coming from the divider. PFD is designed to generate charge-up (UP) and charge-down (DOWN) pulses for control of the charge pump. The block accepts two inputs, from the reference clock (shown by A) and the feedback clock (shown by B). The feedback signal rising edge is compared with the reference signal rising edge and the PFD produces either an up or down reference pulse per comparison cycle whose width is proportional to the time difference (phase difference) between the signal edges.

The PFD can be in one of the following four states:

- UP = 0, DN = 0 --- state 1
- UP = 1, DN = 0 --- state 2
- UP = 0, DN = 1 --- state 3
- UP = 1, DN = 1 --- state 4

The additional 4th state is hidden and not shown in Fig. 4-1 because it happens due to the delay time of the AND gate. Whenever both flip-flops' are in the 1 state, a logic high level appears at their reset inputs, which resets both flip-flops. Consequently the device acts as a tri-stable device shown in figure 4.2 [18-19].

- UP = 0, DN = 0 --- state 1
- UP = 1, DN = 0 --- state 2
- UP = 0, DN = 1 --- state 3

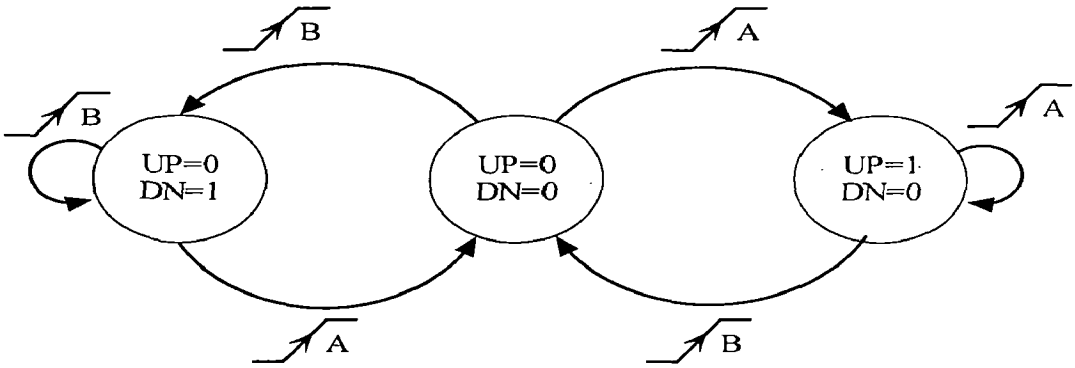


Figure 4.1 State transition diagram of PFD

Where A and B are representing reference and feedback signal respectively.

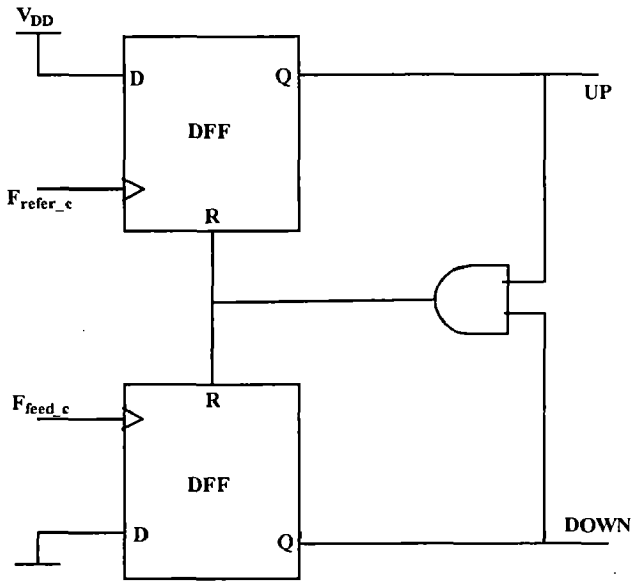


Figure 4.2 Phase Frequency Detector

RESET signal is generated by the AND gate in the PFD's has own feedback loop, so the time duration of the hidden 4th state will be controlled by the transition delay of the AND gate. In general, a delay element is inserted between the AND gate and RESET input of the D flip-flops in order to control the time duration of the hidden 4th state. A delay element for controlling the 4th state is very important to correct the deadzone problem. In case when phase difference between the reference and feedback signal is below a certain value, the UP and DOWN control signals can not reach their logic high level without a delay element due to the finite rising and falling speed, failing to turn on the charge pump. Dead zone is shown in figure 4.3.

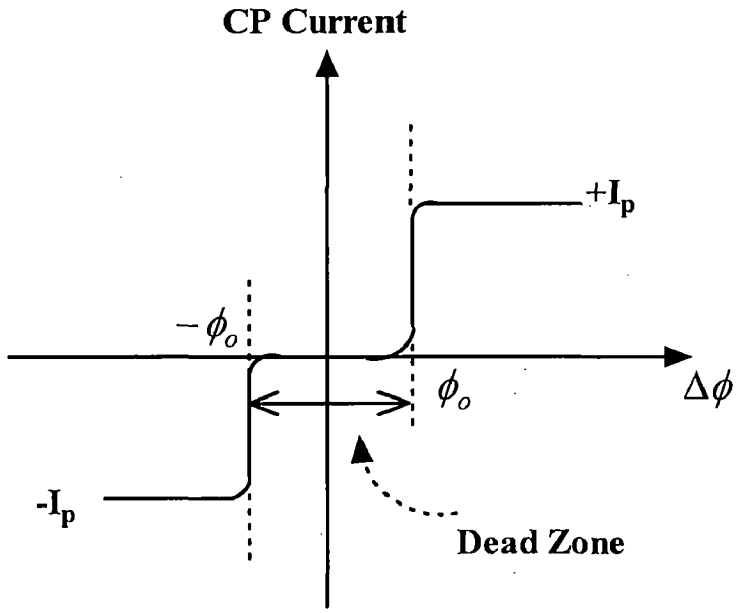
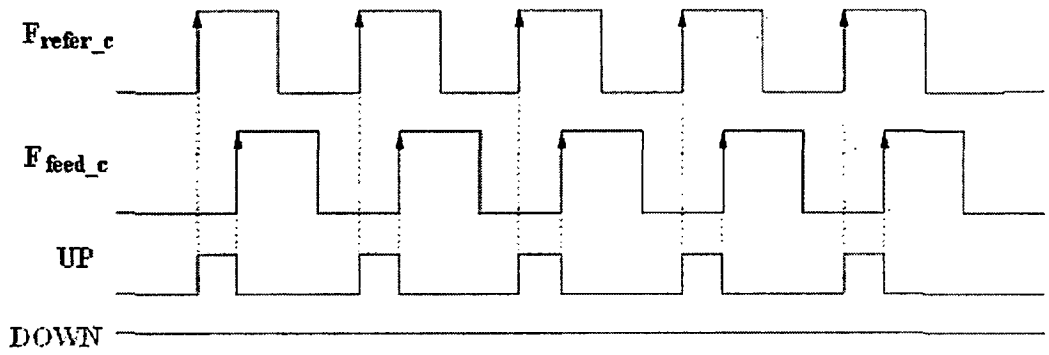


Figure 4.3 Dead Zone in the charge pump current

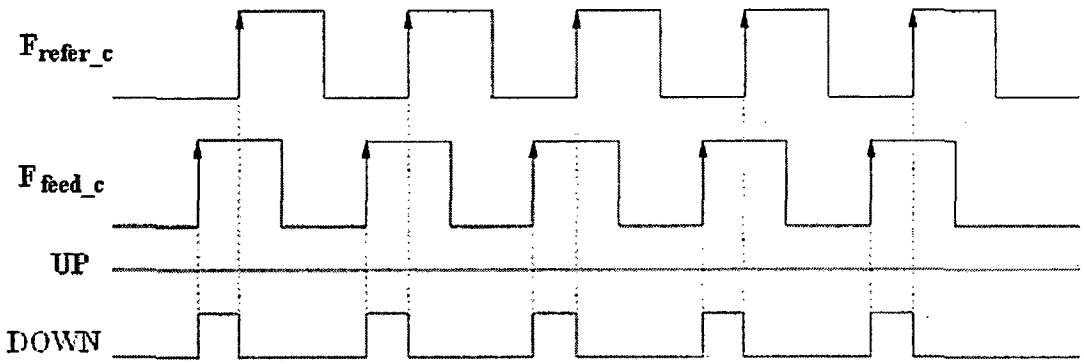
PFD eliminates the "dead zone" by turning both sources on at the same time and produces a minimum pulse width on UP and DOWN at the PFD output. These simultaneous Up and Down signals in the steady state of the PLL create a short circuit in the charge pump which results in a perturbation on the LPF voltage, and hence produce jitter. To limit the LPF voltage perturbation without having a deadzone we have to reduce the minimum Up and Down pulse width by reducing the reset delay in the PFD [20].

The 3-state PFD output is used to modify the voltage on the loop filter capacitor by adding or removing charge through the charge pump. More precisely:

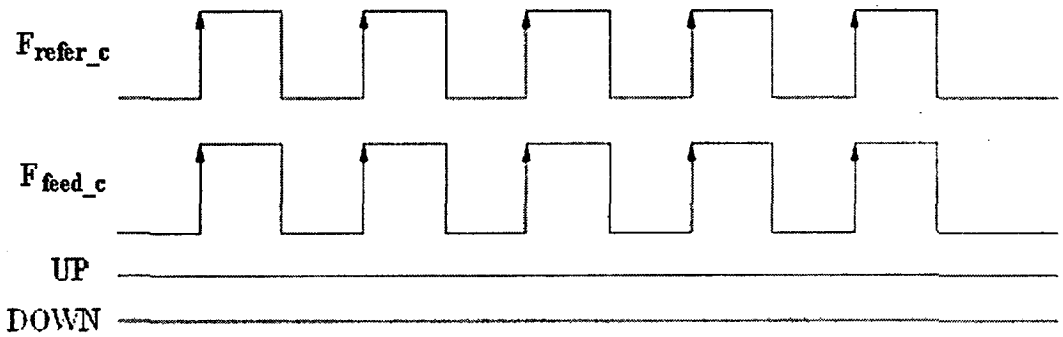
- A current pulse (I_{CP}) to charge the loop filter capacitor is produced when the VCO is lagging the reference (UP = high, DOWN = low)
- A current pulse (I_{CP}) to discharge the loop filter capacitor is produced when the VCO is leading the reference (UP = low, DOWN = high)
- No charge/discharge pulses generated to keep the filter charge constant (UP = DOWN = low)



(a)



(b)



(c)

Figure 4.4 Expected Output of PFD

(a) F_{refer_c} is leading F_{feed_c} (b) F_{feed_c} is leading F_{refer_c} (c) F_{refer_c} and F_{feed_c} both are in phase

4.2 Charge Pump

The output of a PFD (Up and Down pulses) can be converted to DC (voltage/current) in many different ways. One approach is to sense the difference between the two outputs by using a differential amplifier and apply the result to a low pass filter. The second method is by using a charge pump. In this work we are using second method to convert PFD output in a voltage.

The charge pump circuit used is shown in Figure. 4.5 [20]. The purpose of the charge-pump is to source or sink current to the loop filter node. Charge-pump operation is controlled via the outputs of the PFD. Since the PFD eliminates the "dead zone" by turning both sources on at the same time, a current mismatch between the sources can inject extra noise to the output control node. To avoid variations of the output current due to the output voltage, high-impedance cascode current sources are used [21].

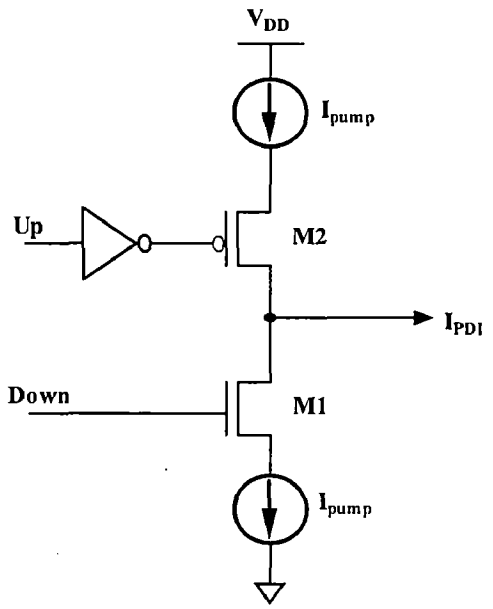


Figure 4.5 Charge Pump Circuit

The average amount of current added (by Up) to or subtracted (by Down) from the node is proportional to instantaneous phase difference between the signals present at the inputs of the PFD. The charge-pump circuitry is designed to provide equal average source and sink currents. Charge-pump descriptions are given in [22]. The charge-pump has a sensitive analog output. Therefore, direct access to this node could have undesirable effects on overall DPLL operation.

4.2.1 Current source

The current sources are implemented by connecting the gate of PMOS to ground and the gate of NMOS to $V_{dd.}$ Current source implemented with PMOS transistor acts as a current source and the other implemented with NMOS acts as current sink. MOSFET current sources are used in place of resistors since the actual implementation of resistors requires a relatively large area on a silicon chip. The aspect ratios of current sources are adjusted to generate output current, according to the following equation.

$$I_{CP} = K_P . W/2L . (V_{GS} - V_{th})^2 \quad (4.1)$$

Where channel length modulation is neglected. Here, K_p is the process transconductance of a PMOS transistor, W and L are the width and length of the transistor, respectively, V_{GS} is the gate to source voltage and V_{TH} is the threshold voltage.

4.3 Loop filter

The primary function of the loop filter is to convert the output from the charge-pump into a steady voltage proportional to the phase difference between the signals present at the input of the PFD. The loop filter also aids in suppression of high frequency transients resulting from the switching characteristics of the charge-pump [23]. The design of the LPF involves the analysis of the loop dynamics of the PLL .Encapsulating various tradeoffs such as lock range, lock time, and bandwidth, it is arguably the most challenging block to design. To reflect a design-oriented approach, key ideas of control theory are summarized, followed immediately by a discussion on how design variables are chosen as predicted by the theory. In this work we are using second order filter shown in Figure. 4.6 (a).

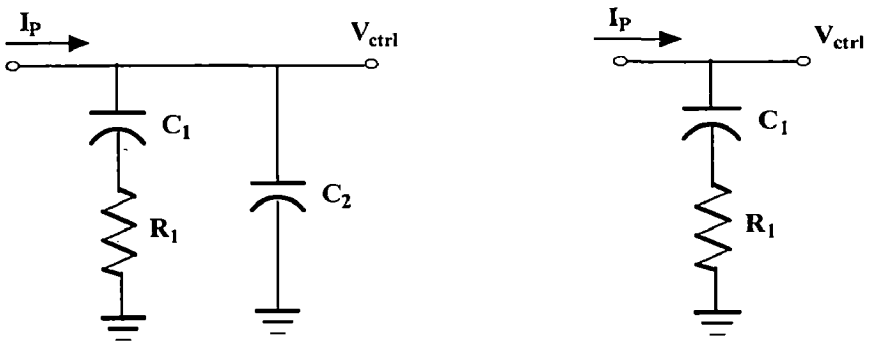


Figure 4.6 (a) Second order Low Pass filter (b) Simplified filter

4.3.1 Loop dynamics for stability

In order to understand and analyze the functional behavior of loop pass filter and frequency synthesizer, it is necessary to construct a linear model for the system. As we will see, the frequency synthesizer is a non-linear device but it can be modeled as a linear device since under normal operation, the system behaves fairly linearly [23]-[24]. In previous chapter, we discussed each building block and its linear model. Now we will combine the models and analyze the synthesizer system as a whole. Since we intend to concentrate on circuit design here, an in-depth discussion of each building block and its model is beyond the scope of this thesis.

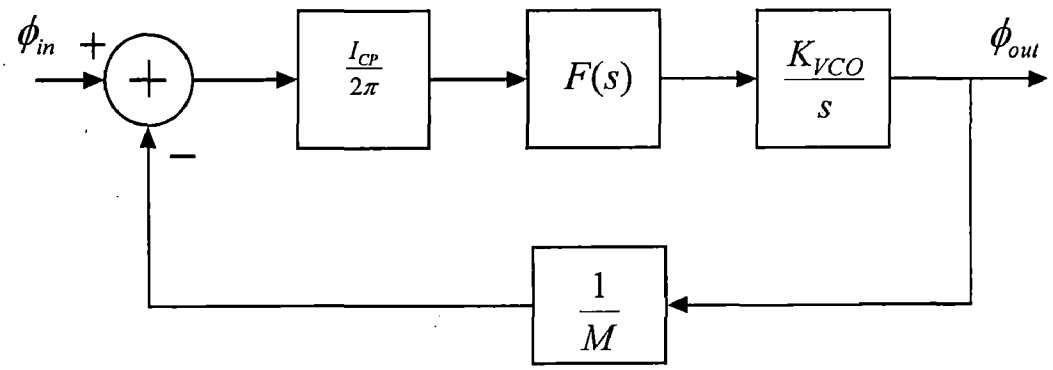


Figure 4.7 Linear model of frequency synthesizer

Transfer function of Second order loop filter (figure 4.6 (a))

$$F(s) = \frac{1 + sR_1C_1}{sC_1(1 + \frac{C_2}{C_1} + sR_1C_2)} \tag{4.2}$$

Zero and Second pole of F(s) are located at:

$$\omega_Z = \frac{1}{R_1.C_1} \tag{4.3}$$

$$\omega_P = \frac{C_1 + C_2}{R_1.C_1C_2} \tag{4.4}$$

Where ω_Z and ω_P are location of zero and pole of F(s).

Capacitor C_2 (in figure 4.6 (a)) is used for suppressing the ripple noise caused by R_1-C_1 loop and can be neglected as long as it is much smaller than C_2. Thus, the loop filter can be simplified to the circuit shown in Figure 4.6 (b). Then pole of the system becomes

$$\omega_P = \frac{1}{R_1.C_2} \tag{4.5}$$

and loop filter's transfer function becomes

$$F(s) = \frac{V_{out}}{I_{out}}(s) = \frac{1 + s.R_1.C_1}{s.C_1} \tag{4.6}$$

Therefore, open loop transfer function of Frequency synthesizer is

$$G(s).H(s) = \frac{I_{CP}}{2\pi}.\left(\frac{1 + s.R.C_1}{s.C_1}\right).\frac{K_{VCO}}{s}.\frac{1}{M} \tag{4.7}$$

And yielding new frequency synthesizer's closed loop transfer function

$$T.F = \frac{G(s)H(s)}{1 + G(s)H(s)}$$

$$= \frac{\frac{I_{CP}}{2\pi}.\left(\frac{1 + s.R.C_1}{s.C_1}\right).\frac{K_{VCO}}{s}.\frac{1}{M}}{1 + \frac{I_{CP}}{2\pi}.\left(\frac{1 + s.R.C_1}{s.C_1}\right).\frac{K_{VCO}}{s}.\frac{1}{M}}$$

$$= \frac{\frac{I_{cp}}{2\pi}.K_{VCO}\left(s.R_1 + \frac{1}{C_1}\right)}{s^2 + sR_1.\frac{I_{cp}}{2\pi M}.K_{VCO} + \frac{I_{cp}}{2\pi.MC_1}.K_{VCO}} \tag{4.8}$$

The dynamic behavior of the PLL can be analyzed after converting the denominator to the normalized form: $s^2 + 2\zeta\omega_n s + \omega_n^2$

Therefore, the natural frequency ω_n, damping factor ζ, and loop bandwidth ω_{lpf} can be written as

$$\omega_n = \sqrt{\frac{I_{cp}}{2\pi.MC_1}.K_{VCO}} \tag{4.9}$$

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_{cp}C_1}{2\pi M}}.K_{VCO} \tag{4.10}$$

$$\omega_{lpf} = 2\zeta\omega_n = \frac{I_{cp}K_{VCO}R_1}{2\pi.M} \tag{4.11}$$

In a synthesizer, Divider and PFD are digital blocks, whereas the LF and VCO usually consist of analog circuits. So the fact that two different systems are mixed in the frequency synthesizer necessitates discrete time analysis for the stability check. As the loop bandwidth becomes comparable with the input frequency, the PLL suffers from stability problems. In typical designs, the loop bandwidth should be less than approximately one tenth of the reference frequency. F. M Gardner has derived the following stability limit based on the reference frequency and loop bandwidth [22].

$$\omega_{lpf}^2 < \frac{\omega_{REF}^2}{\pi(R_1C_1\omega_{REF} + \pi)} \tag{4.12}$$

Where ω_{lpf} is the loop bandwidth, ω_{REF} is the reference frequency, and R_1 and C_1 are components of the passive LF. Equ. (4.10) indicates the limitation on not only the upper bound of the loop bandwidth, but also the time constant of R_1 and C_1 for the given reference frequency .

To determine the loop filter's circuit parameters, high-level MATLAB models are developed. A second order system is first modeled to ensure PLL's stability and then using a third-order system, the final values of R_1, C_1, and C_2 are determine by placing the third pole at a high frequency in the left hand plane to filter out the high frequency spur noise . The final values for R_1, C_1, and C_2 are 5.8 MΩ , 32.5 pF, and 2.16 pF, respectively.

4.4 Voltage controlled oscillator

The VCO is the most important functional block in a DPLL. The purpose of the VCO is to convert the voltage present at the output of the loop filter into a proportional frequency [24]. A VCO topology is chosen based on its linearity criteria, frequency range, and power supply. The most commonly used design for embedded CMOS oscillators is the current starved ring oscillator. Ring oscillators also have the advantages of wider oscillation frequency range and a small die size [25]-[27]. This type of oscillator

generally consists of a number of CMOS inverter stages connected in a feedback configuration. Altering the current available to each stage, alters the drive capabilities of the inverters, and therefore controls the oscillation frequency. The voltage from the loop filter output is generally converted to a controlling current using voltage to current conversion circuitry. This is usually constructed from a current mirror arrangement coupled with a voltage to current conversion element. Simplified views of a single stage of current-starved VCO shown in figure 4.8.

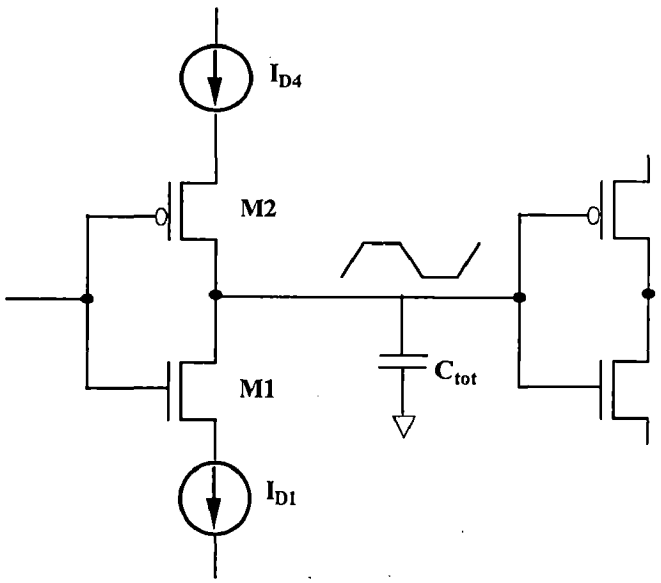


Figure 4.8 Simplified view of a single stage of the current-starved VCO

Input voltage in VCO

$$V_{inVCO} = I_{CP} * \left((1 + j\omega R_1 . C_1) \Big/ \left(j\omega (C_1 + C_2) * \left[1 + j\omega R_1 \frac{C_1 C_2}{C_1 + C_2} \right] \right) \right) \tag{4.13}$$

The average (center) current drawn by the VCO is

$$I_{avg} = I_{Dcenter} = N . \frac{V_{DD} C_{tot}}{T} = N . V_{DD} . C_{tot} . f_{osc} \tag{4.14}$$

The sizes (Width) of M2 and M1 are determined as (L is fixed)

$$I_{Dcenter} = \left(\frac{\mu_n C_{ox} W}{2L} \right) . (V_{GS} - V_{TH})^2 \tag{4.15}$$

It can be shown that the oscillation frequency is

$$f_{osc} = \frac{I_D}{N.C_{tot}.V_{DD}} \tag{4.16}$$

Where N is the number of stages and C_{tot} is the output capacitance. Gains of the VCO and PFD/charge-pump circuits are important factors in determining the loop bandwidth (BW). VCO gain is chosen based on a tradeoff between operating frequency range and loop bandwidth. VCO used in (Figure. 5.7) is a balanced seven stage, single-ended current starved ring oscillator. With V_{DD} =1.9 V, the measured VCO gain is 1.88 (rad.GHz/V) with good linearity over a range of operating frequencies from 780 to 1020 MHz. VCO tuning range and output waveform are shown in figure 5.5 and 5.9, respectively.

Frequency Synthesizer using Phase Locked loop is a feedback Control System. In such a system, the time domain performance specifications are important indices because control systems are inherently time domain systems. It is necessary to determine initially whether the system is stable or not. Equ. (3.2) implies that the output frequency step is exactly the same as the reference frequency, so a smaller reference frequency results in a higher resolution synthesizer. However, a smaller reference frequency also makes the system slower because the settling time is affected by the loop bandwidth. The relationship between the loop bandwidth, ω_n and settling time, t_s can be approximately expressed by [6]

$$t_s \approx \frac{1}{\zeta\omega_n} \ln\left(\frac{k}{M|\alpha|\sqrt{1-\zeta^2}}\right) \tag{5.1}$$

Where ζ is the damping ratio, M is the divider ratio, k is the change in divider ratio, and α is the required settling accuracy. The t_s is inversely proportional to ω_n, so increasing ω_n results in smaller steeling time in Equ. (5.1). However, ω_n is limited by the stability condition. In this chapter first we will look at the designed PLL, it is stable or not.

5.1 Loop Stability

The stability of a feedback system is related to the location of the roots of the characteristic equation of the system transfer function in the s plane. For the stability of system, values of ω_Z and ω_P given in Table 2 and calculated values of parameter given in Table 3.

Table 2: Stability Condition

For Stability	For optimal performance
$\omega_Z \leq K$	ω_Z = K/4
$\omega_P \geq K$	ω_P = 4K

We will look at root locus method to determine, whether designed PLL is stable or not

Table 3: Parameters

Parameter	Calculated value
R	5.775 M ohms
C_1	32.4675 pF
C_2	2.1654 pF
K	20 K rad/sec
I_p	100 nA

5.1.1 Root Locus of PLL

A system is stable if all the poles of the transfer function have negative real parts. We can show that all the poles of the transfer function H(s) of designed PLL, are all in the left s plane; therefore the designed system is stable. However, it is also very important to determine, how the roots of the characteristic transfer function move around in the s plane, as we change one of the parameter of the system. Usually this parameter is selected to be the gain, the bandwidth of the PLL. One method that depicts this behavior of the roots; as gain of the transfer function is increased is Root Locus. A root locus plot of the transfer function of the designed PLL is shown in Figure 5.1.

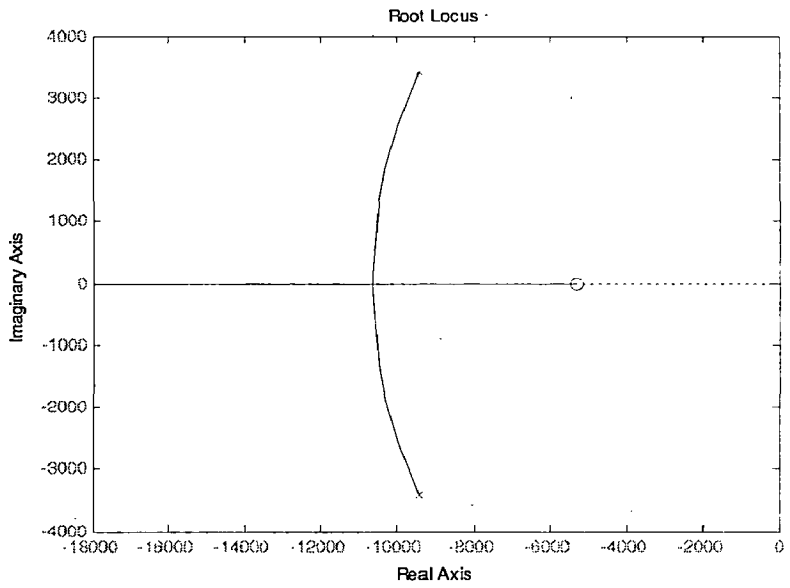


Figure 5.1 Root locus plot of second order PLL

We see as K is varied from 0 to infinity, the roots remain in the left half plane, so the system remain stable, the value of K, where the two poles split and go towards open loop zero and infinity, is the point, where the system becomes oscillatory, but is still stable.

Increasing K, thus will increase the oscillatory behavior of the system in time domain. We would discuss about this more in the subsequent section

5.1 2 Step Response of PLL

The step response of a system is basically its time domain performance. Step response of a system provides details about settling time and percent overshoot parameters. Settling time of a step response has a direct relation to the Pull-in-time parameter of the PLL. The percent overshoot provides details about system's oscillatory behavior. The relation between these two parameters is inversely proportional. We will see reducing one result in increasing the other. So the compromise is made at the best possible point to optimize the performance of the system. Figure 5.2 is the step response of the designed PLL for different values of w_z. As we showed previously that w_z should be less than K, in this plot we see how the selection of w_z for various different values affects the step response. It seems from the step response plot that, it is always best to select w_z as small as possible. This slightly slows the response, but it makes the system very stable, as overshoot is very less. However a small value of w_z implies large capacitor, and they take longer to charge during lock acquisition. Therefore a good compromise is to select $w_z = k/4$, this assures fast acquisition and the resulting step response is shown in Figure 5.2.

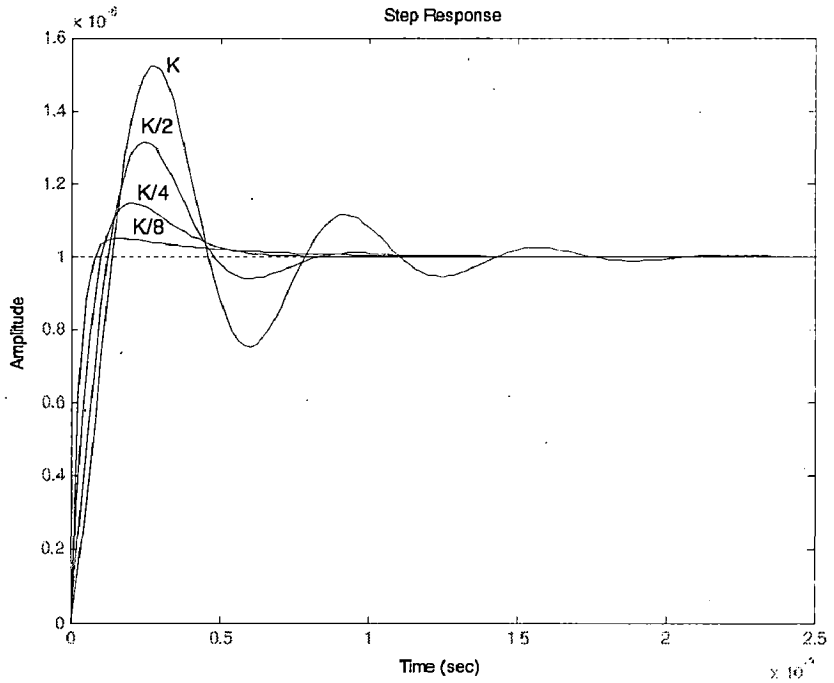


Figure 5.2 Step response of second order PLL

T-SPICE 0.18 μm CMOS Technology is used to get transient response of the entire PLL frequency synthesizer. The input reference frequency is set to 300 KHz, and measured lock time is 0.235 μs (shown in figure 5.4) at 780-1020 MHz VCO tuning range (figure 5.5).The performance of the designed Digital PLL-based frequency synthesizer is summarized in Table 4. As a comparison, The Lock time of other PLL Frequency synthesizers were 0.320 μs [21] and 0.643 μs [28].

Table 4: Result Summary

Process technology	0.18 µm CMOS technology
Supply voltage	1.9-2 V
Lock time	0.235 µs
Reference frequency	300 KHz
VCO output frequency range	780-1020 MHz
Bandwidth	20 KHz
Damping factor	0.83

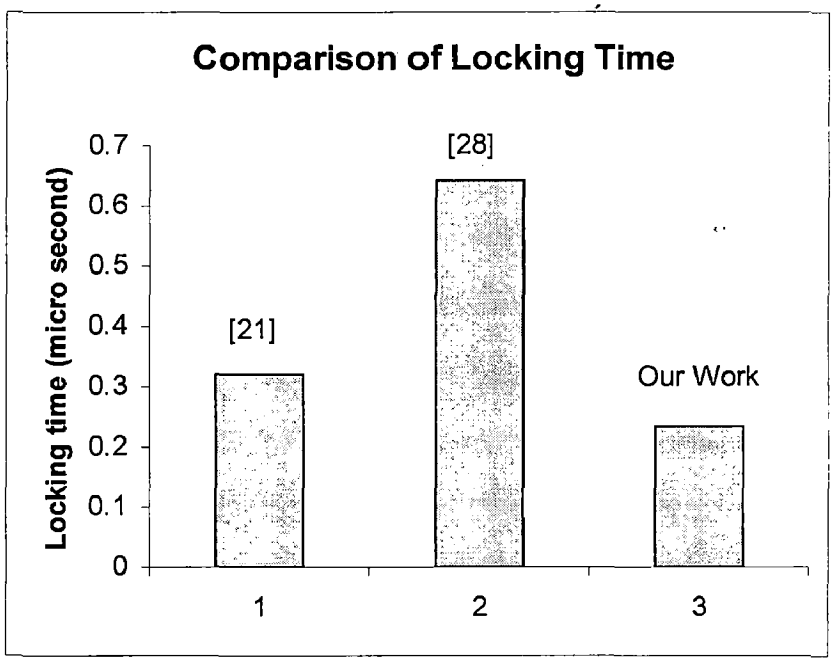


Figure 5.3 Comparison of Locking time with other's work

As expected earlier during the design stage, VCO and dual-modulus divider are the two most power-hungry components in the Digital PLL frequency synthesizer (see Figure 5.4). 44% of the total power is dissipated by the dual-modulus divider while VCO dissipates about 45% of the total share in design frequency synthesizer.

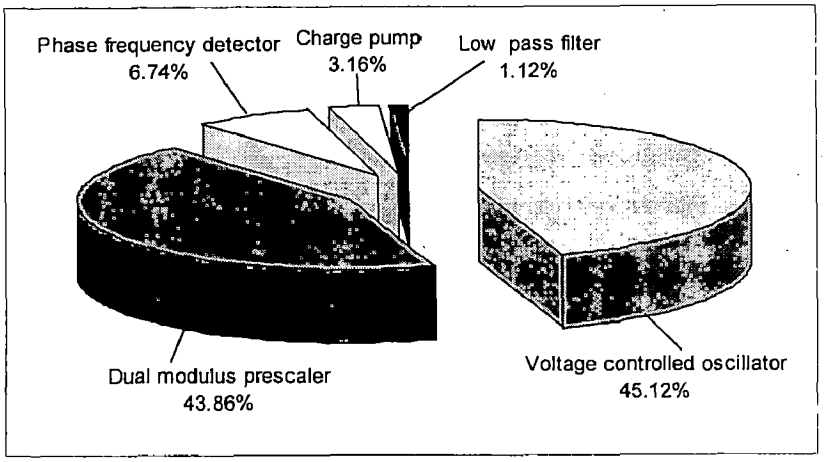


Figure 5.4 Power dissipations in each block of Frequency Synthesizer

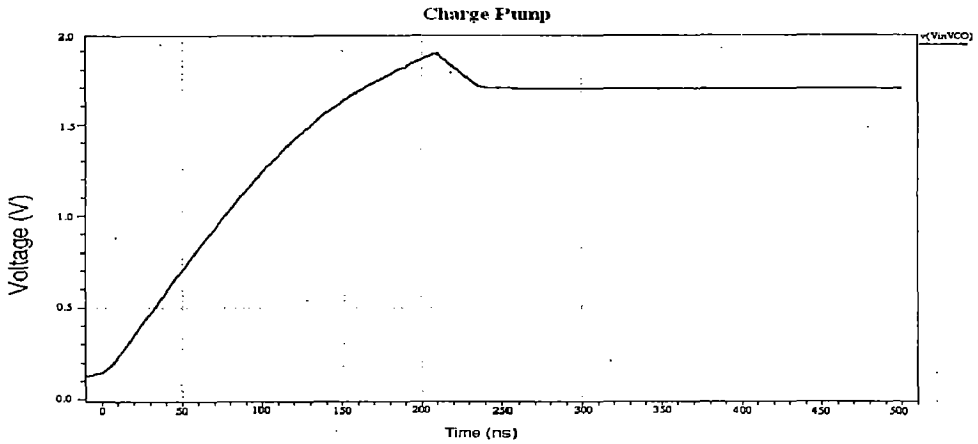


Figure 5.5 Output of charge pump and filter combination

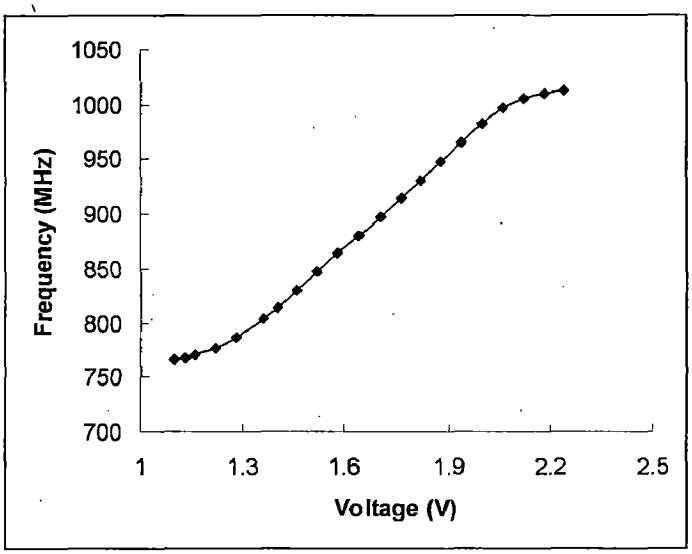


Figure 5.6 VCO Tuning range

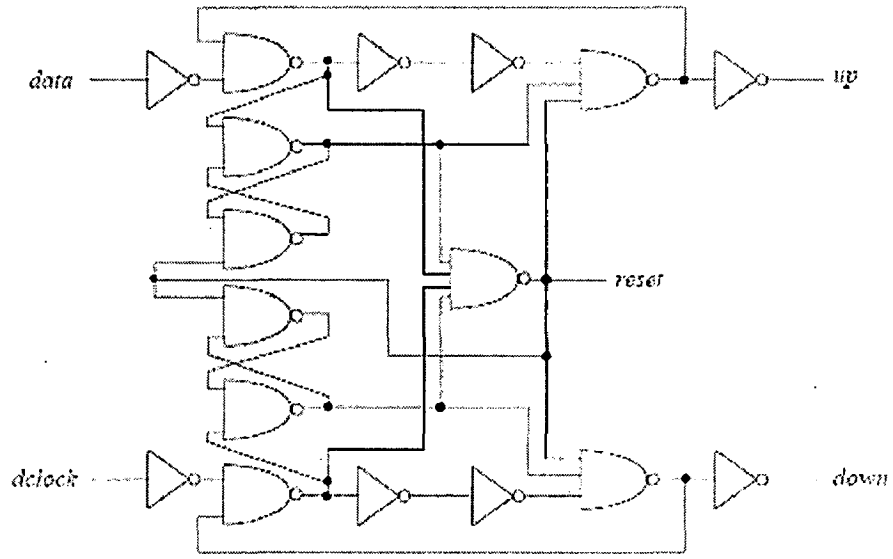


Figure 5.7 CMOS implementation of PFD

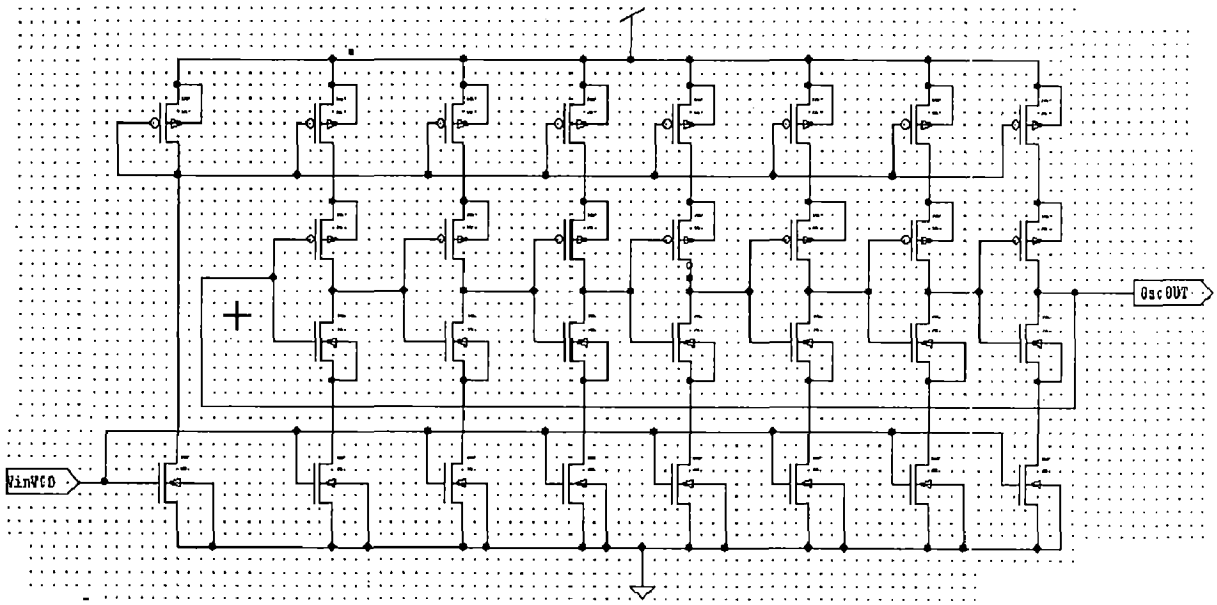


Figure 5.8 CMOS implementation of VCO

Output waveforms of phase frequency detector and voltage controlled oscillator are shown in figure 5.8 (a), (b), (c) and 5.9 respectively. Output waveforms show the results as expected.

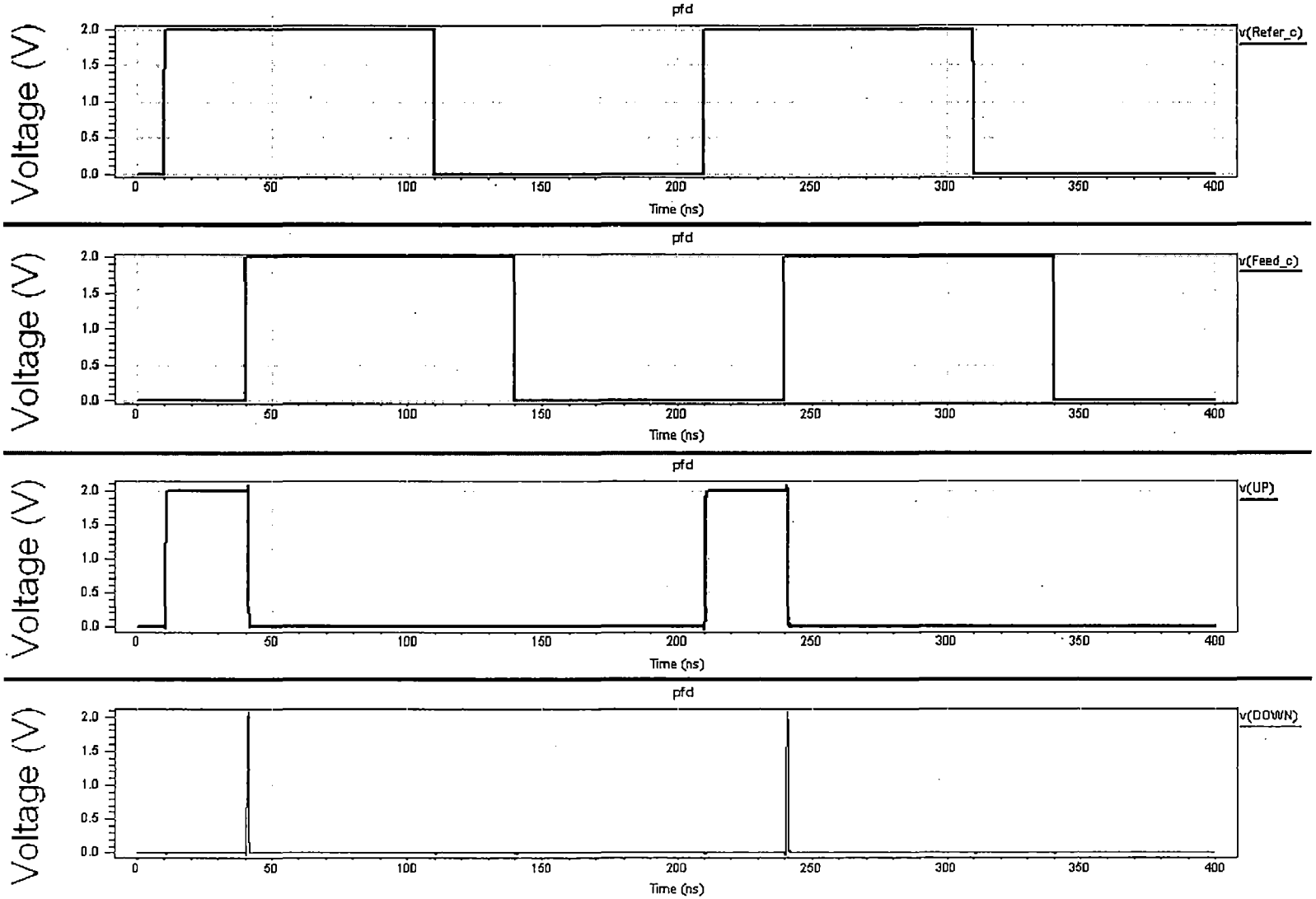


Figure 5.9 (a) Output Waveform of Phase frequency detector when F_{refer_c} is leading F_{feed_c}
Compare with figure 4.4 (a)

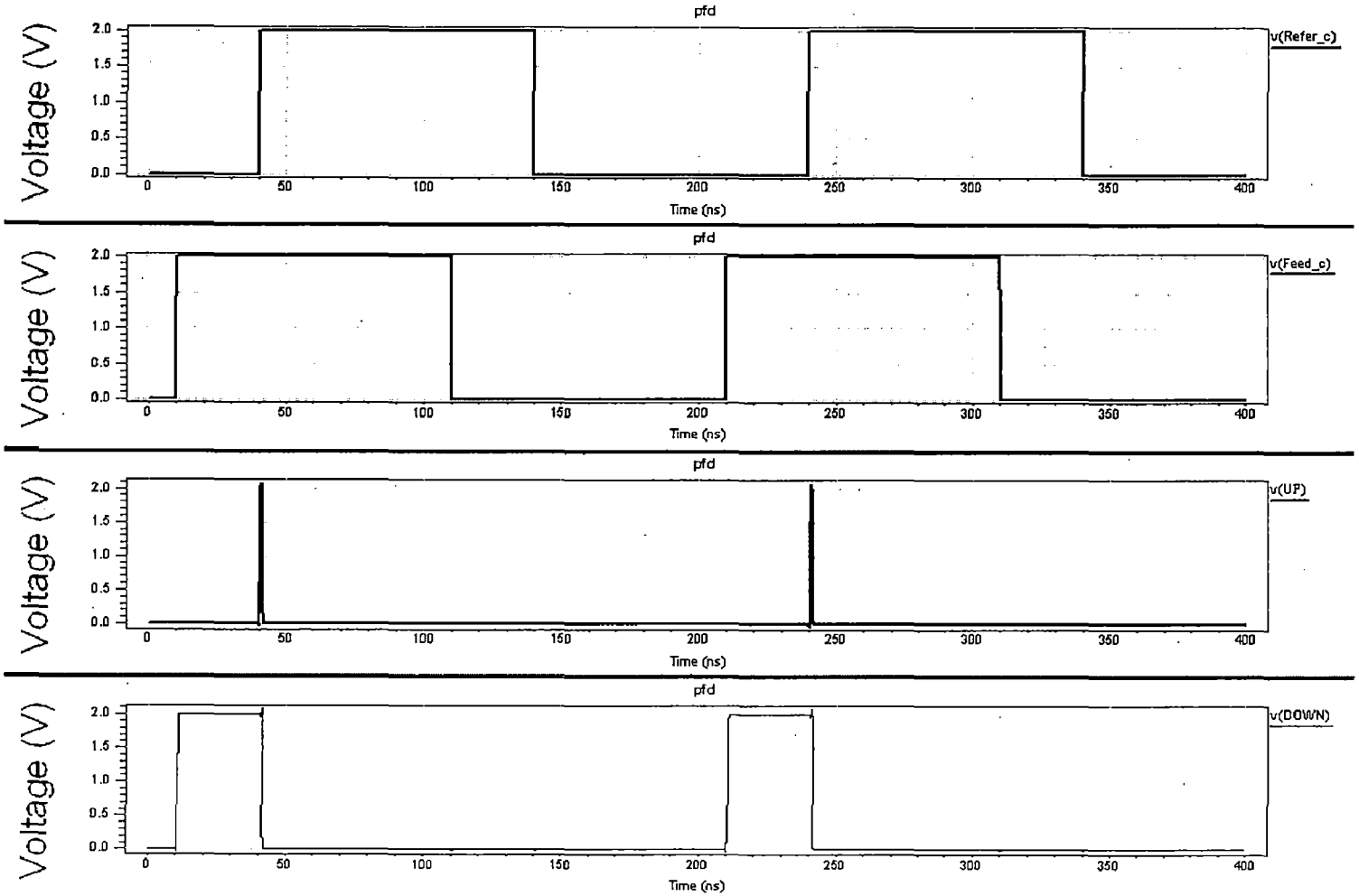


Figure 5.9 (b) Output Waveform of Phase Frequency Detector when F_{feed_c} is leading F_{refer_c}
Compare with figure 4.4 (b)

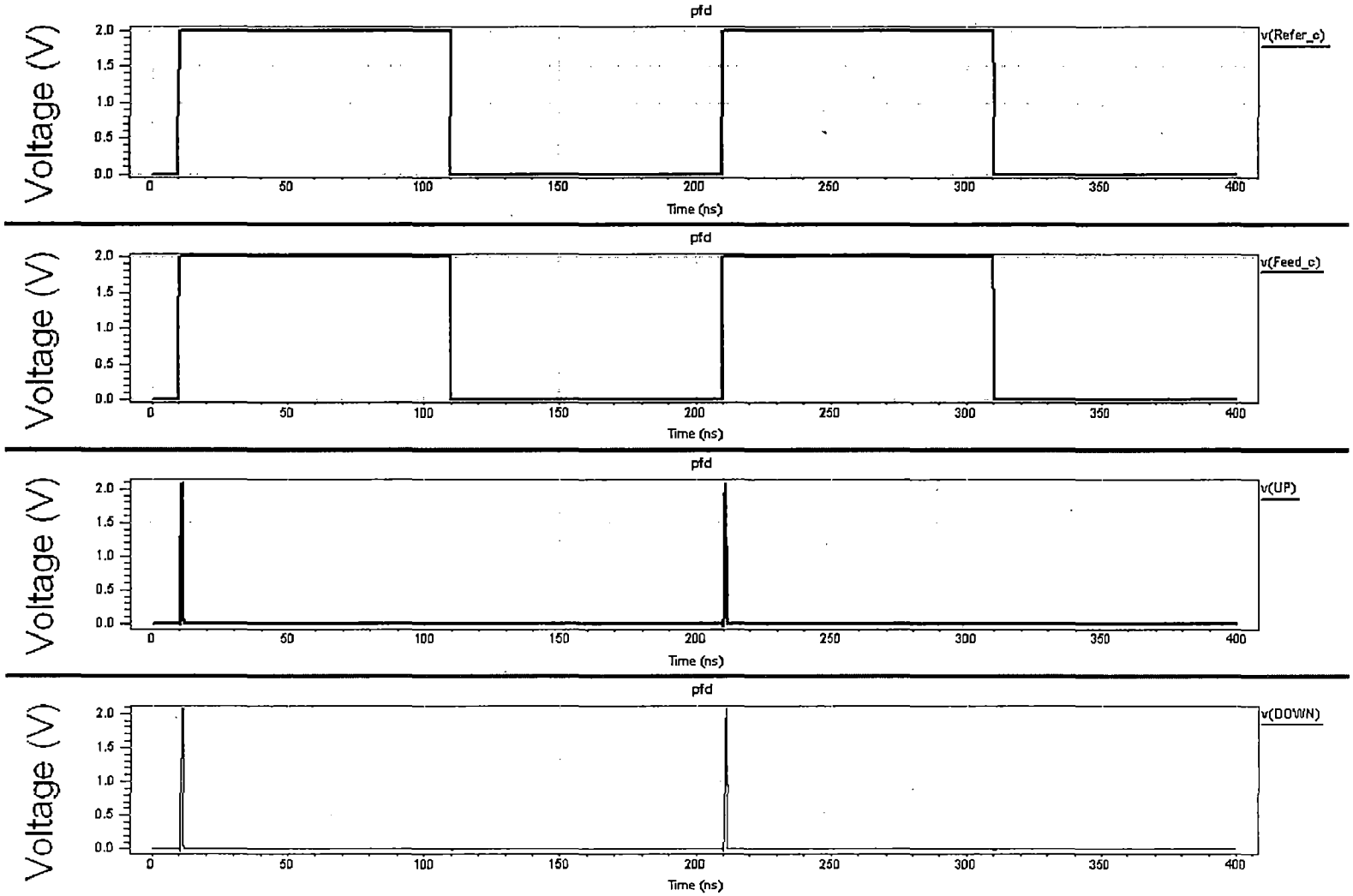


Figure 5.9 (c) Output Waveform of Phase frequency detector when F_{refer_c} and F_{feed_c} both in phase
Compare with figure 4.4(c)

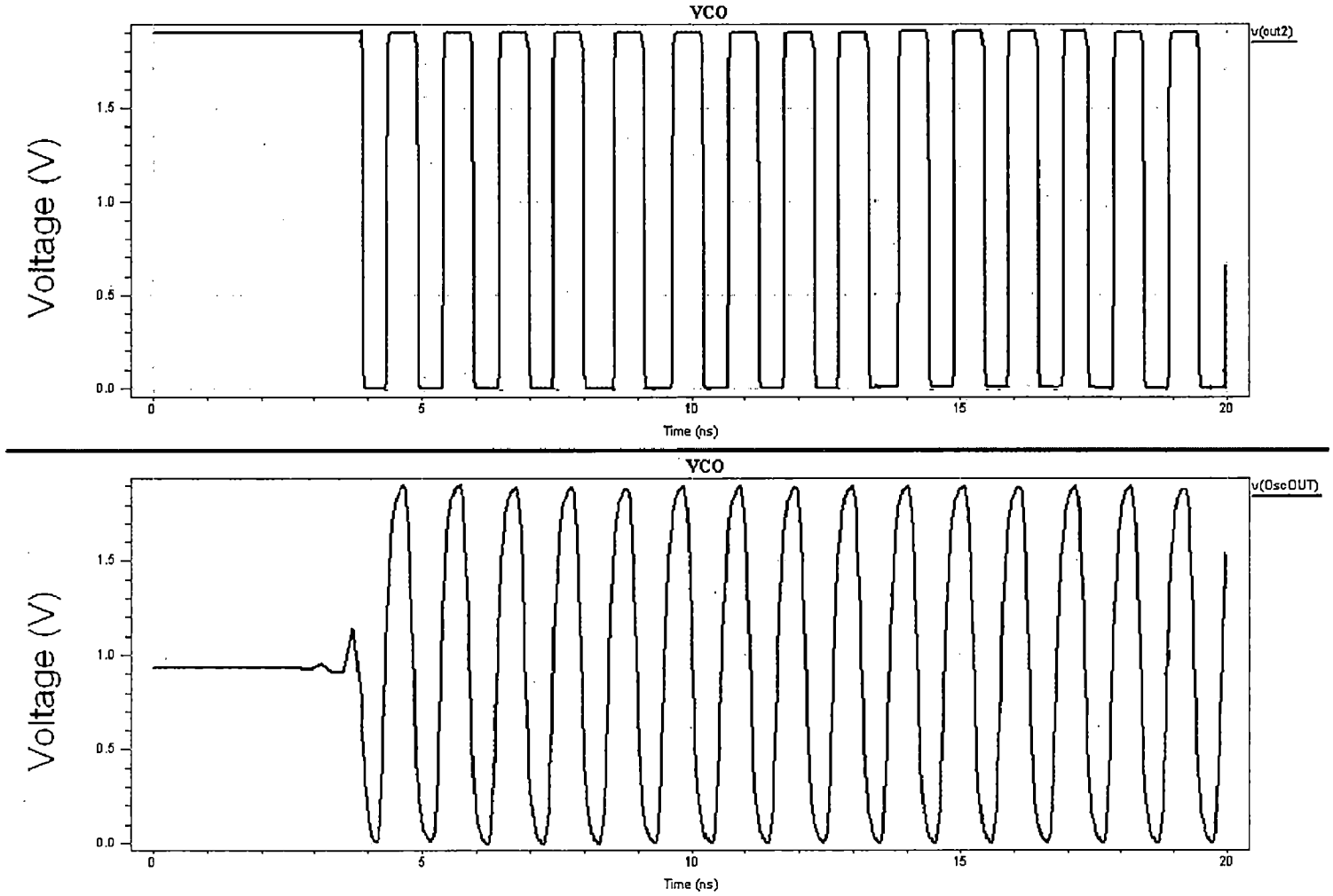


Figure 5.10 Output Waveform of Voltage controlled oscillator

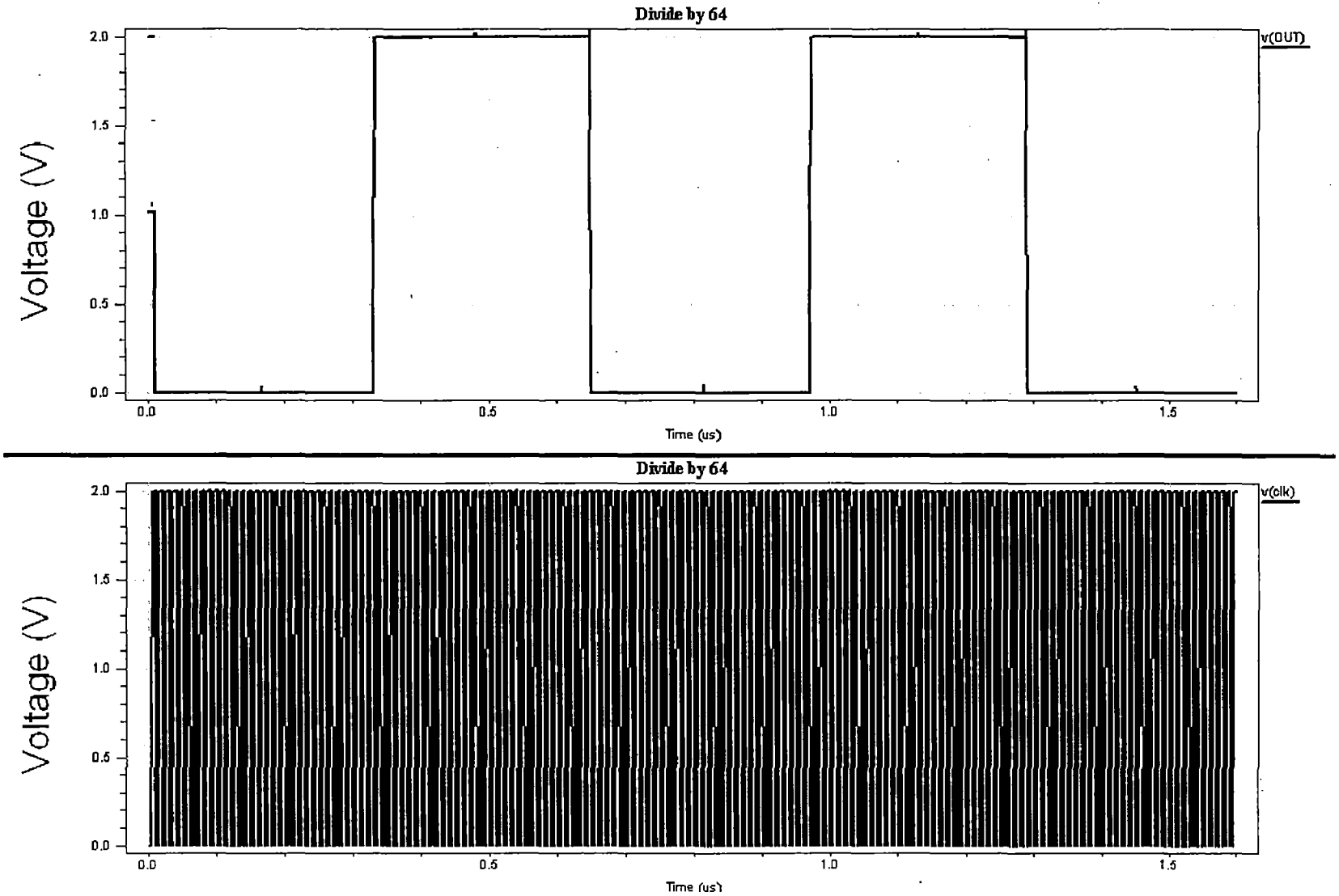


Figure 5.11 Output Waveform of Prescaler (Divide by 64 Counter)

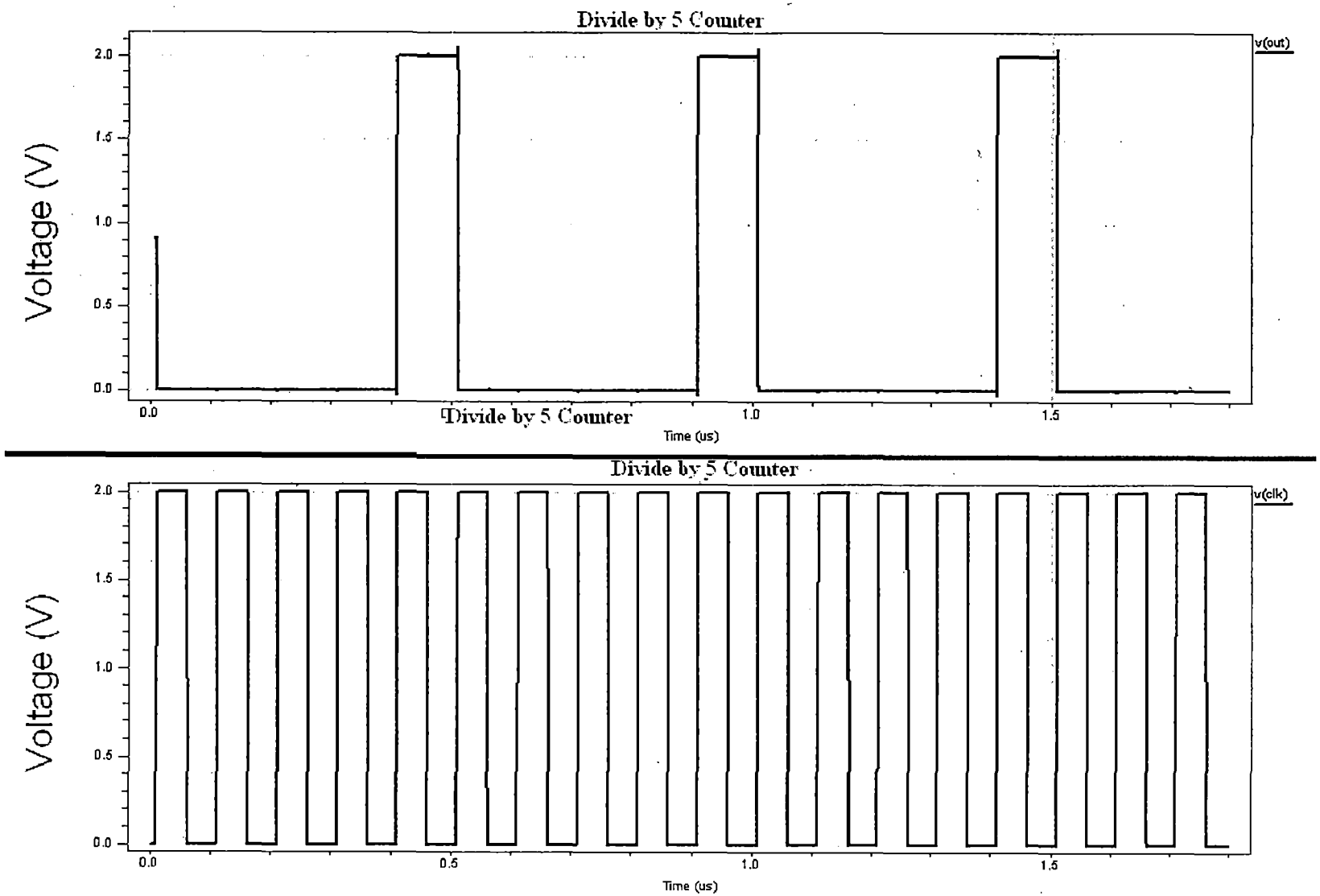


Figure 5.12 (a) Output Waveform of Divide by 5 Counter

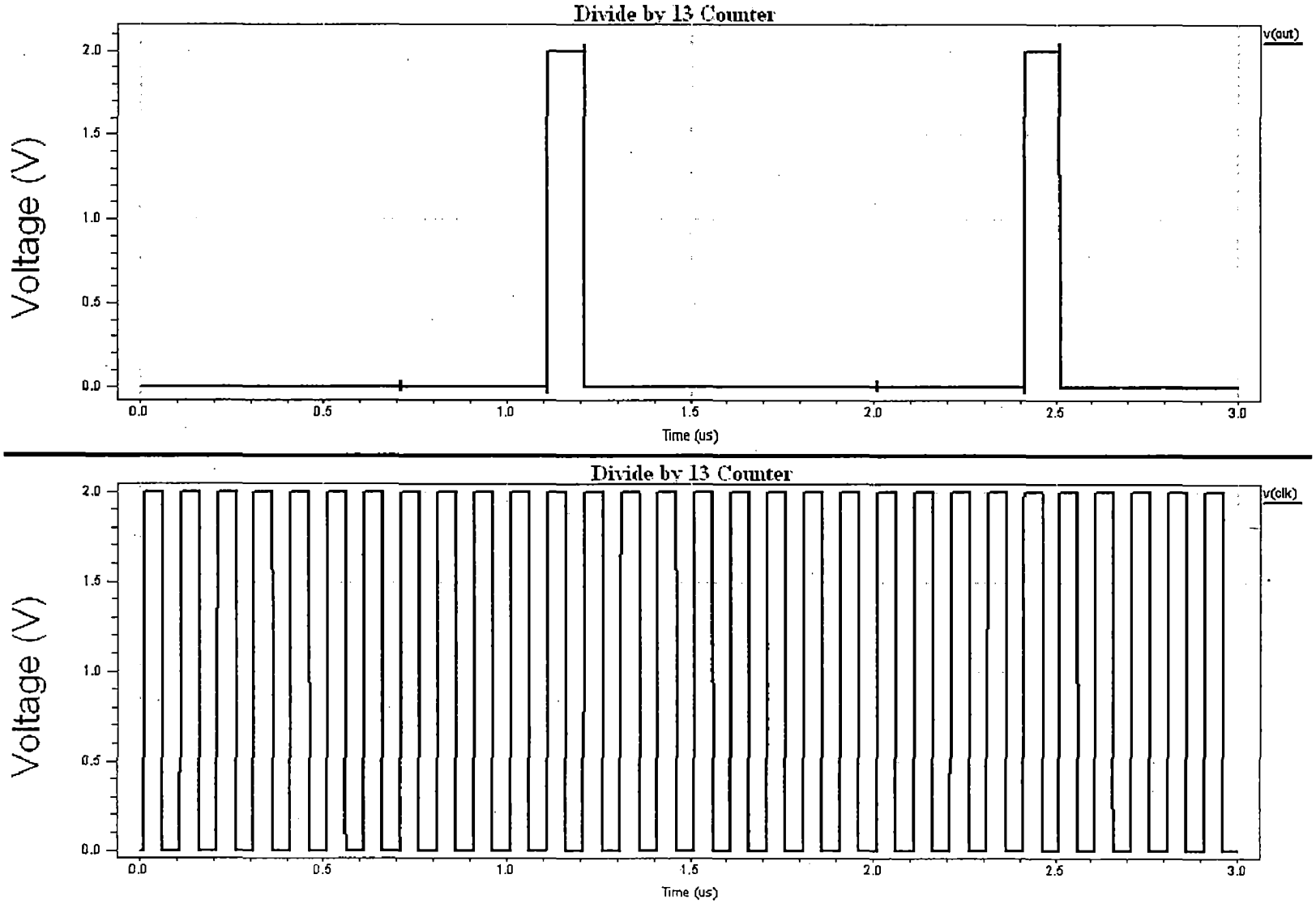


Figure 5.12 (b) Output Waveform of Divide by 13 Counter

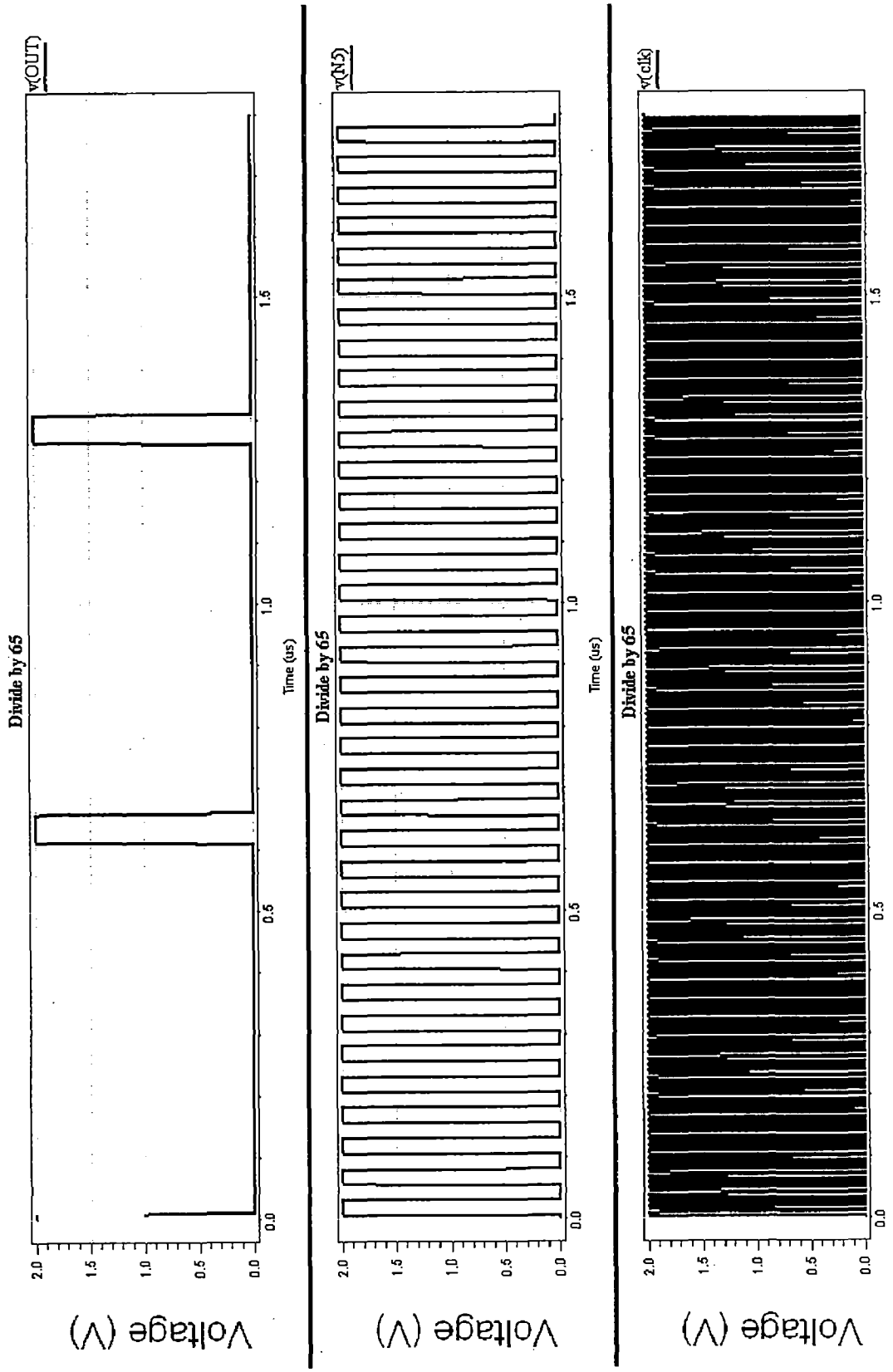


Figure 5.13 Output Waveform of Prescaler (Divide by 65 Counter)

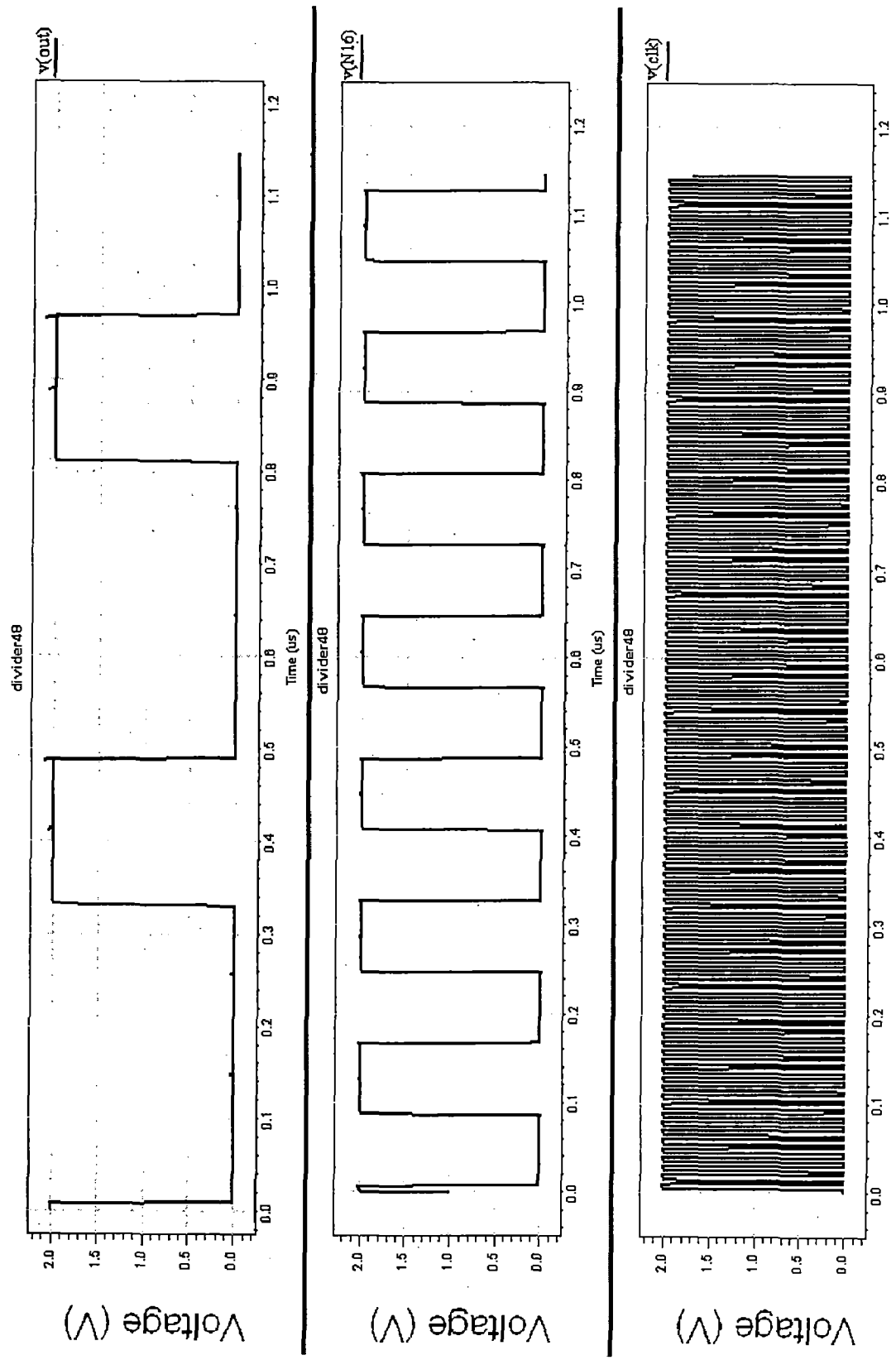


Figure 5.14 Output Waveform of Main Counter (Divide by 48 Counter)

Figure 5.15 Output Waveform of Swallow Counter (load =0)

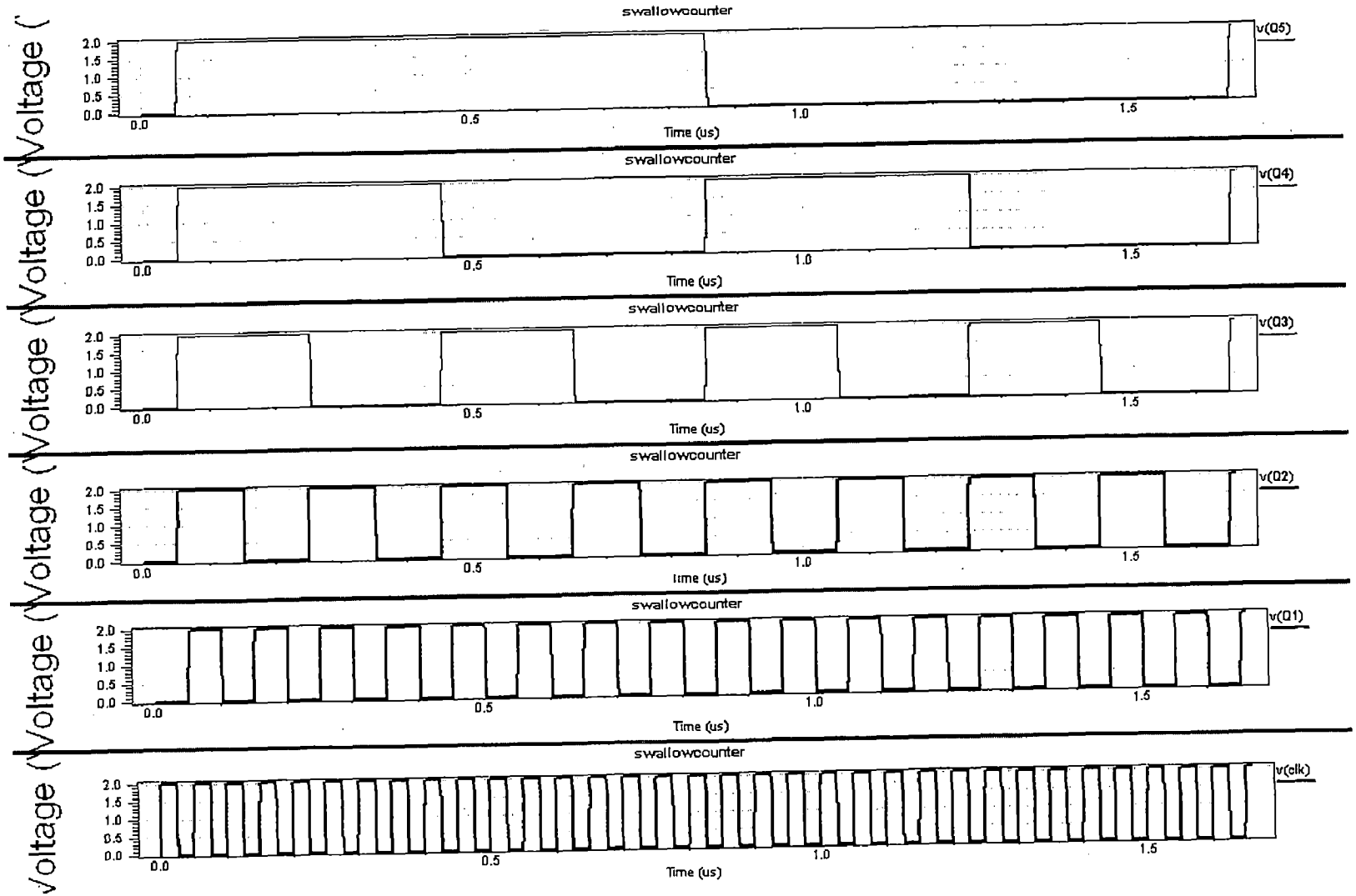


Figure 5.16 Output Waveform of Swallow Counter (load =1)

6.1 Conclusion

This thesis presents design of a Digital PLL Frequency Synthesizer for the clock generation. Simulation results of the Digital PLL Frequency Synthesizer with 0.18 μm, 2 Volts CMOS technology illustrate a locking time of 0.235 μs at 780-1020 MHz which can be use for GSM mobile communication. Key elements in this design are Phase Frequency detector (PFD), Charge pump (CP), Loop filter (Second order) and VCO which provide low locking time and high precision. PFD circuit is designed to prevent fluctuation of the charge pump under the locked condition. A small charge pump current can reduce a passive capacitance without changing loop gain so charge pump current of 100 nA is selected. The designed circuit also shows that it is possible to overcome the issue of DPLL lock time, by adjusting charge pump current and loop filter capacitor. This Digital PLL Frequency Synthesizer can be applied in modern integrated telecommunication systems and clock generators where lock time is a limiting factor and frequency multipliers are demanding.

6.2 Future Work

The subject of phase locked loop is wide and diverse. There are many other aspects that can be combined in the design to achieve better performance and more powerful.

1. Consider for instant incorporating Fault Tolerant Design Techniques to a PLL design. Since recent advances in VLSI technology has made it possible to put complex digital circuits on a single chip, more and more circuits are now combined on a single chip to make a system as compact as possible, such as a PLL Frequency synthesizer for clock generation in chip environment. As a result of this capability, it is very hard to locate an error in the event if the output of a system is not the expected one. Some of such systems are related to critical application, where it is necessary that the system operates reliably, even under the circumstances that one of the major components fails. The design techniques that make it possible for a system to be operational even under the condition of failure are termed as Fault Tolerant Design Techniques and the system as the Fault Tolerant system.

So the idea of fault tolerance is that masking up the weak points of a system, where that system may become faulty under physical defects, environmental conditions or may be because of basic design errors. We would like to suggest study and design of a Fault Tolerant PLL Frequency Synthesizer, by including both digital design and VLSI fault tolerance techniques. The incorporation of this will make it more reliable and powerful.

2. The Other aspect that was not included in this design was the Noise Analysis. Since noise is an important parameter which affects the performance of a design mostly in non-linear fashion, is necessary to accurately measure the performance of that design. Including noise consideration provide more details about the sensitive points and parameters of a design. We would like to suggest study of various noise sources in this design and its effect on the performance.

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APPENDIX

SPICE CODE FOR CIRCUITS

A1. Phase Frequency Detector

```
*phase frequency detector
.options probefilename="sedit.dat"
.include "C:\Tanner\TSpice91\models\models1\180nm.md"
.param l='.18u'

****************** CIRCUIT DESCRIPTION ********************

.SUBCKT Inv In Out Gnd Vdd
M2 Out In Gnd Gnd     NMOS W='28*l' L='2*l'
M1 Out In Vdd Vdd     PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND2 A B Out Gnd Vdd
M3 Out B N1 Gnd       NMOS W='28*l' L='2*l'
M4 N1 A Gnd Gnd       NMOS W='28*l' L='2*l'
M2 Out B Vdd Vdd      PMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd      PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND3 A B C Out Gnd Vdd
M4 Out C N1 Gnd       NMOS W='28*l' L='2*l'
M5 N1 B N2 Gnd        NMOS W='28*l' L='2*l'
M6 N2 A Gnd Gnd       NMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd      PMOS W='28*l' L='2*l'
M2 Out B Vdd Vdd      PMOS W='28*l' L='2*l'
M3 Out C Vdd Vdd      PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT Dffwreset clk Din Q Reset Gnd Vdd
XNAND2_1 N11 N1 N10 Gnd Vdd          NAND2
XNAND2_2 N1 N2 Q Gnd Vdd             NAND2
XNAND3_1 N1 clk N11 N4 Gnd Vdd       NAND3
XNAND3_2 N10 Reset clk N1 Gnd Vdd    NAND3
XNAND3_3 N4 Reset Din N11 Gnd Vdd    NAND3
XNAND3_4 Q Reset N4 N2 Gnd Vdd       NAND3
.ENDS

* Main circuit: pfd
XDffwreset_1 Refer_c D1 up reset Gnd Vdd Dffwreset
XDffwreset_2 feed_c D2 down reset Gnd Vdd Dffwreset
*XInv_1 N10 reset Gnd Vdd Inv
```

```
XNAND2_1 up down reset Gnd Vdd NAND2
* End of main circuit: pfd
****************** ANALYSIS AND PLOT ********************

vd VDD Gnd 2.0
vd1 D1 Gnd 2.0
vd2 D2 Gnd 2.0
vrefer Feed_c  Gnd  PULSE (0 2.0 10n 0 0 100n 200n)
vrefer Refer_c Gnd  PULSE (0 2.0 40n 0 0 100n 200n)
.ic v(up)=0 v(down)=0

.tran .1n 400n
.print Refer_c Feed_c UP DOWN
.End
```

A2. Charge Pump and Loop Filter

```
*charge pump circuits

.probe
.options probefilename="chargepump1.dat"
.include "C:\Tanner\TSpice91\models\models1\180nm.md"
.param l='.18u'

****************** CIRCUIT DESCRIPTION ********************

.SUBCKT Inv In Out Gnd Vdd
M2 Out In Gnd Gnd          NMOS W='14*l' L='2*l'
M1 Out In Vdd Vdd          PMOS W='28*l' L='2*l'
.ENDS

* Main circuit: Charge-pump
C1 VinVCO Gnd 10pF
XInv_1 UP N3 Gnd Vdd Inv
M2 VinVCO DOWN Gnd Gnd      NMOS W='10*l' L='1*l'
M3 VinVCO N3 Vdd Vdd        PMOS W='20*l' L='1*l'
* End of main circuit: Charge-pump
.ic v(VinVCO)=0

****************** ANALYSIS AND PLOT ********************

vd VDD Gnd 2
vup UP Gnd             PULSE (0 2 4n 0 0 20n 100n)
vdown DOWN Gnd     PULSE (0 2 23n 0 0 1n 100n)

.tran .1n 100n
.print UP DOWN VinVCO
.end
```

A3. Voltage Controlled Oscillator

```
* vco circuits
.probe
.options probefilename="vco.dat"
.include "C:\Tanner\TSpice91\models\models1\180nm.md"

****************** CIRCUIT DESCRIPTION ********************

* Main circuit: Module0
M1 N3 OscOUT N10 N10          NMOS  L=.10u W=2u
M2 N4 N3 N16 N16              NMOS  L=.10u W=2u
M3 N5 N4 N17 N17              NMOS  L=.10u W=2u
M4 N6 N5 N18 N18              NMOS  L=.10u W=2u
M5 N7 N6 N19 N19              NMOS  L=.10u W=2u
M6 N8 N7 N20 N20              NMOS  L=.10u W=2u
M7 OscOUT N8 N22 N22          NMOS  L=.10u W=2u
M8 N10 VinVCO Gnd Gnd         NMOS  L=.10u W=3u
M9 N16 VinVCO Gnd Gnd         NMOS  L=.10u W=3u
M10 N17 VinVCO Gnd Gnd        NMOS  L=.10u W=3u
M11 N18 VinVCO Gnd Gnd        NMOS  L=.10u W=3u
M12 N19 VinVCO Gnd Gnd        NMOS  L=.10u W=3u
M13 N20 VinVCO Gnd Gnd        NMOS  L=.10u W=3u
M14 N22 VinVCO Gnd Gnd        NMOS  L=.10u W=3u
M15 N23 VinVCO Gnd Gnd        NMOS  L=.10u W=3u

M16 N3 OscOUT N9 N9           PMOS  L=.10u W=6u
M17 N5 N4 N12 N12             PMOS  L=.10u W=6u
M18 N4 N3 N11 N11             PMOS  L=.10u W=6u
M19 N6 N5 N13 N13             PMOS  L=.10u W=6u
M20 N7 N6 N14 N14             PMOS  L=.10u W=6u
M21 N8 N7 N15 N15             PMOS  L=.10u W=6u
M22 OscOUT N8 N21 N21         PMOS  L=.10u W=6u
M23 N9 N23 Vdd Vdd            PMOS  L=.10u W=8u
M24 N11 N23 Vdd Vdd           PMOS  L=.10u W=8u
M25 N12 N23 Vdd Vdd           PMOS  L=.10u W=8u
M26 N13 N23 Vdd Vdd           PMOS  L=.10u W=8u
M27 N14 N23 Vdd Vdd           PMOS  L=.10u W=8u
M28 N15 N23 Vdd Vdd           PMOS  L=.10u W=8u
M29 N21 N23 Vdd Vdd           PMOS  L=.10u W=8u
M30 N23 N23 Vdd Vdd           PMOS  L=.10u W=8u
* End of main circuit: Module0

****************** ANALYSIS AND PLOT *********************

c OscOUT Gnd 10fF
vd Vdd Gnd 1.9
Vin VinVCO Gnd 1.9
```

```
.tran .1n 15n
.measure tran tp trig v(OscOUT) val=1.45 rise=2 targ v(OscOUT) val=1.45 rise=3
.print OscOUT VinVCO
.end
```

A4. Prescaler (Divide by 64)

```
* Prescaler (Divide by 64 Counter)
.probe
.options probefilename="sedit.dat"
.param l='.18u'
.include "C:\Tanner\TSpice91\models\models1\180nm.md"

****************** CIRCUIT DESCRIPTION ********************

.SUBCKT Inv A Out Gnd Vdd
M2 Out A Gnd Gnd        NMOS W='14*l' L='2*l'
M1 Out A Vdd Vdd        PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND2 A B Out Gnd Vdd
M3 Out B 1 Gnd          NMOS W='20*l' L='2*l'
M4 1 A Gnd Gnd          NMOS W='20*l' L='2*l'
M2 Out B Vdd Vdd        PMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd        PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT dff clk Din Q Qbar Gnd Vdd
XInv_1 Din N7 Gnd Vdd Inv
XNAND2_1 Din clk N11 Gnd Vdd NAND2
XNAND2_2 clk N7 N13 Gnd Vdd NAND2
XNAND2_3 N11 Qbar Q Gnd Vdd NAND2
XNAND2_4 Q N13 Qbar Gnd Vdd NAND2
.ENDS

.SUBCKT masterslave clk Din Q Qbar Gnd Vdd
Xdff_1 clk Din N7 N1 Gnd Vdd dff
Xdff_2 N8 N7 Q Qbar Gnd Vdd dff
XInv_1 clk N8 Gnd Vdd Inv
.ENDS

* Main circuit: Prescaler
Xmasterslave_1 clk N1 N6 N1 Gnd Vdd masterslave
Xmasterslave_2 N6 N5 N2 N5 Gnd Vdd masterslave
Xmasterslave_3 N2 N7 N12 N7 Gnd Vdd masterslave
Xmasterslave_4 N12 N9 N13 N9 Gnd Vdd masterslave
Xmasterslave_5 N13 N10 N14 N10 Gnd Vdd masterslave
Xmasterslave_6 N14 N11 OUT N11 Gnd Vdd masterslave
* End of main circuit: Prescaler
```

```
****************** ANALYSIS AND PLOT ********************
vd Vdd Gnd 2
Vclk clk Gnd PULSE (0 2 5n .5n .5n 5n 10n)
.tran .1n 1800n
.print clk N11 OUT
.end
```

A5. Divide by 5 Counter

```
*Divide by 5 counter
.probe
.options probefilename="dff.dat"
.include "C:\Tanner\TSpice91\models\models1\180nm.md"
.param l='.18u'

****************** CIRCUIT DESCRIPTION ********************

.SUBCKT Inv In Out Gnd Vdd
M2 Out In Gnd Gnd       NMOS W='14*l' L='2*l'
M1 Out In Vdd Vdd       PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND2 A B Out Gnd Vdd
M3 Out B 1 Gnd          NMOS W='20*l' L='2*l'
M4 1 A Gnd Gnd          NMOS W='20*l' L='2*l'
M2 Out B Vdd Vdd        PMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd        PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT XOR2 A B Out Gnd Vdd
M1 N38 B Gnd Gnd        NMOS W='22*l' L='2*l'
M2 N38 A Gnd Gnd        NMOS W='22*l' L='2*l'
M6 Out B N7 Gnd         NMOS W='22*l' L='2*l'
M5 N7 A Gnd Gnd         NMOS W='22*l' L='2*l'
M9 Out N38 Gnd Gnd      NMOS W='22*l' L='2*l'
M3 N38 B N36 Vdd        PMOS W='22*l' L='2*l'
M4 N36 A Vdd Vdd        PMOS W='22*l' L='2*l'
M7 N20 A Vdd Vdd        PMOS W='22*l' L='2*l'
M10B Out N38 N20 Vdd    PMOS W='22*l' L='2*l'
M8 N12 B Vdd Vdd        PMOS W='22*l' L='2*l'
M10 Out N38 N12 Vdd     PMOS W='22*l' L='2*l'
.ENDS

.SUBCKT dff clk Din Q Qbar Gnd Vdd
XInv_1 Din N7 Gnd Vdd Inv
XNAND2_1 Din clk N11 Gnd Vdd NAND2
XNAND2_2 clk N7 N13 Gnd Vdd NAND2
XNAND2_3 N11 Qbar Q Gnd Vdd NAND2
XNAND2_4 Q N13 Qbar Gnd Vdd NAND2
.ENDS
```

```
.SUBCKT masterslave clk Din Q Qbar Gnd Vdd
Xdff_1 N5 Din N1 N2 Gnd Vdd dff
Xdff_2 clk N1 Q Qbar Gnd Vdd dff
XInv_1 clk N5 Gnd Vdd Inv
.ENDS

* Main circuit: divide by 5
XInv_1 N13 N3 Gnd Vdd Inv
XInv_2 N1 N11 Gnd Vdd Inv
Xmasterslave_1 clk N3 N14 N15 Gnd Vdd masterslave
Xmasterslave_2 clk N7 N16 N5 Gnd Vdd masterslave
Xmasterslave_3 clk N11 out N9 Gnd Vdd masterslave
XNAND2_1 N15 N9 N13 Gnd Vdd NAND2
XNAND2_2 N16 N14 N1 Gnd Vdd NAND2
XXOR2_1 N16 N14 N7 Gnd Vdd XOR2
* End of main circuit: divide by 5

****************** ANALYSIS AND PLOT ********************

vd Vdd gnd 2
.ic v(out)=0
vclk clk Gnd  PULSE (0 2 10n 1n 1n 50n 100n)

.tran 1n 1800n
.print clk out
.end
```

A6. Divide by 13 Counter

```
* Divide by 13 counter
.probe
.options probefilename="dff.dat"
.include "C:\Tanner\TSpice91\models\models1\180nm.md"
.param l='.18u'

****************** CIRCUIT DESCRIPTION ********************

.SUBCKT Inv In Out Gnd Vdd
M2 Out In Gnd Gnd       NMOS W='14*l' L='2*l'
M1 Out In Vdd Vdd       PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND2 A B Out Gnd Vdd
M3 Out B 1 Gnd          NMOS W='20*l' L='2*l'
M4 1 A Gnd Gnd          NMOS W='20*l' L='2*l'
M2 Out B Vdd Vdd        PMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd        PMOS W='28*l' L='2*l'
```

```
.ENDS

.SUBCKT NAND3 A B C Out Gnd Vdd
M4 Out C 1 Gnd      NMOS W='20*l' L='2*l'
M5 1 B 2 Gnd        NMOS W='20*l' L='2*l'
M6 2 A Gnd Gnd      NMOS W='20*l' L='2*l'
M1 Out A Vdd Vdd    PMOS W='28*l' L='2*l'
M2 Out B Vdd Vdd    PMOS W='28*l' L='2*l'
M3 Out C Vdd Vdd    PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND4 A B C D Out Gnd Vdd
M5 Out D 1 Gnd      NMOS W='20*l' L='2*l'
M6 1 C 2 Gnd        NMOS W='20*l' L='2*l'
M7 2 B 3 Gnd        NMOS W='20*l' L='2*l'
M8 3 A Gnd Gnd      NMOS W='20*l' L='2*l'
M1 Out A Vdd Vdd    PMOS W='28*l' L='2*l'
M2 Out B Vdd Vdd    PMOS W='28*l' L='2*l'
M3 Out C Vdd Vdd    PMOS W='28*l' L='2*l'
M4 Out D Vdd Vdd    PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT dff clk Din Q Qbar Gnd Vdd
XInv_1 Din N7 Gnd Vdd Inv
XNAND2_1 Din clk N11 Gnd Vdd NAND2
XNAND2_2 clk N7 N13 Gnd Vdd NAND2
XNAND2_3 N11 Qbar Q Gnd Vdd NAND2
XNAND2_4 Q N13 Qbar Gnd Vdd NAND2
.ENDS

.SUBCKT masterslave clk Din Q Qbar Gnd Vdd
Xdff_1 N5 Din N1 N2 Gnd Vdd dff
Xdff_2 clk N1 Q Qbar Gnd Vdd dff
XInv_1 clk N5 Gnd Vdd Inv
.ENDS

.SUBCKT XOR2 A B Out Gnd Vdd
M1 N38 B Gnd Gnd NMOS W='18*l' L='2*l'
M2 N38 A Gnd Gnd NMOS W='18*l' L='2*l'
M6 Out B N7 Gnd NMOS W='18*l' L='2*l'
M5 N7 A Gnd Gnd NMOS W='18*l' L='2*l'
M9 Out N38 Gnd Gnd NMOS W='18*l' L='2*l'
M3 N38 B N36 Vdd PMOS W='22*l' L='2*l'
M4 N36 A Vdd Vdd PMOS W='22*l' L='2*l'
M7 N20 A Vdd Vdd PMOS W='22*l' L='2*l'
M10B Out N38 N20 Vdd PMOS W='22*l' L='2*l'
M8 N12 B Vdd Vdd PMOS W='22*l' L='2*l'
M10 Out N38 N12 Vdd PMOS W='22*l' L='2*l'
.ENDS
```

```
* Main circuit: Divide by 13 counter
XInv_1 N7 out Gnd Vdd Inv
Xmasterslave_1 clk N16 N2 N9 Gnd Vdd masterslave
Xmasterslave_2 clk N8 N6 N5 Gnd Vdd masterslave
Xmasterslave_3 clk N15 N10 N11 Gnd Vdd masterslave
Xmasterslave_4 clk N19 N24 N20 Gnd Vdd masterslave
XNAND2_1 N11 N9 N3 Gnd Vdd NAND2
XNAND2_2 N20 N9 N4 Gnd Vdd NAND2
XNAND2_3 N3 N4 N16 Gnd Vdd NAND2
XNAND2_4 N11 N24 N18 Gnd Vdd NAND2
XNAND2_5 N17 N18 N19 Gnd Vdd NAND2
XNAND3_1 N5 N10 N20 N14 Gnd Vdd NAND3
XNAND3_2 N2 N6 N11 N12 Gnd Vdd NAND3
XNAND3_3 N9 N10 N20 N13 Gnd Vdd NAND3
XNAND3_4 N14 N12 N13 N15 Gnd Vdd NAND3
XNAND3_5 N2 N6 N10 N17 Gnd Vdd NAND3
XNAND4_1 N5 N9 N10 N24 N7 Gnd Vdd NAND4
XXOR2_1 N2 N6 N8 Gnd Vdd XOR2
* End of main circuit: Divide by 13 counter


********** ANALYSIS AND PLOT **********

vd Vdd gnd 2
vclk clk Gnd  PULSE (0 2 10n 0 0 50n 100n)
.ic v(N2)=0, v(N6)=0, v(N10)=0, v(N24)=0
.tran 1n 3000n
.print clk out
.end
```

A7. Main counter

```
* Main counter (Divide by 48)
.probe
.options probefilename="sedit.dat"
.include "C:\Tanner\TSpice91\models\models1\180nm.md"
.param l='.18u'

********** CIRCUIT DESCRIPTION **********

.SUBCKT Inv A Out Gnd Vdd
M2 Out A Gnd Gnd      NMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd      PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND2 A B Out Gnd Vdd
M3 Out B 1 Gnd        NMOS W='28*l' L='2*l'
M4 1 A Gnd Gnd        NMOS W='28*l' L='2*l'
M2 Out B Vdd Vdd      PMOS W='28*l' L='2*l'
```

```
M1 Out A Vdd Vdd    PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT dff clk Din Q Qbar Gnd Vdd
XInv_1 Din N7 Gnd Vdd Inv
XNAND2_1 Din clk N11 Gnd Vdd NAND2
XNAND2_2 clk N7 N13 Gnd Vdd NAND2
XNAND2_3 N11 Qbar Q Gnd Vdd NAND2
XNAND2_4 Q N13 Qbar Gnd Vdd NAND2
.ENDS

.SUBCKT masterslave clk Din Q Qbar Gnd Vdd
Xdff_1 N8 Din N2 N1 Gnd Vdd dff
Xdff_2 clk N2 Q Qbar Gnd Vdd dff
XInv_1 clk N8 Gnd Vdd Inv
.ENDS

.SUBCKT XOR2 A B Out Gnd Vdd
M1 N38 B Gnd Gnd        NMOS W='22*l' L='2*l'
M2 N38 A Gnd Gnd        NMOS W='22*l' L='2*l'
M6 Out B N7 Gnd         NMOS W='22*l' L='2*l'
M5 N7 A Gnd Gnd         NMOS W='22*l' L='2*l'
M9 Out N38 Gnd Gnd      NMOS W='22*l' L='2*l'
M3 N38 B N36 Vdd        PMOS W='22*l' L='2*l'
M4 N36 A Vdd Vdd        PMOS W='22*l' L='2*l'
M7 N20 A Vdd Vdd        PMOS W='22*l' L='2*l'
M10B Out N38 N20 Vdd    PMOS W='22*l' L='2*l'
M8 N12 B Vdd Vdd        PMOS W='22*l' L='2*l'
M10 Out N38 N12 Vdd     PMOS W='22*l' L='2*l'
.ENDS

* Main circuit: divide by 48
Xmasterslave_1 clk N1 N15 N1 Gnd Vdd masterslave
Xmasterslave_2 N1 N3 N4 N3 Gnd Vdd masterslave
Xmasterslave_3 N3 N6 N5 N6 Gnd Vdd masterslave
Xmasterslave_4 N6 N10 N11 N10 Gnd Vdd masterslave
Xmasterslave_5 N11 out N16 N7 Gnd Vdd masterslave
Xmasterslave_6 N11 N2 out N12 Gnd Vdd masterslave
XXOR2_1 out N16 N2 Gnd Vdd XOR2
* End of main circuit: divide by 48

********** ANALYSIS AND PLOT **********

vd Vdd gnd 2
vclk clk  Gnd  PULSE (0 2 5n .5n .5n 5n 10n)
.ic v(out)=0, V(N11)=0
.tran .1n 800n
.print clk out N11
.End
```

A8. Swallow Counter

```
* Swallow counter
.probe
.options probefilename="logicblock.dat"
.include "C:\Tanner\TSpice91\models\models1\180nm.md"
.param l='.18u'

****************** CIRCUIT DESCRIPTION ********************

.SUBCKT XNOR2 A B Out Gnd Vdd
M3 1 A 2 Gnd          NMOS W='22*l' L='2*l'
M4 2 B Gnd Gnd        NMOS W='22*l' L='2*l'
M10B Out 1 4b Gnd     NMOS W='22*l' L='2*l'
M7 4b B Gnd Gnd       NMOS W='22*l' L='2*l'
M10 Out 1 4 Gnd       NMOS W='22*l' L='2*l'
M8 4 A Gnd Gnd        NMOS W='22*l' L='2*l'
M1 1 A Vdd Vdd        PMOS W='22*l' L='2*l'
M2 1 B Vdd Vdd        PMOS W='22*l' L='2*l'
M5 3 B Vdd Vdd        PMOS W='22*l' L='2*l'
M6 Out A 3 Vdd        PMOS W='22*l' L='2*l'
M9 Out 1 Vdd Vdd      PMOS W='22*l' L='2*l'
.ENDS

.SUBCKT Inv A Out Gnd Vdd
M2 Out A Gnd Gnd    NMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd    PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND2 A B Out Gnd Vdd
M3 Out B 1 Gnd        NMOS W='28*l' L='2*l'
M4 1 A Gnd Gnd        NMOS W='28*l' L='2*l'
M2 Out B Vdd Vdd      PMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd      PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND3 A B C Out Gnd Vdd
M4 Out C 1 Gnd        NMOS W='28*l' L='2*l'
M5 1 B 2 Gnd          NMOS W='28*l' L='2*l'
M6 2 A Gnd Gnd        NMOS W='28*l' L='2*l'
M1 Out A Vdd Vdd      PMOS W='28*l' L='2*l'
M2 Out B Vdd Vdd      PMOS W='28*l' L='2*l'
M3 Out C Vdd Vdd      PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT NAND4 A B C D Out Gnd Vdd
M5 Out D 1 Gnd          NMOS W='28*l' L='2*l'
M6 1 C 2 Gnd            NMOS W='28*l' L='2*l'
M7 2 B 3 Gnd            NMOS W='28*l' L='2*l'
M8 3 A Gnd Gnd          NMOS W='28*l' L='2*l'
```

```
M1 Out A Vdd Vdd        PMOS W='28*l' L='2*l'
M2 Out B Vdd Vdd        PMOS W='28*l' L='2*l'
M3 Out C Vdd Vdd        PMOS W='28*l' L='2*l'
M4 Out D Vdd Vdd        PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT dff clk Din Q Qbar Gnd Vdd
XInv_1 Din N7 Gnd Vdd Inv
XNAND2_1 Din clk N11 Gnd Vdd NAND2
XNAND2_2 clk N7 N13 Gnd Vdd NAND2
XNAND2_3 N11 Qbar Q Gnd Vdd NAND2
XNAND2_4 Q N13 Qbar Gnd Vdd NAND2
.ENDS

.SUBCKT masterslave clk Din Q Qbar Gnd Vdd
Xdff_1 N8 Din N7 N1 Gnd Vdd dff
Xdff_2 clk N7 Q Qbar Gnd Vdd dff
XInv_1 clk N8 Gnd Vdd Inv
.ENDS

.SUBCKT NOR2 A B Out Gnd Vdd
M4 Out B Gnd Gnd        NMOS W='28*l' L='2*l'
M3 Out A Gnd Gnd        NMOS W='28*l' L='2*l'
M2 Out B 1 Vdd          PMOS W='28*l' L='2*l'
M1 1 A Vdd Vdd          PMOS W='28*l' L='2*l'
.ENDS

.SUBCKT Module0 OUT W X Y Z Gnd Vdd
XInv_1 N2 N8 Gnd Vdd Inv
XInv_2 N9 N5 Gnd Vdd Inv
XInv_3 N1 OUT Gnd Vdd Inv
XNAND2_1 X Y N2 Gnd Vdd NAND2
XNAND2_2 Z W N9 Gnd Vdd NAND2
XNOR2_1 N8 N5 N1 Gnd Vdd NOR2
.ENDS

* Main circuit: Swallow counter
XInv_1 load N4 Gnd Vdd Inv
XInv_2 N19 N8 Gnd Vdd Inv
XInv_3 N26 N6 Gnd Vdd Inv
XInv_4 N27 N10 Gnd Vdd Inv
Xmasterslave_1 clk N5 Q1 Q1bar Gnd Vdd masterslave
Xmasterslave_2 clk N9 Q2 Q2bar Gnd Vdd masterslave
Xmasterslave_3 clk N13 Q3 Q3bar Gnd Vdd masterslave
Xmasterslave_4 clk N15 Q4 Q4bar Gnd Vdd masterslave
Xmasterslave_5 clk N16 Q5 Q5bar Gnd Vdd masterslave
XModule0_1 N5 Q1bar N4 I1 load Gnd Vdd Module0
XModule0_2 N9 N7 N4 I2 load Gnd Vdd Module0
XModule0_3 N13 N2 N4 I3 load Gnd Vdd Module0
XModule0_4 N15 N1 N4 I4 load Gnd Vdd Module0
```

```
XModule0_5 N16 N11 N4 I5 load Gnd Vdd Module0
XNAND2_1 Q2bar Q1bar N19 Gnd Vdd NAND2
XNAND3_1 Q3bar Q2bar Q1bar N26 Gnd Vdd NAND3
XNAND4_1 Q4bar Q3bar Q2bar Q1bar N27 Gnd Vdd NAND4
XXNOR2_1 N6 Q4bar N1 Gnd Vdd XNOR2
XXNOR2_2 N8 Q3bar N2 Gnd Vdd XNOR2
XXNOR2_3 Q1bar Q2bar N7 Gnd Vdd XNOR2
XXNOR2_4 N10 Q5bar N11 Gnd Vdd XNOR2
* End of main circuit: Swallow counter

******************** ANALYSIS AND PLOT **********************

vd Vdd Gnd 2
vload load Gnd bit ({01111 11111} on=2.0 off=0.0 pw=90n rt=1n ft=1n)
vI1 I1 Gnd 0
vI2 I2 Gnd 0
vI3 I3 Gnd 2
vI4 I4 Gnd 0
vI5 I5 Gnd 0
vclk clk  Gnd  PULSE (0 2 10n 1n 1n 25n 50n)
.tran .1n 1500n
.print clk Q1 Q2 Q3 Q4 Q5
.End
```