STUDY OF HIGH-K DIELECTRICS FOR MIS CAPACITOR APPLICATIONS

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

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ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialzation in Micro Electronics & VLSI Technology)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation report, entitled **"Study of High-K Dielectrics For MIS Capacitor Applications",** is being submitted in partial fulfilment of the requirements for the award of the degree of **Master of Technology** in **Microelectronics and VLSI,** in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work, carried out from June 2010 to June 2011, under guidance and supervision of **Dr. Sanjeev Kumar Manhas,** Assistant Professor and **Dr. Ashok Kumar Saxena,** Professor, Department of Electronics and Computer Engineering and **Dr. Ramesh Chandra,** Associate Professor Institute Instrumentation Centre, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not submitted for the award of any other Degree or Diploma.

Date: 30/6/11 V. Siva Krishna

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CERTIFICATE

This is to certify that the statement made by the candidate is correct to best of my knowledge and belief.

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May God keep you all well and smiling always.

ABSTRACT

Scaling of integrated circuits (IC) into nanoscale technology node requires a gate dielectric material of thickness near to $20A^0$. This ultrathin feature shows evidences of a large direct tunnelling current into gate. To reduce this tunnelling effect high-k dielectrics which have large dielectric constant compared to SiO_2 are investigated in many literatures. However a manufacurable solution of high-k material for nanoscale technology is not available. In this dissertation, to investigate the properties of gate dielectric materials MIS capacitors, Al/HfO_2/p-Si, Al/ZrO_2/p-Si and laminated structures of Al/ZrO_2/HfO_2/p-Si and Al/HfO_2/ZRO_2/p-Si, are fabricated using RF Magnetron sputtering. Electrical and physical characterization is studied with variation in annealing temperature and reliability nature. The reliability characteristics are made in case of binary and laminated MIS capacitors. Results shows high-k materials (ZrO_2, HfO_2) with dielectric constant 15-22 are reported. Study of annealing shows HfO_2 coated films tend to poly crystalline nature from amorphous at 450^0C annealing with N_2. From the electrical characterization decrease in positive oxide charge present inside the dielectric material is reported. Reliability analysis shows degradation of dielectric performance is mainly due to induced oxide charges inside the dielectric. This effect is observed in both binary and bilayer structures of ZrO_2 and HfO_2.

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CHAPTER 1

INTRODUCTION AND LETERATURE REVIEW

1.1 Need For High-k Dielectric Materials

Scaling trends of integrated circuits are defined by G.E. Moore in his famous article are known after as "Moore's Law" [1]. Moore's Law predicts the number of transistors on an integrated circuit (IC) will be double in each 24 months. This is considered as a self fulfilling prediction as the semiconductor industry accepted this scaling trend as a roadmap and set their goals accordingly. It explains how integrated device complexity increases by time in order to meet goals for performance and device costs.

The need for high-k gate dielectric has been described in numerous scientific reports [3-14]. The gate capacitance is one of the key factors for determining Metal Oxide Semiconductor Field Effect Transistor (MOSFET) performance [17]. The gate capacitance in scaled MOSFETs has to be kept high for good control of the inversion charge by the gate voltage. Large capacitance with smaller area is achieved by diminishing the dielectric thickness or enhancing the dielectric constant. According to the parallel plat capacitor relation which is defined as

$$C = \frac{Ak\varepsilon_0}{t_{ox}} \tag{1.1}$$

where, C is the capacitance, A is capacitor area, t_{ox} is the oxide thickness, ε_0 is permitttivity of free space and k is the relative dileectric constant of oxide.

Conventional dielectrics (SiO_2 or SiON) with low dielectric constant show unacceptably high tunneling currents. Therefore a thicker oxide layer capable of limiting direct tunneling is compulsory to meet the leakage currents requirements [2, 3]. In other words, for a given oxide thickness, there is no other way that using high dielectric constant, i.e. high-k material for maintaining the high capacitance level.

The SiO_2 (with a k value of 3.9) equivalent oxide thickness (EOT) of high-k dielectric materials can be written as

$$EOT = t_{high-k}\frac{3.9}{k_{high-k}} \quad (1.2)$$

where k_{high-k} is relative dielectric constant of dielectric with a physical thickness of t_{high-k}.

Figure 1.1 illustrates how the dielectric layer thickness changes by replacing SiO_2 with high-k material with the same EOT. Increase in physical thickness is the key for the leakage current reduction with high-k materials.

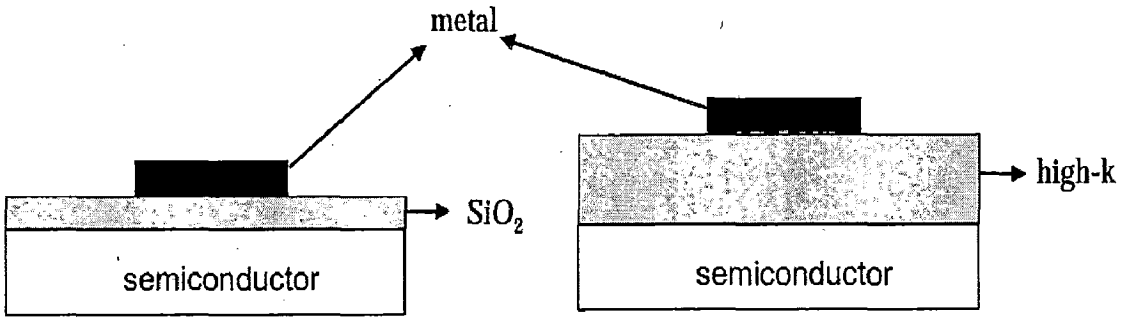

Figure 1.1 *Illustration of two MOS devices with SiO_2 (left) and with high-k material (right), which has the same EOT with the other one (not in scale).*

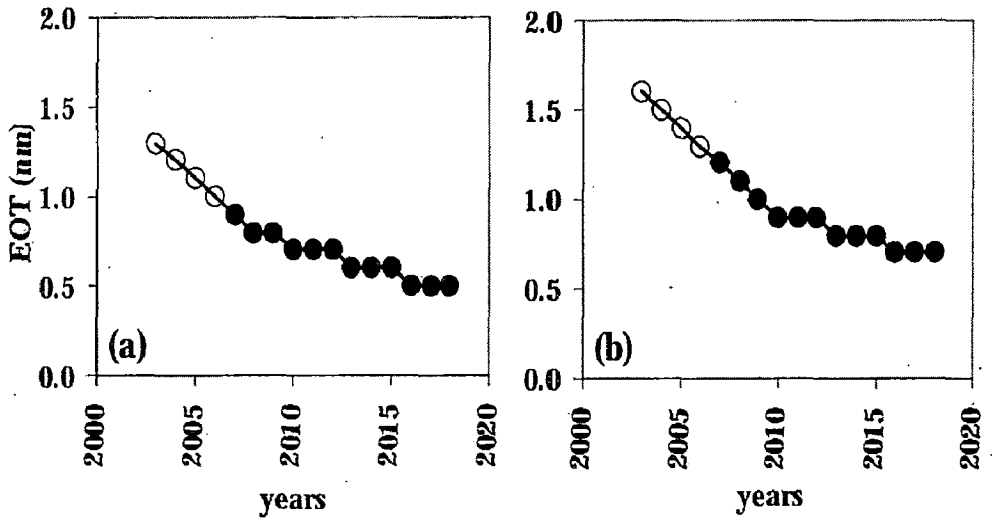

Figure 1.2 *ITRS projections for EOT of gate dielectrics, (a) for high performance and (b) low power applications. Full circles indicate where manufacturable solutions for EOT requirement are known up to 2004 [2].*

The need for high-k gate dielectrics is projected as one of biggest near ages in Industrial Technology Roadmap for Semiconductors (ITRS), and EOT requirements in ITRS are shown in Figure 1.2, for high performance and low power applications according to the 2004 update [2].

1.2 High-k Dielectric Materials

Integration of high-k gate dielectrics to silicon technology is a demanding task after the success of SiO_2 gate dielectrics, with two main advantages comparing to the other oxides: Large band gap (~ 9.1eV), which gives excellent leakage current properties and high quality interface with silicon, compared to the other oxides on silicon. The requirements for appropriate high-k dielectric materials have been described in details in literature [3, 9, and 16] can be summarized as follows:

1.2.1 Permittivity and barrier height

Table 1.1 Comparison of relevant properties for high-k materials [15,16].

Material	Dielectric Constant (k)	Band Gap E_G (eV)	ΔE_C to Si (eV)	Crystal Structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.1	Amorphous
Y_2O_3	15	5.6	2.3	Cubic
ZrO_2	25	5.7	1.5	Mono., tetrag., cubic
HfO_2	25	5.7	1.5	Mono., tertag., cubic
La_2O_3	30	4.3	2.3	Hexagonal, cubic
Ta_2O_5	26	4.5	0.5	orthorhombic
TiO_2	80	3.5	1.2	Tetrag.(rutile, anatase)

mono. - Monoclinic, tetrag.-tetragonal

As shown in the Table 1.1, band gap reduction in high-k materials is a limitation that must be realized and expected, while selecting a suitable high-k gate dielectric. In the cases of Ta_2O_5 and TiO_2, both materials have small E_G values and correspondingly small ΔE_C values. These small ΔE_C values directly correlate with high leakage currents for both materials, making pure Ta_2O_5 and TiO_2 are unlikely choices for gate dielectric applications. ZrO_2, HfO_2 and La_2O_3 offer relatively high values for both k and E_G.

1.2.2 Thermodynamic stability on Si

Most of the high-k metal oxide systems investigated so far have unstable interfaces with Si: i.e., they react with Si under equilibrium conditions to form an undesirable

interfacial layer. As many of the material candidates result in mixed interfacial alloys upon deposition or further processing, the use of materials such as silicates ($HfSiO_3$, $ZrSiO_3$) may allow for control of the Si interface composition, which may solve a key problem for the high-k gate dielectric materials approaches. The k values of materials such as $(HfO_2)_x(SiO_2)_{1-x}$ and $(ZrO_2)_x(SiO_2)_{1-x}$ are substantially lower than those of their pure metal oxide counterparts (ZrO_2, HfO_2), but this trade off for interfacial control and relatively higher mobility will be acceptable as long as the resulting leakage currents are low enough.

Because of the softness in the high-k material metal-oxygen (M-O) bonds compared to silicon-oxygen bonds (Si-O), scattering are strengthened which causes mobility degradation across channel region in high-k based MOSFETs [12]. Pure metal oxide systems such as HfO_2 and ZrO_2, suffers from high mobility degradation, where as materials incorporated with 'Si-O' such as silicates works far better. Thin interface layer with 'Si-O' improves the channel mobility, but maximum attainable mobility is lower than that of SiO_2 systems.

1.2.3 Interface quality

It is difficult to imagine any material creating a better interface to Si than that of SiO_2, since typical production quality SiO_2 gate dielectrics have a midgap interface state density D_{it} $\sim 2 \times 10^{10}$ states/cm^{2}eV. Most of the high-k materials have D_{it} $\sim 10^{11}$–10^{12} states/cm^{2}eV, and in addition exhibit a substantial flat band voltage shift $\Delta V_{FB} > 300$mV [3]. Metal oxides which contain elements with a high coordination (such as Ta and Ti) will have a high (> 3.5) N_{av} and form an over-constrained interface with Si with a related degradation in leakage current and electron channel mobility. Similarly, materials with low coordination (e.g. Ba, Ca) compared to that of Si lead to under-constrained systems in the corresponding metal oxides. Such systems (metal oxides, ternary alloys, etc.) that are either over- or under-constrained with respect to SiO_2, lead to the formation of a high density of electrical defects near the Silicon - dielectric interface, resulting in deprived electrical properties.

Metal oxides such as ZrO_2 and HfO_2 are well known to exhibit high oxygen diffusivities [3-5] and are therefore a serious concern in regard to the control of interfacial layer formation. Annealing treatments with excess oxygen present (e.g. from the ambient or from a sidewall oxide), will lead to rapid O_2 diffusion through the oxides, resulting in SiO_2 or SiO_2-containing interface layers. Although SiO_2 is an ideal interface with Si, an uncontrolled

amount of SiO_2 formation at the interface will severely compromise the capacitance gain from any high-k layers in the gate stack. Any silicide bonding (M-Si) which forms near the channel interface, will tend to produce unfavorable bonding conditions, leading to high leakage current and electron channel motilities.

1.2.4 Film morphology

Many of the alternate gate dielectrics exhibit either polycrystalline or single crystal structures. Poly-crystalline gate dielectrics could be problematic because grain boundaries may serve as high-leakage paths [3], and this may lead to the need for an amorphous interfacial layer to reduce leakage current. In addition, grain size and orientation changes throughout a poly-crystalline film can cause significant variations in k value, leading to irreproducible properties, especially if gate dimensions approach that of the dielectric grain size.

In literature it is reported that phosphorus penetration is noticed in case of polycrystalline ZrO_2 and HfO_2 [13, 9]. Recent work suggests that annealing incorporation of N_2 reduces the diffusivity in side high-k dielectric films [3, 11]. The phase transition from amorphous ZrO_2 and HfO_2 to polycrystalline is reported at 550°C and 450°C of annealing in N_2 [14].

1.2.5 Gate compatibility

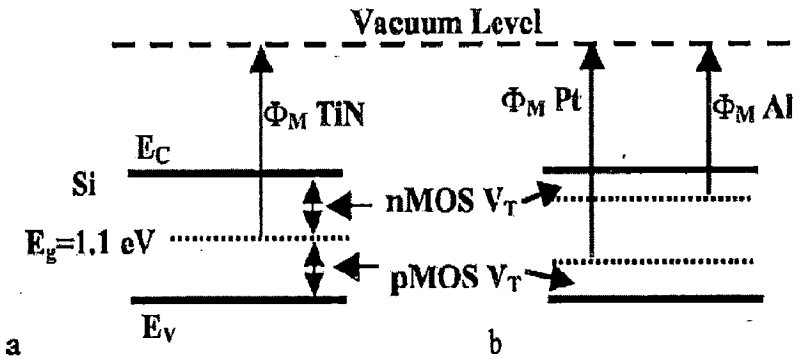

Figure 1.3 Energy diagrams of threshold voltages for NMOS and PMOS devices using (a) midgap metal gates and (b) dual metal gate [3].

Metal gates such as TiN and Pt have been used with most of the high-k gate dielectrics mentioned above for material evaluation purposes due to their expected stability toward adverse reactions with various dielectrics.

The two basic approaches are followed to achieve successful insertion of metal electrodes are: a single midgap metal or two separate metals. The energy diagrams associated with these two approaches are shown in Figure 1.3.

The midgap metal approach is to use a metal (such as TiN) that has a work function that places its fermi level at the midgap of the Si substrate. These are generally referred to as midgap metals. The main advantage of employing a midgap metal arises from a symmetrical V_T value for both NMOS and PMOS, because by definition the same energy difference exists between the metal fermi level and the conduction and valence bands of Si. This affords a simpler CMOS processing scheme, since only one mask and one metal would be required for the gate electrode (no ion implantation step would be required for the gate electrode).

However, a major drawback is that the band gap of Si is fixed at 1.1 eV, thus the threshold voltage for any midgap metal on Si will be ~0.5V for both NMOS and PMOS. Since voltage supplies are expected to be ~1.0V for sub-0.13μm CMOS technology, V_T ~0.5V is much too large, as it would be difficult to turn on the device. Typical threshold voltages for these devices are expected to be 0.2–0.3V [3].

The two separate metals approach towards metal electrodes involves two separate metals, one for PMOS and one for NMOS devices. As shown in Figure 1.3(b), two metals could be chosen by their work functions, Φ_M, such that their fermi levels line up favorably with the conduction and valence bands of Si, respectively. In the ideal case the Φ_M value of Al could achieve V_T ~0.2V for NMOS, while the higher Φ_M value of Pt could achieve V_T ~0.2V for PMOS.

In practice, Aluminium is not a feasible electrode metal because it will reduce nearly any oxide gate dielectric to form an Al_2O_3-containing interface layer. Other metals with relatively low work functions, such as Ta and TaN are feasible gate metals for NMOS. Similarly for PMOS, Pt is not a practical choice for the gate metal, since it is not easily processed, does not adhere well to most dielectrics, and is high cost. Other elemental metals with high Φ_M values such as Au are also not practical, for the same reasons as for Pt. It has been suggested that the work functions for each metal should be within 0.2 eV of the conduction and valance band edges of Si.

1.2.6 Process compatibility

A crucial factor in determining the final film quality and properties is the method by which the dielectrics are deposited in a fabrication process. The deposition process for the dielectric must be compatible with current or expected CMOS processing, cost and throughput. PVD methods have provided a convenient means to evaluate materials systems for alternate dielectric applications. The damage inherent in a sputter PVD process results in surface damage and thereby typically creates unwanted interfacial states. Additionally, device morphology inherent to the scaling process generally rules out such line-of-sight PVD deposition approaches. For this reason, CVD methods have proven to be quite successful in providing uniform coverage over complicated device topologies [5, 6].

The chemical reactions associated with CVD deposition require careful attention in order to control interfacial layer formation. The precursor used in the deposition process must also be modified to avoid unwanted impurities in the film as well as permit useful final compositions in the dielectric film. Indeed, a graded composition for dielectric films may be a key requirement in order to control interface state formation to a level comparable to SiO_2 [5, 6].

Atomic layer deposition (ALD) (or Atomic Layer Epitaxy (ALE)) offers certain excellent large area uniformity, excellent conformality, and atomic level control of film composition and thickness [5, 6]. It is a chemical gas phase thin film deposition method under self limiting growth. The film is grown through sequential saturative surface reactions that are realized by pulsing the two (or more) precursors into the reactor alternately, one at a time, separated by cleaning or evacuation steps. The major drawback of ALD is low deposition rate (100-300nm/hr). However for low thickness layers it holds good and by parallel processing with large wafer it will be economical.

Reactive Magnetron Sputtering is attractive for research on novel dielectrics because it is fast and one can easily investigate a wide range of different materials and compositions. For high-k materials it is necessary to control the thickness and roughness of the thin films down to an atomic scale [5, 6]. Such well-controlled growth can also be used to manufacture artificially layered structures of different materials with different properties.

1.4 Outline of the Dissertation

In this dissertation there are mainly four chapters: The device fabrication steps as cleaning of wafer, deposition of materials by evaporation and thin film deposition by RF magnetron sputtering, and characterization tools like crystal structure study using X-ray diffraction, thickness measurement using surface profilo meter and electrical characterization by capacitance-voltage measurements and leakage current measurement are discussed in chapter 2.

In chapter 3, effects of annealing on structural and electrical properties of Al/HfO_2/p-Si and Al/ZrO_2/p-Si structures are studied. Dielectric films of thickness 25nm to 35nm are deposited using sputtering. On top of the dielectric coating, aluminium circular dots of thickness 150-200nm are deposited by evaporation using shadow masks. Analysis using XRD and electrical measurements are performed for these capacitors after annealing at 100^0C, 250^0C, 350^0C and 450^0C. Electrical properties are measured at three different temperatures: room temperature and 80^0C and 100^oC. Based on the results proper deposition criterion for dielectric deposition is selected. By evaluating results it is identified that post deposition annealing increases the poly crystallenity and decreases the fixed oxide charges inside the capacitor.

Chapter 4 discusses the accelerated stress of fabricated Al/HfO_2/p-Si and Al/ZrO_2/p-Si MIS capacitors. These devices are stressed under constant current stress (CCS) of -1mA at room temperature and at 80^0C in accumulation region for 10000sec. Meanwhile I-V and C-V measurements are performed at different stress timings. Based on the results, degradization behavior of dielectric films is studied. From the leakage measurements possible dominant mechanism occurring inside the dielectric are investigated.

In chapter 5 using the studies discussed in chapter 3 and 4, Metal Insulator Semiconductor (MIS) Capacitors of laminate structures of HfO_2 and ZrO_2 are fabricated. From C-V measurements a dielectric constant of 20.5 is achieved with Al/HfO_2/ZrO_2/p-Si. Reliability analysis using time dependent constant current stress (CCS) of -1mA on metal gate at room temperature and 80^0C are studied using C-V and I-V measurements.

The details of wafer cleaning steps used in this work are described in step by step manner in Appendix A. Detailed experimental steps for deposition using Evaporation and Sputtering are illustrated in Appendix B and Appendix C. In Appendix D, the details of

electrical characterization details and analysis of measurements are explained including MATLAB program to extract the parameters from C-V characteristics of MOS capacitor.

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CHAPTER 2

FABRICATION AND CHARACTERIZATION TECHNIQUES

2.1 Introduction

The transition from silicon dioxide (SiO_2) and silicon oxynitrate to high-k dielectric material represents a fundamental change in technological processing towards deposited dielectrics and away from dielectrics that can be thermally grown on silicon [1-2]. To ensure the good electrical performance of the resulting devices, the deposited dielectrics must have an excellent thickness uniformity and superior interfacial and bulk properties. To maintain these requirements a careful selection and processing of materials and various characterization techniques are involved [1-4].

2.2 Device Fabrication

The structure of metal insulator semiconductor capacitor (MISC) using high-k material is shown in Figure 2.1. A thin layer of high dielectric material is deposited on polished surface of cleaned substrate using Radio Frequency Magnetron Sputtering. On top of dielectric, a layer of metal is deposited by Physical Vapor Deposition by means of evaporation process. A shadow mask having circular dots, each dot of radius 1mm is used to obtain a précised size. Prior to the deposition of dielectric, a stable ohmic contact is achieved between deposited metal on backside and silicon substrate. In this work aluminium (Al) metal is used to form an ohmic contact with p-type silicon. To form a stable ohmic contact after deposition of aluminium samples are annealed at 450^0C in nitrogen gas ambient of 10 bar of pressure for 15 minutes. [5]

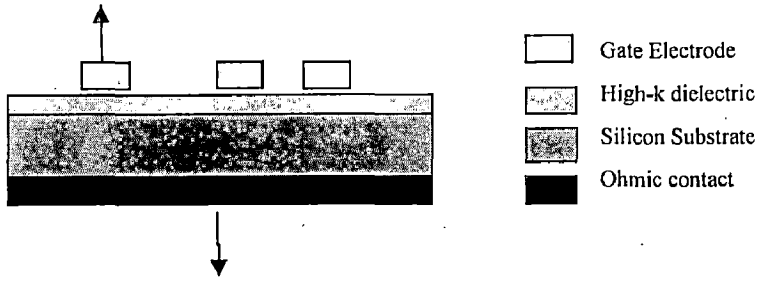


Figure 2.1 *Schematic diagram of metal insulator semiconductor capacitor structure.*

2.2.1 Substrate preparation

The first step of producing a MIS device with a high-k gate dielectric is the cleaning of silicon substrate. This step has been reported to be affecting the silicon-dielectric interface [6-7]. Three objects are usually required in cleaning.

One is the removal of organic species that can affect bond ability. Organic solvents are required to clean this. The second one is the removal of ionic species that can cause corrosion during the life of device or in an unusual instance, contribute to charge accumulation. Water is a good solvent for ionic species. Distilled water is used to clean the ionic impurities on substrates. Silicon wafers usually contains thin layer of native oxide layer on its surface. To remove it from chemical etching with diluted hydrofluoric acid (HF) is used.

The detailed cleaning procedure of substrates is given in Appendix A. Cleaned substrates are preserved in a vacuum sealed container to keep away from atmospheric conditions.

2.2.2 Thin film metal deposition by evaporation

The most common methods of Physical Vapor Deposition (PVD) for metals are evaporation, e-evaporation and sputtering [8-9]. Out of these vaporation is a simple apparatus and good to liftoff. Evaporation occurs when the material is heated more than its melting temperature in an evacuated chamber. The evaporated atoms travel with high speed velocities in straight line trajectories and get deposited on substrates placed in chamber.

The rate of evaporation is controlled by the vapor pressure as given in equation 2.1[9] and vapor pressure varies exponential with temperature ($P_e \sim e^T$) [9].

$$r_{evap} = \sqrt{\frac{M}{2\pi kT}} P_e \qquad (2.1)$$

r_{eveap} = evaporation rate M= atomic mass

k =Boltzmann's constant P_e=vapor pressure T= temperature

Deposition rate depends on location and orientation of wafer in the chamber. Deposition rate is governed by the following equation 2.2 [9].

$$r_{deposit} = \frac{r_{evap}}{\Omega d^2 \rho} cos\theta \quad (2.2)$$

$r_{deposit}$ = deposition rate (thickness/sec) Ω = solid angle over source emits (steradians)

r_{evap} = evaporation rate (mass/sec) d = distance form source to substrate

ρ = material density θ = Inclination of substrate away from substrate to source

To improve the uniformity the distance from the source to substrate is longer compared to substrate area of cross section. To increase the deposition rate, where substrates are placed at so far, we can increase the temperature. Too high rate of material deposition can results in condensation of the material into droplets. Droplets on wafer cause poor surface morphology.

From the equation 2.2 if $\theta = 90^0$ then deposition rate is zero. So good step coverage is not possible using evaporation. Due to having longer mean free paths (M α diameter of molecule^{-2}) the uniformity of deposition for ultra thin depositions is doubted. Since the filament must be the heating source, contamination from filament itself can be a concern at high temperatures.

The procedure that we follow for deposition of metal by evaporation is described in detail in Appendix B.

2.2.3 Deposition by sputtering technique

Among various PVD techniques, sputtering process exhibits several advantages: any material can be volatilized, compounds are volatilized stochiometrically and film deposition rates can be made uniform over large areas. Furthermore, the kinetic energy of sputtered atoms falls on the substrate strongly controls structure and physical properties [8-11]. In sputter deposition technique the thin film is deposited by sputtering, i.e. removal of atoms from a "target"(source), which then deposits onto a substrate. In other words, it is the ejection of atoms from the surface of material (the target) by bombardment with energetic particles, the process called 'sputtering'. Sputtering is largely driven by momentum exchange between the ions and atoms in the material, due to collisions. Although the first collision, ions pushes atoms deeper into the cluster, subsequent collisions between the atoms can result in some of the atoms near the surface being ejected away from the cluster of target atoms.

Sputtering process begins when inert gas atoms gets ionized due to the applied negative dc potential to the target material and these positive ions of inert gas hits the target atoms, the latter gains part of the momentum and transfer it to other atoms through further collisions, leading to a cascade which results in some of the target atoms to 'sputter' out of the target with secondary electrons. The sputtered atoms, those ejected into the gas phase, are not in their equilibrium state, therefore, they tend to condense back into the solid phase upon colliding with any surface in the sputtering chamber with maximum deposition taking place on the substrate, which is in the line of sight of the target to form a thin film. It subtends the maximum area perpendicular to the momentum of ejected target atoms and clusters. Along with the sputtered atoms secondary electrons also emits as shown in Figure 2.2. These secondary electrons collide and ionize the inert gas atoms and plasma is generated. The initial positive ions needed to trigger the generation of secondary electrons are thought to be either the stray ions always present in the atmosphere or the ions produced by field ionization of the inert gas atoms.

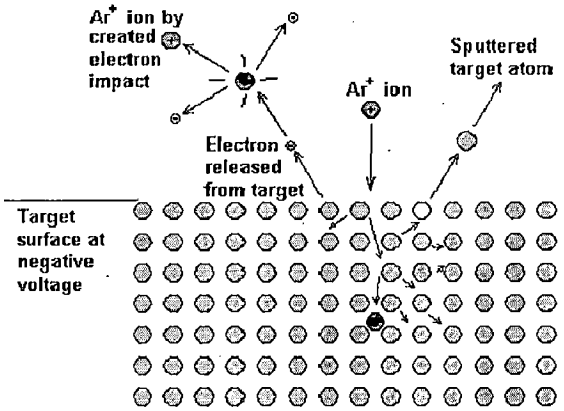


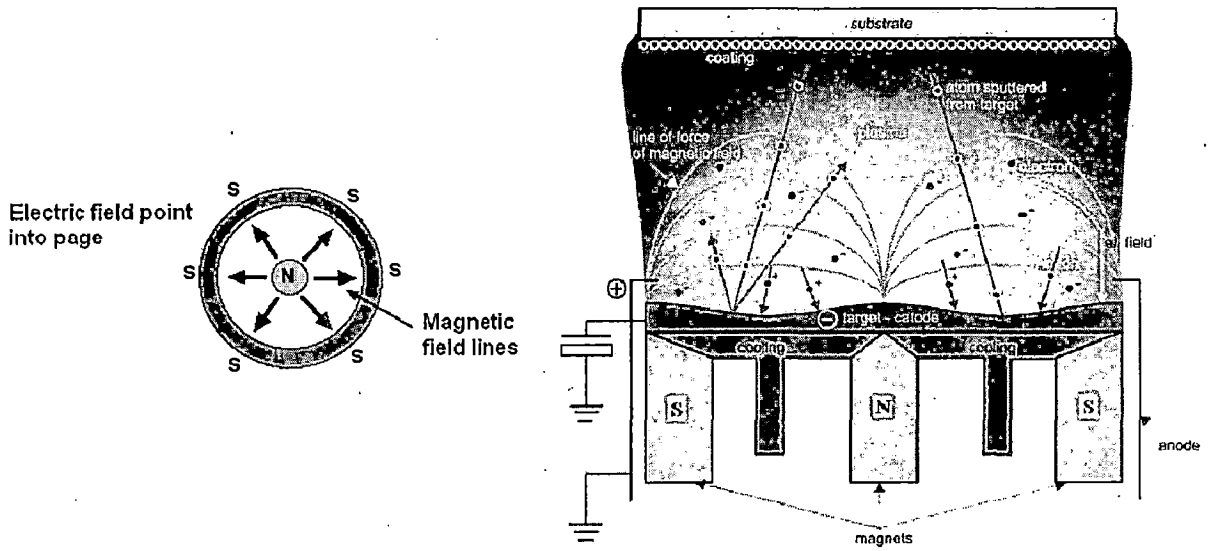
***Figure 2.2** Processes generated by the impact of highly energetic particle on a target [11].*

To use sputtering as a useful thin film deposition process, some criteria have to be met. First, ions of sufficient energy must be created and directed towards the surface of a target to eject atoms from the surface of the material. To achieve this, an argon gas of ionization energy 15.76 eV, for example, can be used in a chamber and by application of a sufficiently large voltage between the target and the substrate; a glow discharge is set up in a way to accelerate the positive ions towards the target to cause sputtering. Secondly, the ejected materials must be able to get to the substrate with little impedance to their movement. The pressure determines the mean free path of the sputtered particles which according to the Paschen's relation is proportional to 1/P (vapor pressure) [11].

In addition to pressure, the target-substrate distance determines the scattering of the sputtered particles on their way to the substrate and also the amount of energy with which they deposit on the substrate. Generally, the average energy of sputtered atom is 10-40 eV.

Magnetron sputtering is a thin film deposition technique based on the physical sputtering effects caused by the bombardment of a target material with accelerated ions produced in glow discharge plasma. In sputtering, not all of the electrons escaping the target contribute to the ionized plasma glow area. The wasted electrons fly around the chamber causing radiation and other problems, for example, the heating of the target. A magnetron sputtering source addresses the electron problem by placing a set of strong permanent magnets in the gun arranged in a circular geometry giving rise to a radial magnetic field parallel to the target surface as shown in Figure 2.3(a) and the process is given in 2.3 (b).

A plate of a highly permeable material (such as iron) located behind the magnets, prevents the magnetic field flux from spreading into regions other than in front of the target surface. Thus the electrons are forced to follow a closed drift path caused by the crossed electric and magnetic fields of magnetron sputtering process [11].



(a) (b)

***Figure 2.3** a) Electric and magnetic field lines in electron gun b) Magnetron sputtering process [11].*

Due to the confinement of secondary electrons, the larger number of sputtered atoms gets deposited as thin film on the substrate. DC magnetron sputtering is used for conducting targets such as metals or doped semiconductors but not for non-conducting targets (non

metals or insulators) because of its non-conducting nature, positive ions would lead to a charging of the surface and subsequently to a shielding of the electric field. Subsequently, the ion current would die off. Therefore, RF magnetron sputtering (radio frequency of 13.56 MHz) is used for non-conducting and semiconductor targets in which an AC voltage is applied to the target [11]. In one phase, ions are accelerated towards the target surface to sputter material. In the other phase, charge neutrality is achieved.

In reactive magnetron sputtering, the deposited film is formed by chemical reaction between the target material and gases like oxygen or nitrogen fed into the sputter chamber additionally to the argon, to produce oxide or nitride films and the reaction is usually occurs either on the substrate surface or on the target itself. The composition of the films can be controlled by varying the relative pressures of the inert and reactive gases. The sequence of steps that we follow while sputtering is described in detail in Appendix C.

The advantages of sputtering as deposition technique are as follows: The deposited films have high uniformity at large area, better reproducibility of deposited films, good adhesion of film with substrate, high flexibility of large-scale as well as complex geometry shape production, easy deposition of materials with high melting points and high reactivity. A homogeneous multicomponent phases as well as multilayer coatings can be produced with completely new material properties and the deposited films show the same concentration as that of the target material [11].

2.3 Characterization Techniques

2.3.1 Microstructure analysis using X-Ray Diffraction (XRD)

X-ray diffraction (XRD) is a versatile, non-destructive technique that reveals detailed information about the chemical composition and crystallographic structure of a crystalline material. It is most widely used for the identification of unknown crystalline materials and also information related to the crystal structure of the films, including lattice constants, crystallite size, phase analysis, crystal defects, stress, etc. The XRD methods are generally applied to films thicker than several angstroms on account of the strong penetrating power of the X-rays. X-rays are electromagnetic radiation of exactly the same nature as light, but of very much shorter wavelength. X-rays used in diffraction have wavelengths lying in the range of 0.5-2.5 Å where as visible light is of the order of 4000-7000 Å. X-ray diffraction is

based on constructive interference of monochromatic X-rays and a crystalline sample. When a monochromatic X-ray beam with wavelength λ is projected onto a crystalline material at an angle θ, X-rays are scattered by the electrons of the atoms without change in wavelength. As the wavelength of X-rays is close to atomic size (~ 1.5 Å), they get diffracted by atoms and ions. If, as in the case of crystals, the atoms or ions are arranged in a particular fashion, then the diffracted X-rays interfere constructively or destructively with each other depending on the path difference. W.L. Bragg formulated the condition for constructive interference as [12],

$$2dsin\theta = n\lambda \tag{2.3}$$

Where d is the spacing between two adjacent atomic planes θ is the angle between the atomic plane and the X-rays, *n* is the order of diffraction maximum and λ is the wavelength of the X-rays. The resulting diffraction pattern comprising both the positions and intensities of the diffraction effects is a fundamental physical property of the substance. Analysis of the positions of the diffraction effect leads immediately to a knowledge of the size, shape and orientation of the unit cell. The crystallite size is an important parameter, which can be determined from the width of the Bragg reflection and is given by the Scherer's formula [12]

$$t = \frac{0.9\lambda}{Bcos\theta} \tag{2.4}$$

Where t is the crystallite size, λ is the wavelength of the target material, *B* is the full width at half maximum (FWHM) of the Bragg reflection in the radians on the 2θ scale and θ is the Bragg reflection angle. It is important to subtract the instrumental line width from the observed line width to get a correct estimate of broadening due to small particle size. Therefore, by the Scherrer's formula, crystallite size is inversely proportional to full width at half maximum (FWHM), hence, small crystallites give rise to broad diffraction peak while large crystallites result in sharp peaks. X-ray diffractometer consist of three basic elements: an X-ray tube, a sample holder, and an X-ray detector as shown in Figure 2.6.[12] X-rays are generated in a cathode ray tube by heating a filament to produce electrons, accelerating the electrons toward a target by applying a voltage, and bombarding the target material with electrons.

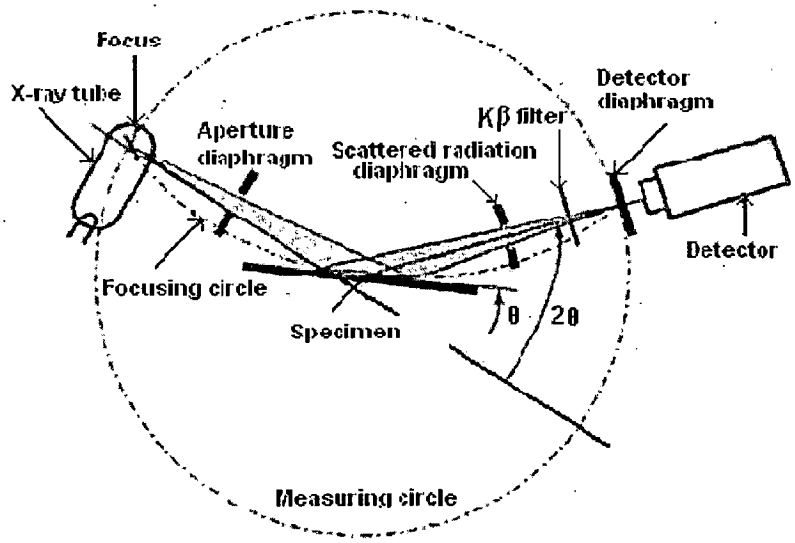
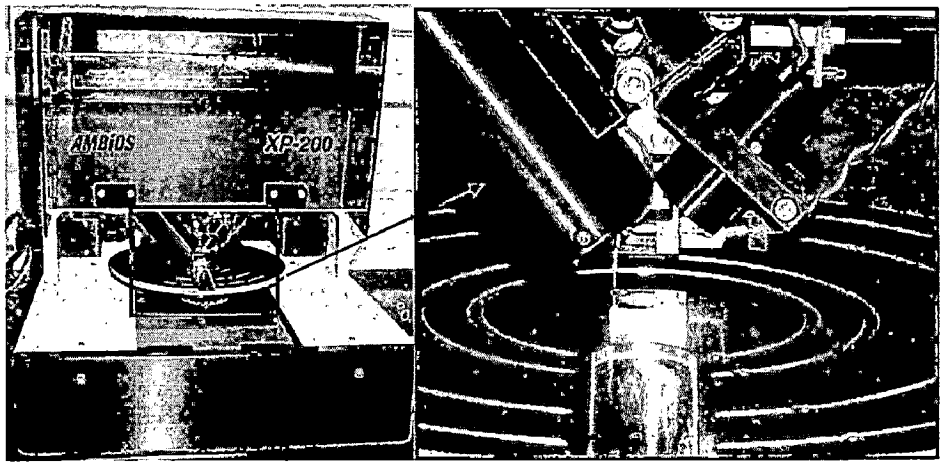


Figure 2.4 Schematic diagram of beam path in XRD [12].

2.3.2 Thickness measurement using surface profilo meter

A surface profilometer (also known as a stylus profilometer) is an instrument used for surface texture analysis as it measures the surface topography of a sample to reveal a topographical image of the surface. Surface profilometers are equipped with a sharp diamond-tipped stylus used to move vertically and laterally to scan across the surface of the sample. A Profilometer typically uses a mass cantilever system to keep the tip force constant while scanning stylus profilometers can measure vertical displacement as a function of position. These typical surface texture measuring systems can measure a vertical range from 5nm to 1mm. These contact profilometers can provide direct resolution as low as 1nm for surface metrology applications. Profilometers are typically used to measure surface roughness or film thickness.

To measure the thickness of a film, a surface step height of deposited material is maintained on the target surface. This can be done by providing clipping mask at an edge of substrate which covers the substrate and prevents coating. The stylus is moved across the step interface resulting in a step increase in scanning profile height. Figure 2.10 (a) shows the surface profilo meter used in this work. Figure 2.10(b) shows closer view of measurement system.



(a) (b)

Figure *2.5 (a) Surface profilo meter used in our lab*
(b) Closer view of diamond tip and scanning camera

2.3.3 Electrical characterization using C-V and I-V measurements

In general terms, electrical characterization of dielectric films includes primarily MOS capacitance-voltage (C-V) and dc conduction (I-V) measurements. Due to large leakage currents drawn through ultra thin gates, measurement and analysis have become more complex. Extraction of valid parameters forms measurement redundant to additional elements including series resistors, wafer probe station and parasitic capacitances. Once a valid representation of valid C-V and I-V data are obtained, extraction of primary parameters including Equivalent oxide thickness (EOT), silicon surface doping density and flatband voltage requires a complex analysis that previously including quantum confinement effects and poly depletion effects that must be deduced because their magnitude no longer be neglected.

The detailed procedure that we followed for Leakage current measurements, C-V measurements and extraction of parameters from C-V curves is described in detail at Appendix D.

a) Capacitance–voltage (C-V) measurements

In a C-V measurement there are three major steps: first, a reference sinusoidal signal is generated and applied to the device under test (DUT) and a reference resistor. The difference, or error voltage, is sent through phase detectors that separate it into in-phase and 90^0 out-of-phase components. These are applied to a modulator, amplified, and fed back to the reference resistor until a null is achieved. A vector ratio detector then measures the voltages across the DUT and the known reference resistor, generating outputs that can be displayed in a number of formats. The available choice of these pairs of output parameters

can vary widely with the instrument used, but may include $|Z|-\Theta$, $|Y|-\Theta$, C_s-R_s, C_s-D, C_p-G_p, C_p-D. All of these parameters are interdependent.

On-wafer C-V measurements are usually made on prober (probe station). Signals to multipad test structures are connected between the C-V analyzer and the prober through a switch matrix and interconnecting cables. The cables and switch matrix add stray capacitance to the measurements. However the latest instruments (like Wenkerr-4300) comes up with offset zero cancelation by open circuit trimming and short circuit trimming. Prior to measurements offset cancelation must be done to remove parasitic effects due to measurement setup. After performing offset cancelation, for each subsequent measurement offset capacitance value deducted automatically.

The most important, but often neglected, C-V measurement requirement is to record data only under equilibrium conditions. A MOS-C takes time to become fully charged after a voltage step is applied. The fully charged condition is generally referred to as the equilibrium condition. Therefore, to allow the MOS-C to reach equilibrium, as shown in Figure 2.8 [13] 1) after initially applying voltage to a MOS-C, allow an adequate hold time before recording the capacitance, and 2) after each step of the MOS-C voltage, allow an adequate delay time before recording the capacitance. C-V curves swept from different directions may look different. Allowing adequate hold and delay times minimizes such differences.

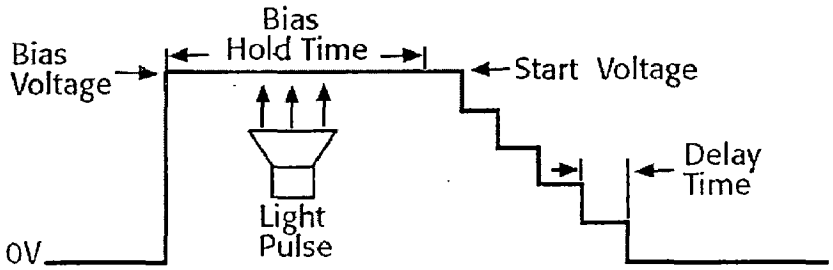


***Figure 2.6** Preferred C-V measurement sequence [13].*

After generation of successful measurement data extraction of parameters with accuracy is quite challenging. Extraction of MOS device parameters from C-V measurement is described in appendix D.

b) Leakage current mechanisms

Table 2.2 Basic conduction processes in insulators [14].

Conduction mechanism	Parameter dependencies
Ohmic	$J \sim \frac{V}{d} \exp\left(^{-\Delta H_{ae}}/_{kT}\right)$
Ionic	$J \sim \frac{V}{dT} \exp\left(^{-\Delta H_{ai}}/_{kT}\right)$
Space charge limited	$J \sim \frac{8\varepsilon_i \mu V^2}{9d^3}$
Schottky emission	$J \sim A \times T^2 \exp\left(\frac{-q(\emptyset_B - \sqrt{\frac{qV}{4\pi\varepsilon_i d}}}{kT}\right)$
Pool-Frenkel emission	$J \sim \frac{V}{d} \exp\left(\frac{-q(\emptyset_B - \sqrt{\frac{qV}{4\pi\varepsilon_i d}}}{kT}\right)$
Tunnel or field emission	$J \sim \left(\frac{V}{d}\right)^2 \exp\left(\frac{-4\sqrt{2m^*}(q\emptyset_B)^{3/2}}{3q\hbar\, {}^{V}/_{d}}\right)$

A = effective Richardson constant, φ_B = barrier height,

V = applied voltage, d = equivalent oxide thickness,

m^* = effective mass, ΔH_{ae} = activation energy of electrons,

ΔH_{ai} = activation energy of ions, k = Boltzmann constant,

ε_i = insulator dynamic permittivity , T = absolute temperature.

Table 2.2 shows the different types of dc conduction mechanisms that are studied in materials in earlier. Out of them all Schottky, Pool-Frenkel and tunneling mechanisms are studied in case of gate dielectric of MIS capacitor. In case of high-k dielectric materials leakage conduction due to Schottky, Pool-Frenkel and tunneling is studied in literature [3, 5, and 7].

Schottky emission is the injection of carriers into a film over the interfacial barrier between the contact and insulator lowered by the image force of injected carrier. For this interface limited mechanism to be dominant, transport of the injected carriers across the bulk

of the film towards opposing electrode must proceed rapidly and the bulk material should not limit the transport of carriers.

In case of Pool-Frenkel emission the injected carriers across the bulk of the film begin to accumulate in the film, bringing about a bulk-limited mechanism. The injected charge carriers are trapped/detrapped by charge carriers present in side bulk material. Interesting thing is Schottky and Pool-Frenkel mechanisms, one is interface limited and the other is bulk limited, they have similar I-V relationships, as can be seen in above Table 2.2 [14].

Compared to tunneling processes, Schottky and Pool-Frenkel are thermally aided phenomena. In the case of FN tunneling, electrons tunnel through a triangular potential barrier, whereas in the case of direct tunneling, electrons tunnel through a trapezoidal potential barrier. The tunneling probability of an electron depends on the thickness of the barrier, the barrier height, and the structure of the barrier [15]. Therefore, the tunneling probabilities of a single electron in FN tunneling and direct tunneling are different, resulting in different tunneling currents.

In case of direct tunneling, there are three major mechanisms in MOS devices, namely, electron tunneling from conduction band (ECB), electron tunneling from valence band (EVB), and hole tunneling from valance band (HVB) [15]. Figure 2.10 shows the band diagram of high-k dielectric MIS structure with interfacing layer. In that figure the four possible leakage mechanisms are mentioned [14].

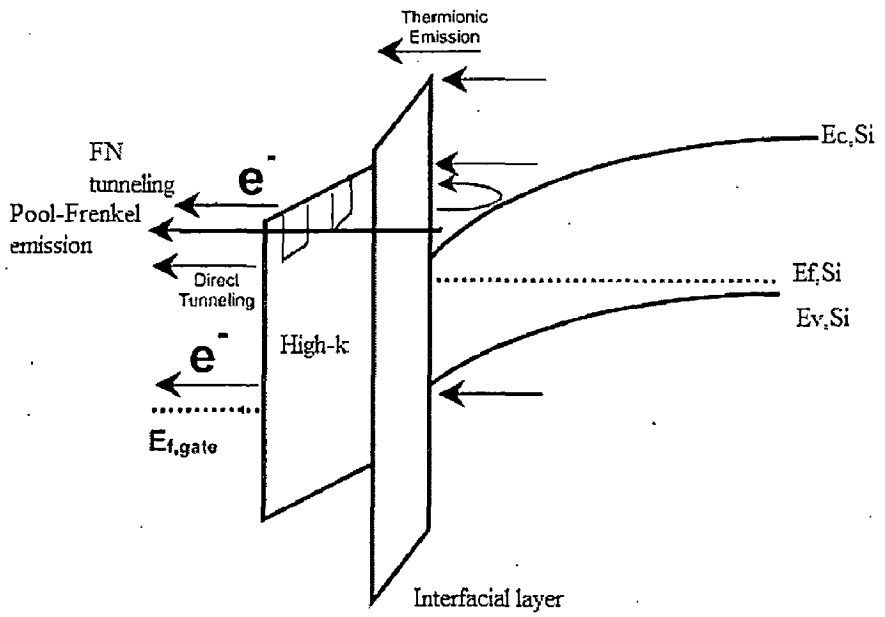


Figure 2.7 Major leakage phenomena occurred in high-k dielectrics [14].

2.4 Conclusion

Fabrication and characterization techniques for high-k dielectric metal insulator capacitor are illustrated in this chapter. Detailed working procedure and physical operations are described for both evaporation and sputtering processes. Physical characterization techniques using X-Ray Diffraction is explained. Application of stylus profilometry for measurement of thickness is mentioned. Electrical characterization issues for measurements of Capacitance and Current with voltage are described. Different types of leakage mechanisms for high-k dielectric material are discussed.

Using techniques that we discussed in this chapter can proceed for the fabrication of Al/HfO_2/p-Si and Al/ZrO_2/p-Si structures and characterization of them for different annealing conditions and reliability observations for constant current stress.

2.5 References

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CHAPTER 3

STUDY OF ANNELAING ON Al/HfO_2/p-Si AND Al/ZrO_2/p-Si MIS CAPACITORS

3.1 Introduction

With the development of CMOS technology, the traditional SiO_2 seems to have reached its limits. HfO_2 [1-3,7] and ZrO_2 [4-7] are the most promising materials to replace SiO_2, for their reasonable dielectric constant (k), the relatively large band gap and thermal stability on Si substrate. However it is too difficult to achieve superior interface as SiO_2 with silicon substrate with these dielectrics. The formation of low-k interface as silicate or SiO_2 interfacial layer is noticed in literature [2-4]. To fabricate nanoscale superior gate insulators, it is necessary to find out the change in electrical properties after annealing treatment. The effect of incorporating N_2 into high-k film at high temperature Rapid Thermal Annealing (RTA) has been studied extensively by different researches [3-5]. It is reported that nitrogen acts as crystallization inhibitor and cause an increase in the crystallization temperature of hafnium and zirconium based dielectric.

However annealing results increase in low–k interfacial layer [2, 4] and ultimately reduces the effective oxide thickness. Increase in annealing temperature results in poly crystallization of amorphous films, which causes formation of grain boundaries which increases the leakage currents inside the dielectric layer. Amorphous films of HfO_2 and ZrO_2 materials are reported with high diffusion rates for O_2 [7] at high temperature annealing process, which predominately increases the formation of SiO_2 layer at interface.

In literature, RF Magnetron Sputtering deposition of HfO_2 and ZrO_2 layers on silicon (100) substrates has been reported [1-6]. As described in Chapter 2.2 deposition of HfO_2 and ZrO_2 oxides followed by Post deposition annealing in N_2 ambient is performed for investigating the possible improvements in layer's properties, in particular decrease in oxide trap charges. With the aim of studying effect of annealing temperature on high-k dielectrics, the Al/ZrO_2/p-Si and Al/HfO_2/p-Si layers, with a thickness range of 25 to 35nm are fabricated using sputtering. Their structural characterization is performed by X-Ray

diffraction (XRD) analyses and electrical properties are characterized by capacitance - voltage (C-V), current-voltage (I-V) measurements at temperatures 15^0C, 80^0C and 100^0C. The results showed that the density of fixed charge and leakage current density of dielectric film were decreased after RTA process in N_2 atmosphere.

3.2 Experimental Details

3.2.1 Substrate preparation

In this work boron doped and polished p-type Silicon (100) wafers of resistivity 2-10 Ωcm are used. Substrates were cleaved to a size of approximately 1 cm x 1 cm by diamond cutter. Substrates are cleaned by the procedure described in appendix A. Prior to the deposition of dielectric material a thin layer (150-200 nm) of Aluminium is deposited on the other side (unpolished surface) using Thermal Evaporation System. To form a strong ohmic contact, substrates are annealed at 450^0C in N_2 ambient at pressure 100mbar for 15 minutes [8]. All substrates were mounted onto a plate with silver paint and loaded into the sputtering system. A portion of each substrate surface was covered in silver paint for thickness measurement after growth.

3.2.2 Film growth

Table 3.1 Recipe used for deposition of HfO_2 and ZrO_2 thin films on p-Si substrates.

Parameters	HfO_2 sputtering (S1)	HfO_2 sputtering (S2)	ZrO_2 sputtering (S3)	HfO_2 sputtering (S4)
Target	2 inch 99.9% Hafnium	2 inch 99.9% Hafnium	2 inch 99.9% Zirconium	2 inch 99.9% Zirconium
Base Pressure (Torr)	2×10^{-6}	2×10^{-6}	2×10^{-6}	2×10^{-6}
Sputtering pressure(mTorr)	10	10	10	10
Ar gas flow (sccm)	20	20	20	20
O_2 gas flow(sccm)	**10**	**20**	**10**	**20**
Substrate temperature	200^0C	200^0C	200^0C	200^0C
Sputtering Power	RF power 50W	RF power 50W	RF power 50W	RF power 50W
Target Distance (cm)	5	5	5	5
Sputtering Time (min)	2	2	2	2
Insitu annealing	15 min at 100^0C in N_2	15 min at 100^0C in N_2	15 min at 100^0C in N_2	15 min at 100^0C in N_2
Expected thickness (nm)	40-50	40-50	40-50	40-50

HfO_2 and ZrO_2 films are grown by reactive RF magnetron sputtering. Total 8 samples of 4 types S1, S2, S3 and S4, i.e. there are two samples of each type. Oxygen gas flow rate is taken as 10 sccm for sample S1, S3 and 20sccm for sample S2, S4. Prior to deposition target material is presputtered in argon ambient for 5 minutes. Thin films of HfO_2 and ZrO_2 are deposited for 2 minutes. There was a total of four combinations of eight samples, i.e. there are two samples of each type, are prepared, the detailed procedure followed is described in appendix C. After completing the deposition of high-k material, samples are undergone to insitu annealing at 100^0C in O_2 ambient. The recipe used for deposition of dielectric is shown in Table 3.1.

3.2.3 Measurements

The thickness of the sputtered dielectric films is measured by stylus profilometry (surface profilometry) using the Filmetrics F20 thin-film measurement system. Table 2.2 shows the thickness measured for each sample.

***Table 3.2** Calculated thicknesses from surface profilo meter for sputtered layers.*

Sample name	Thickness of dielectric layer
S1	~26nm
S2	~31nm
S3	~24nm
S4	~32nm

Out of 2 samples prepared of each type, one sample is used to investigate the structural properties, which are observed by thin film XRD. Remaining samples are prepared for electrical properties measurement. Aluminium electrodes of each area $\pi\times10^{-2}$ cm^2 are fabricated as the top electrode using a shadow mask with a 200micron diameter circle pattern by thermal evaporation. The thickness of these electrodes was approximately 150-200 nm.

The current-voltage properties and capacitance-voltage properties of all samples are measured on silicon at 3 different temperatures: 15°C, 80^0C and 100°C. The capacitance-voltage curve is obtained at 100 kHz using Wenkerr 4300 LCR meter. The voltage is swept from depletion to accumulation and then back to depletion at sweep rate of 1.0 V/s. The detailed procedure for C-V and I-V measurement are described in appendix D. Fabricated

capacitor are rapid thermal annealed in nitrogen ambient at 100 mbar pressure for 15 minutes at 250^{0}C, 350^0 C and 450^{0}C.

3.3 Results and Discussion

3.3.1 Microstructure

X-Ray Diffraction (XRD) is used to investigate the formation of polycrystalline grains as a function of annealing temperature at 100^{0}C, 250^{0}C, 350^{0}C and 450^{0}C. The XRD results of HfO_2 and ZrO_2 coated films shown in Figure 3.1(a) and (b). They point out the amorphous nature of thin films for samples that are annealed at low temperatures. Crystallenity is evident in case of HfO_2 films after annealing at 450^{0}C. A peak appears at 2θ = 28.3° is perceived for HfO_2 thin films. It reveals the nature of polycrystalline monoclinic substance with lattice constants a=5.284^{0}A, b=5.182^{0}A and c=5.116^{0}A and a preferred orientation in (-1, 1, 1). ZrO_2 thin films are reported to be amorphous by annealing up to 450°C. No significant peak related to poly crystalline nature is pointed in case of ZrO_2.

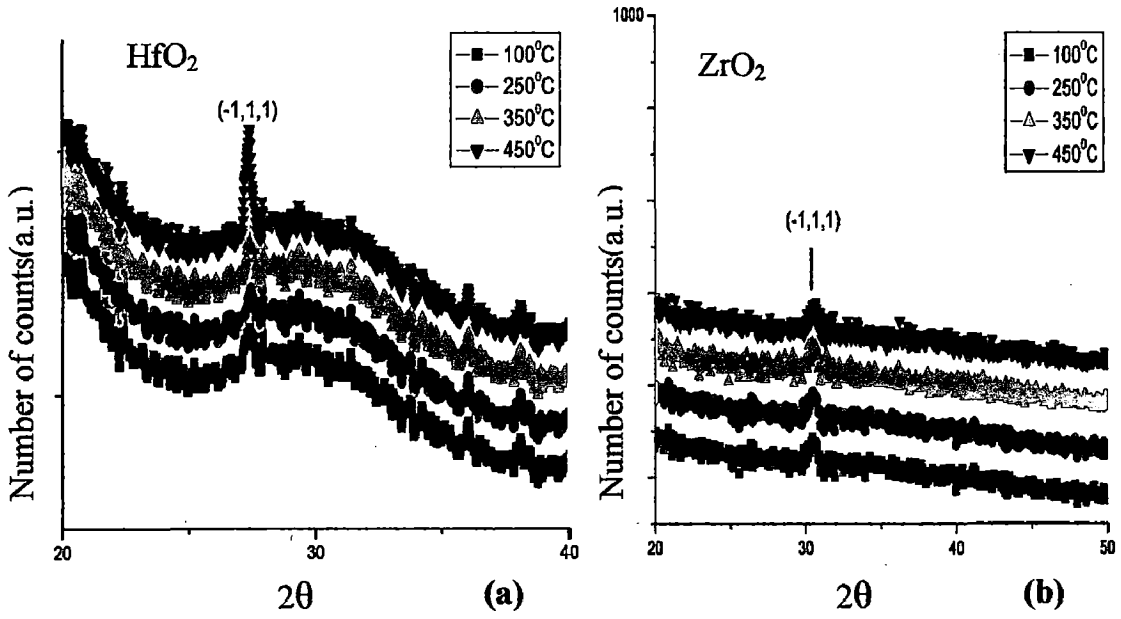


Figure 3.1 XRD spectra of (a) HfO_2 (b) ZrO_2 films for different annealing temperatures

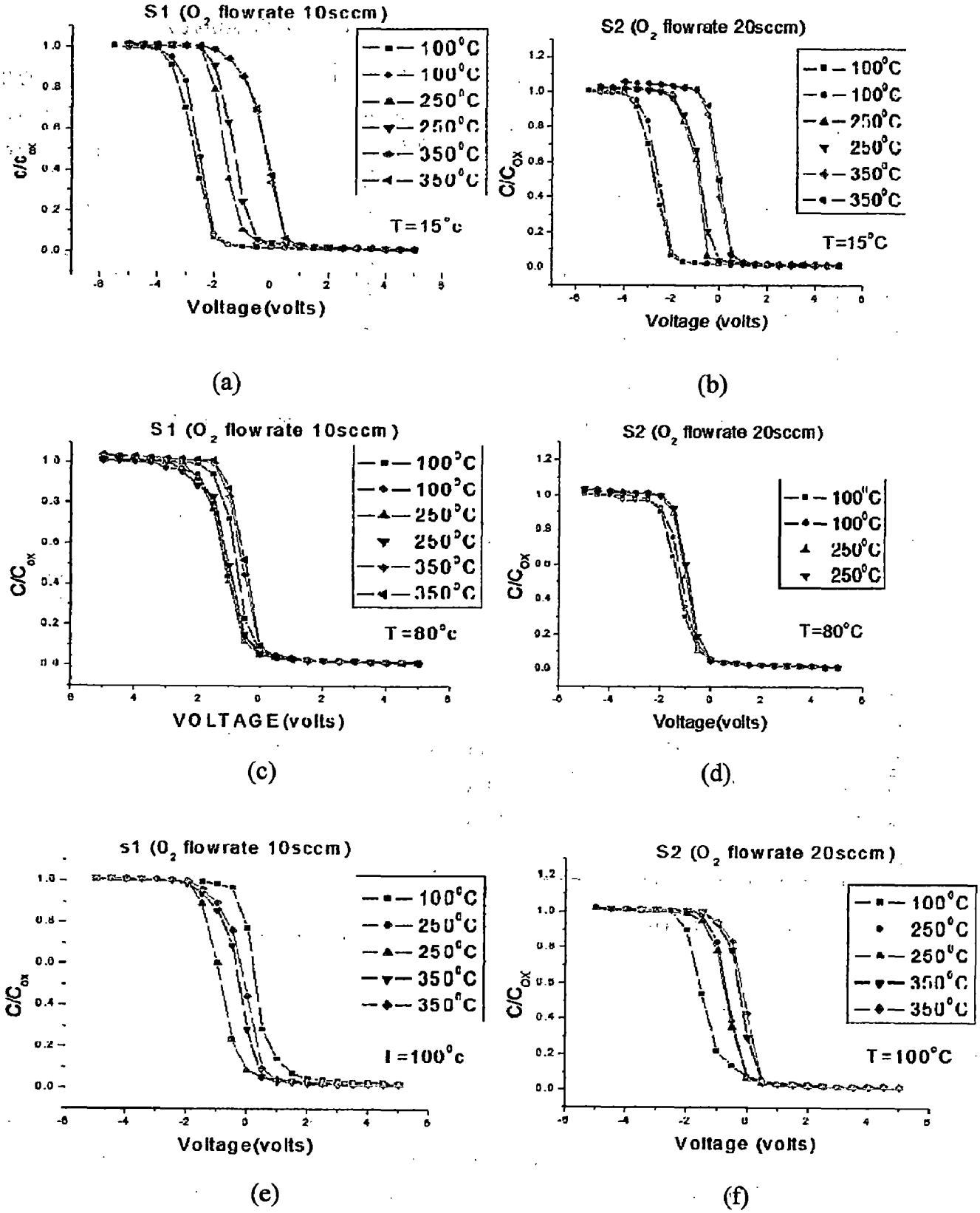


Figure 3.2 100 kHz C-V curves corresponding to annealed Al/ HfO_2/p-Si MIS devices, sample S1measurement at (a) 15^{0}C (c) 80^{0}C (e) 100^{0}C and for sample S2 measurement at (b) 15^{0}C (d) 80^{0}C (e) 100^{0}C.

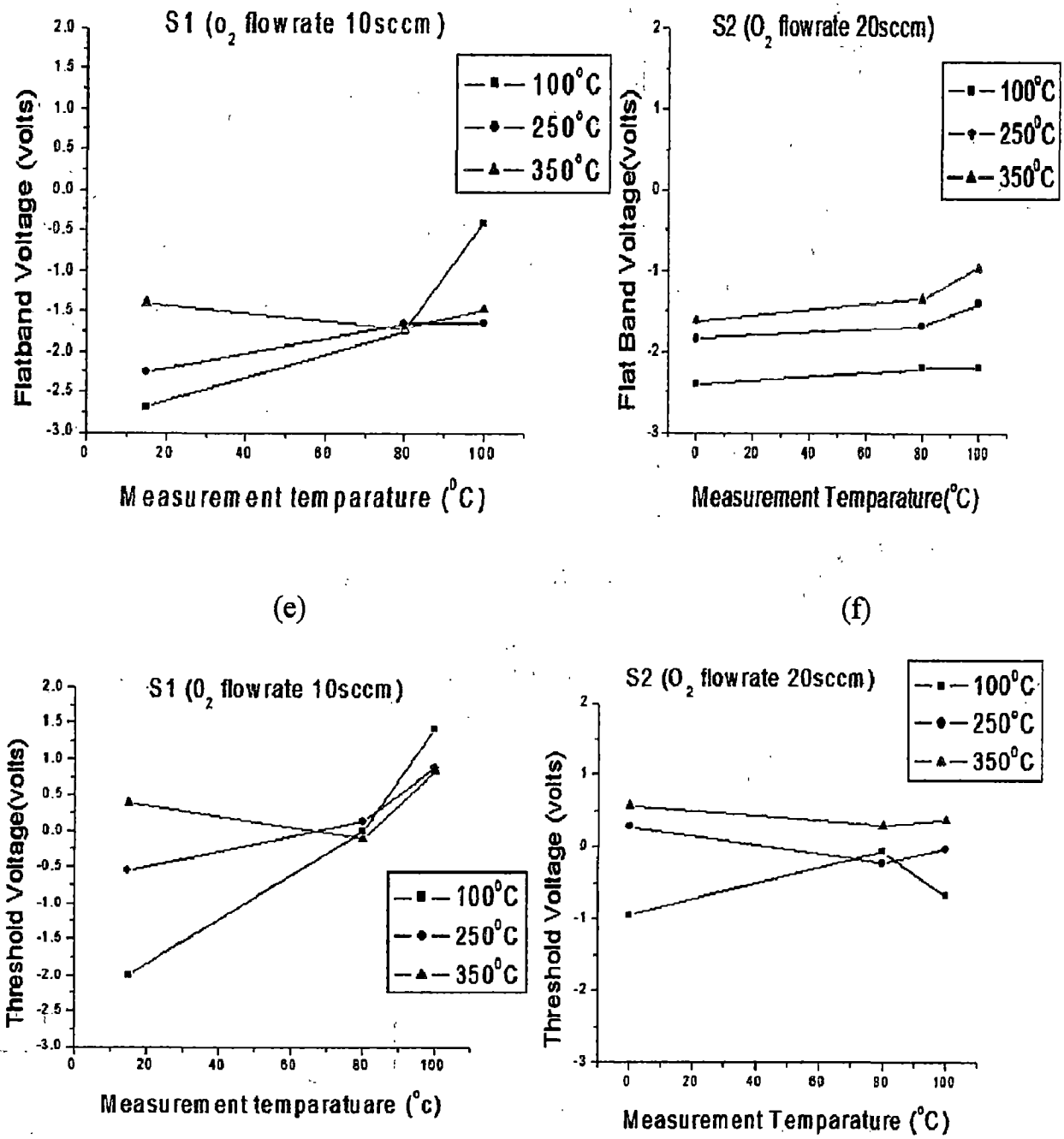


***Figure 3.3** Plots of variation of parameters with measurement temperature for Al/ HfO_2/p-Si MIS capacitors at different annealing temperatures for sample S1: (a) Fixed oxide charge density (cm^{-2}), (c) Equivalent oxide thickness(cm), (e) flat band voltage (volts) and (g) threshold voltage (volts) and for sample S2: b) Fixed oxide charge density (C/cm^2), (d) Equivalent oxide thickness(cm), (f) flat band voltage (volts) and (h threshold voltage (volts).*

3.3.2 Capacitance-Voltage measurements

(A) Al/HfO_2/p-Si MIS capacitors

High frequency (100 kHz) Capacitance-Voltage measurements are performed for both samples S1 (O_2 flow rate is 10sccm) and S2 (O_2 flow rate is 20sccm) of Al/HfO_2/p-Si at three different temperatures 15^0C, 80^0C and 100^0C.

Figure 3.2 shows the high-frequency (100 kHz) C-V curves for samples S1 and S2, of Al/HfO_2/P-Si MIS Capacitor measured using double voltage sweep technique,. i.e. from inversion to accumulation and back to inversion. The Nature of hysteresis (clockwise) is attributed to the trapped charges present in the insulating film. Such trapping occurs in the HfO_2 if unsaturated bonds and/or vacancies are present.

Figure 3.2 (a), (b) shows the deviation in capacitance with voltage for sample S1 and S2 of Al/HfO_2/p-Si MIS structure at different annealing temperatures measured at room temperature. Samples annealed at 100^0C show signs of large number of positive fixed oxide charges. Annealing incorporation with N_2 affects the crystallenity of dielectric and stable interfacial layer leads to reduction of effective trap charges. The hysteresis width also reduces with the effect of annealing indicating decrease in trapping/detrapping of charge carriers at room temperature. However sample S2 fabricated with higher oxygen flow rate contains less number of fixed oxide charge carriers and small hysteresis indicating stable interface formation between dielectric and silicon substrate.

Figure 3.2 (c) , (d) shows high frequency (100 kHz) C-V curves for sample S1 and S2 measured at 80^0C, indicates stable C-V curves with annealing pointing small number of fixed oxide charges inside HfO_2. Spreading in C-V curves at low annealing temperature shows signs of interface trap charges inside dielectric.

In figure 3.3 (e), (f) unannealed samples exhibit dispersion and it is reduced with increase in annealing, indicating reduction in number of inactive interface states at Silicon and HfO_2 interface. Unannealed samples exhibit large number of interface trap charges pointed by large hysteresis and spreading in C-V curves.

Figure 3.3 (a), (b) shows the variation of fixed oxide charge with measurement temperature for different annealing conditions in N_2 ambient. They show decrease in

effective fixed oxide charge density with measurement temperature of charge carrier witch predominately reducing trapping/detrapping efficiency. Annealing at 250^0C and 350^0C results decrease in fixed charge density.

Figure 3.3. (c), (d) shows the variation of Equivalent oxide thickness with measurement temperature. Al/HfO_2/P-Si MIS capacitors of sample S1 exhibits an average EOT of 6±1.5 nm and sample S2 exhibits an average EOT of 6.5±1 nm. With increase in annealing results diffusion of O_2 across HfO_2 incorporates the increase of low-k interfacial layer with increase in annealing temperature observed after annealing at 250^0C. Along with that HfO_2 dielectric layer get densified with annealing in N_2 resulting increase in dielectric constant, because crystalline materials exhibits more dielectric constant compared to amorphous materials, causes decrease in EOT observed after annealing at 350^0C.

Figure 3.3 (e), (f) shows the variation of flatband voltage with respect to measurement temperature. Increase in flatband voltage is noticed with decrease in fixed oxide charges in side dielectric. Same effect is observed in case of 3.3(g) and (h) shows the variation of threshold voltage with annealing temperature. Samples which are annealed at 350^0C indicate stable threshold voltage.

Al/HfO_2/p-Si MIS capacitors deposited with higher O_2 flow rate shows better results in capacitance–voltage Measurement with lesser fixed oxide charges and low interface states.(Sample2 has better results compared to sample1). Sample S1 exhibits large number of traps and dangling bonds which can be recovered by high temperature annealing. Increase in O_2 flow rate during sputtering shows increase in interfacial layer between dielectric layer and Silicon with annealing.

(B) Al/ZrO_2/p-Si MIS capacitors

Figure 3.4 shows High frequency (100 kHz) Capacitance-Voltage curves for Al/ZrO_2/ p-Si MIS capacitors for sample S3 (fabricated with O_2 flow rate10sccm) and S4 (fabricated with higher O_2 flow rate 20 sccm) at different measurement temperatures 15^0C, 80^0C and 100^0C. Results have taken for samples after annealing at 100^0C, 250^0C and 350^0C temperatures.

Figure 3.4 (a), (b) shows the variation of capacitance with voltage for sample S3 and S4 of Al/ZrO_2/p-Si MIS structure prepared at different annealing temperatures measured at

room temperature. Annealing of samples at low temperature (100^0C) exhibits large number of positive fixed oxide charges and hysteresis. Annealing in N_2 environment boasts poly crystalline nature of dielectric. The hysteresis width also reduces with the annealing temperature indicating diminution of trapping/detrapping of charge carriers at room temperature. However sample S4 is fabricated with higher oxygen flow rate results in less number of fixed oxide charge carriers and less hysteresis indicating less mobile charge carriers. But the C_{ox} value in case of sample S4 is lesser compared to that in case of sample S3. It signifies lower dielectric constant in case of capacitors that are deposited at high temperature.

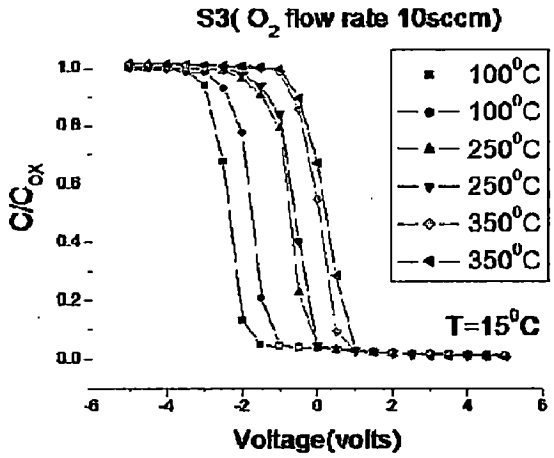
Figure 3.4 (c) and (d) shows high frequency (100 kHz) C-V curves for sample S3 and S4 measured at 80^0C, indicates stable C-V curves with annealing indicating good interface characteristics. At high temperature fixed oxide charges in oxide are thermally ionized exhibits less trapping probability of charges. The fixed charges present near the interface are more effective in trapping and detrapping of charges near to dielectric semiconductor interface. This is recovered by effect of annealing.

In Figure 3.4(e) and (f) unannealed samples exhibit dispersion and it is reduced with increase in annealing temperature pointed by diminishing of inactive interface states at Si and dielectric interface.

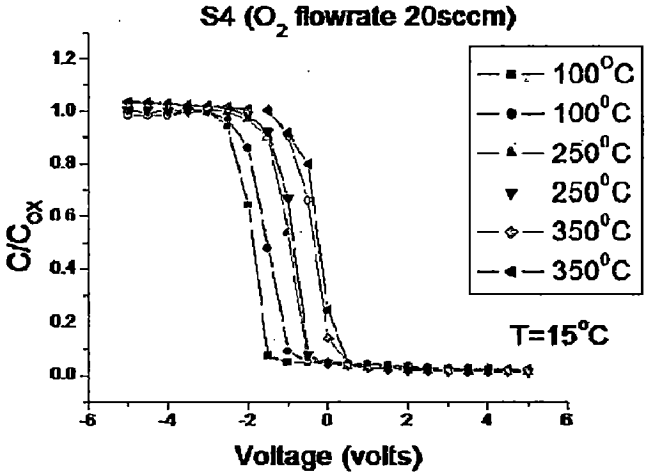
Figure 3.5(a) and (b) shows the variation of fixed oxide charge with measurement temperature for different annealing conditions of Al/ZrO_2/p-Si in N_2 ambient. Decrease in effective fixed oxide charge with measurement temperature is shown in their results. But the effect of unsatisfied and inactive interface states is more. Increase in annealing temperature results in decrease in fixed charge density and interface traps.

Figure 3.5. (c) and (d) shows the variation of Equivalent Oxide Thickness (EOT) with measurement temperature. Al/ZrO_2/p-Si MIS capacitors of sample S3 exhibits an average EOT of 8±1.5 nm and sample S2 exhibits an average EOT of 8.5±1 nm. Increase in annealing results in diffusion of O_2 across ZrO_2 which incorporates the low-k interfacial layer. Increase in annealing temperature results in degradation of dielectric constant and increase in EOT. Along with that ZrO_2 dielectric layer get densified with annealing in N_2 which results in increase in dielectric constant of dielectric layer and decrease in EOT. Its crystallization temperature is higher compared to HfO_2 dielectric results in small dielectric

constant value. Figure 3.3 (e), (f) shows the dissimilarity of flatband voltage with respect to measurement temperature. Increase in flatband voltage was noticed with decrease in fixed oxide charges in side dielectric due to annealing. Same effect is observed in case of 3.3(g) and, (h).



(a)



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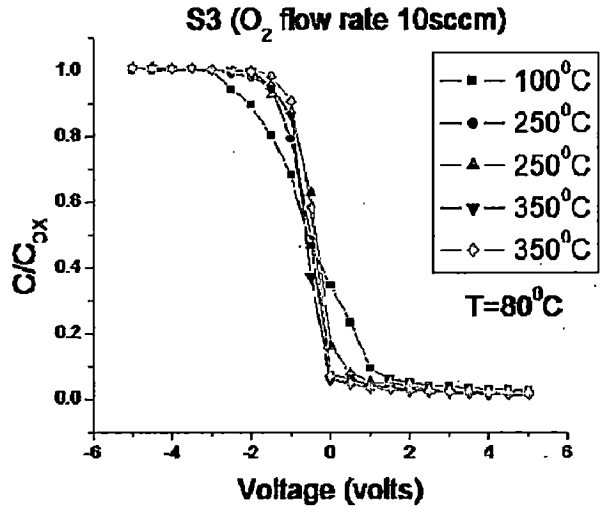
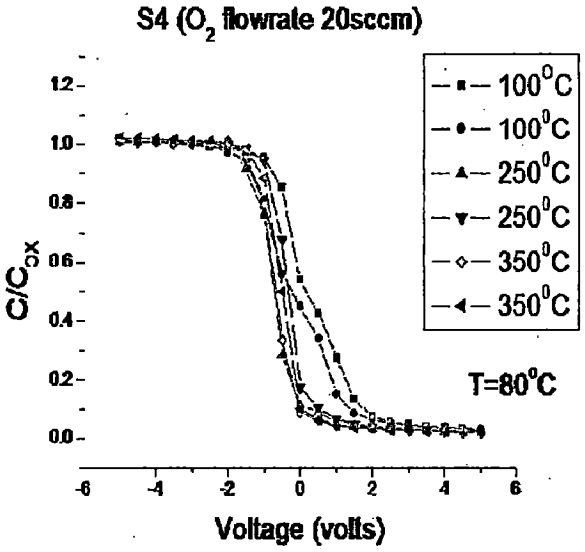
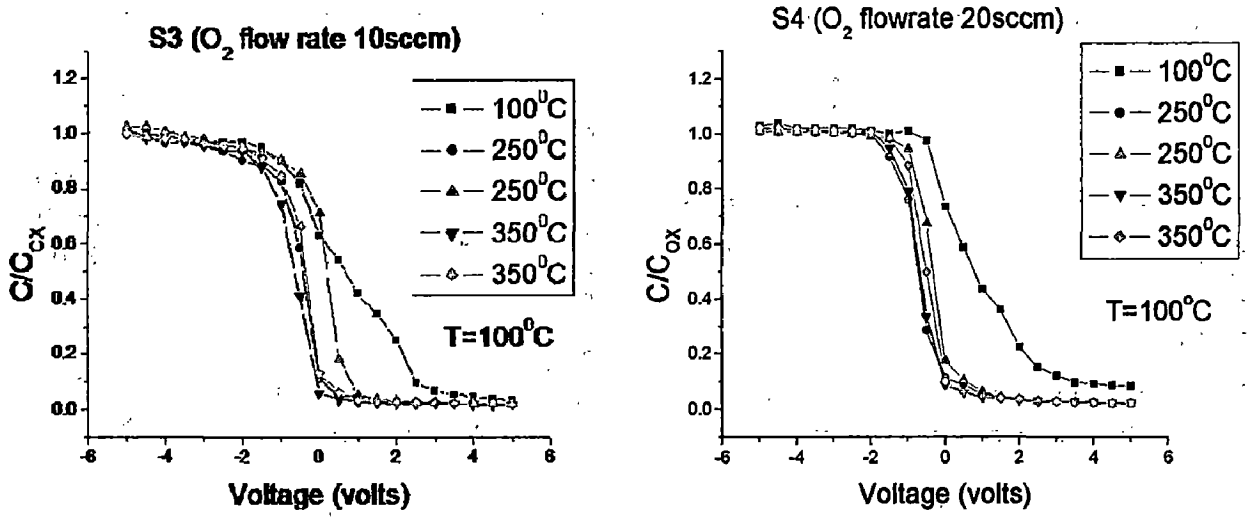


(c)



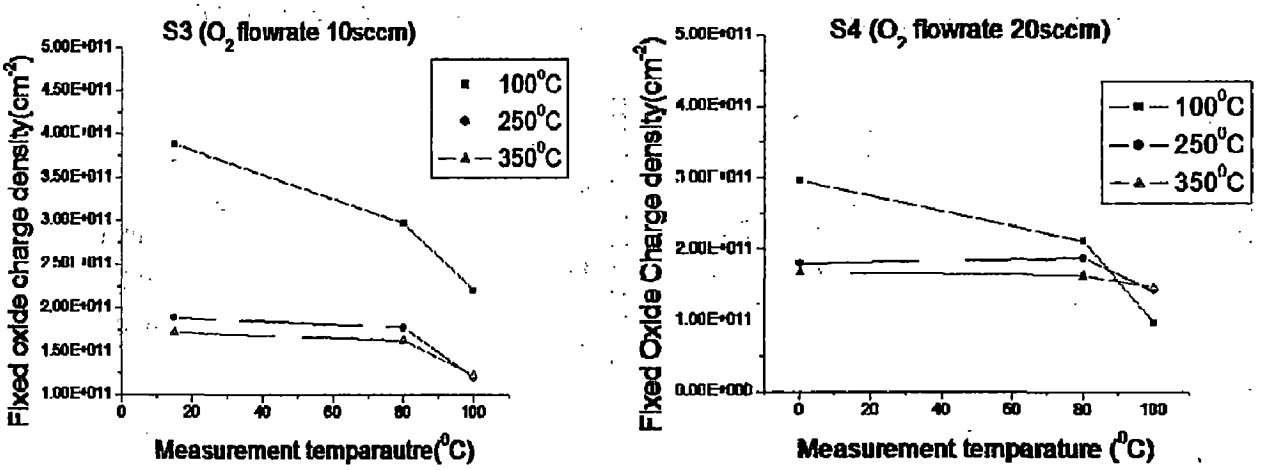
(d)



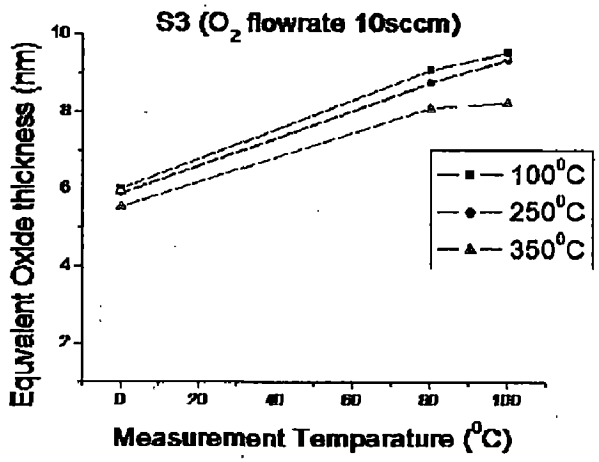
(e) (f)

Figure 3.4 100 kHz C-V curves corresponding to annealed Al/ ZrO_2/p-Si MIS devices, sample S3measurement at (a) 15°C (c) 80°C (e) 100°C and for sample 42 measurement at (b) 15°C (d) 80°C (f) 100°C.

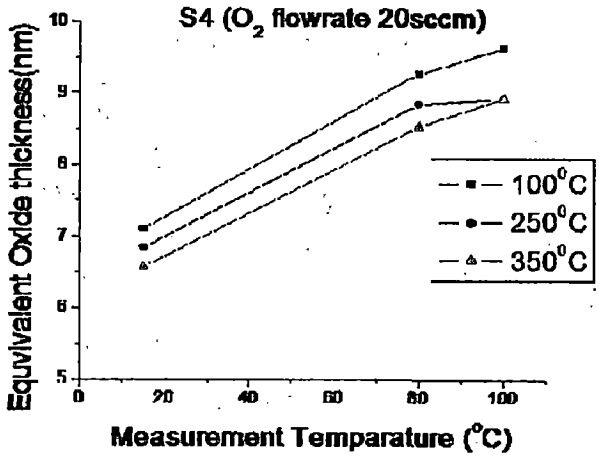
They show the variation of threshold voltage with annealing temperature. Samples which are annealed at 350°C indicate stable threshold voltage. A threshold voltage of 0.7±0.2 is measured in the case of sample S3 after annealing at 350°C. And in case of sample S4 threshold of 0.3±0.1 is measured.



(a) (b)



(c)



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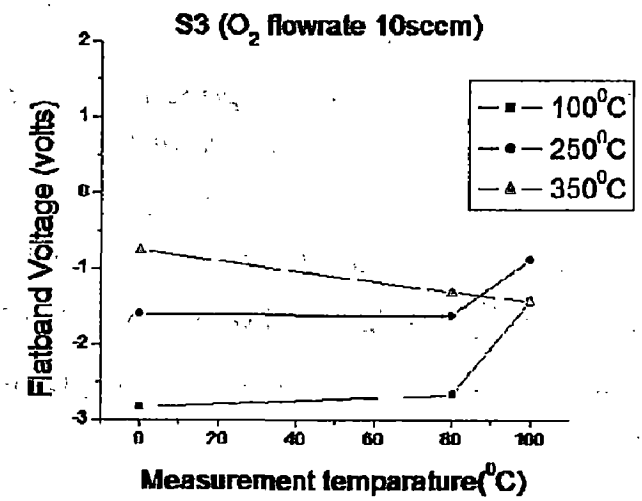
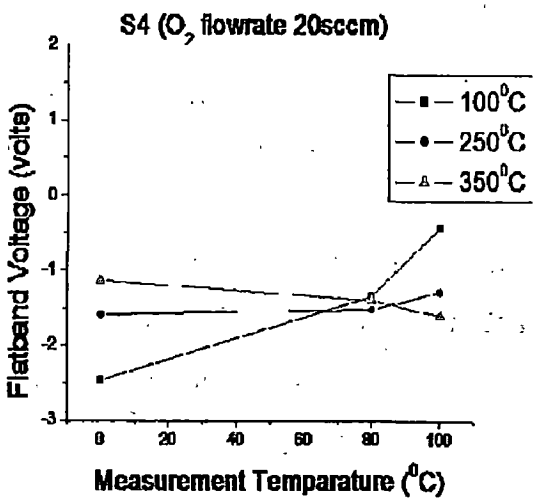


(e)



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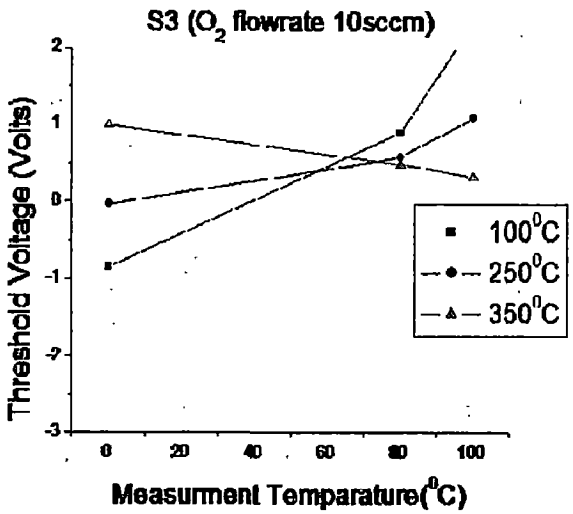
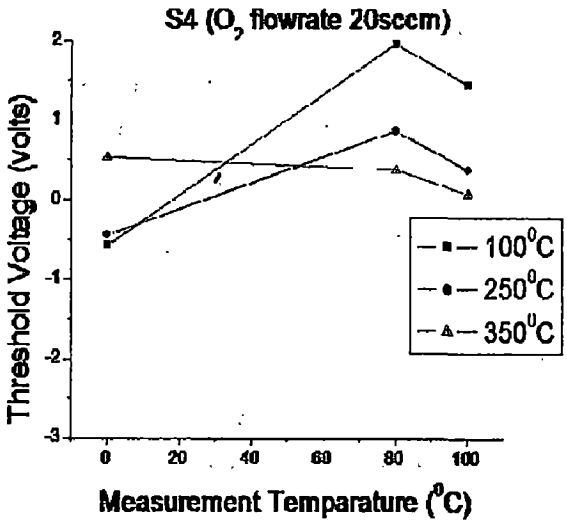


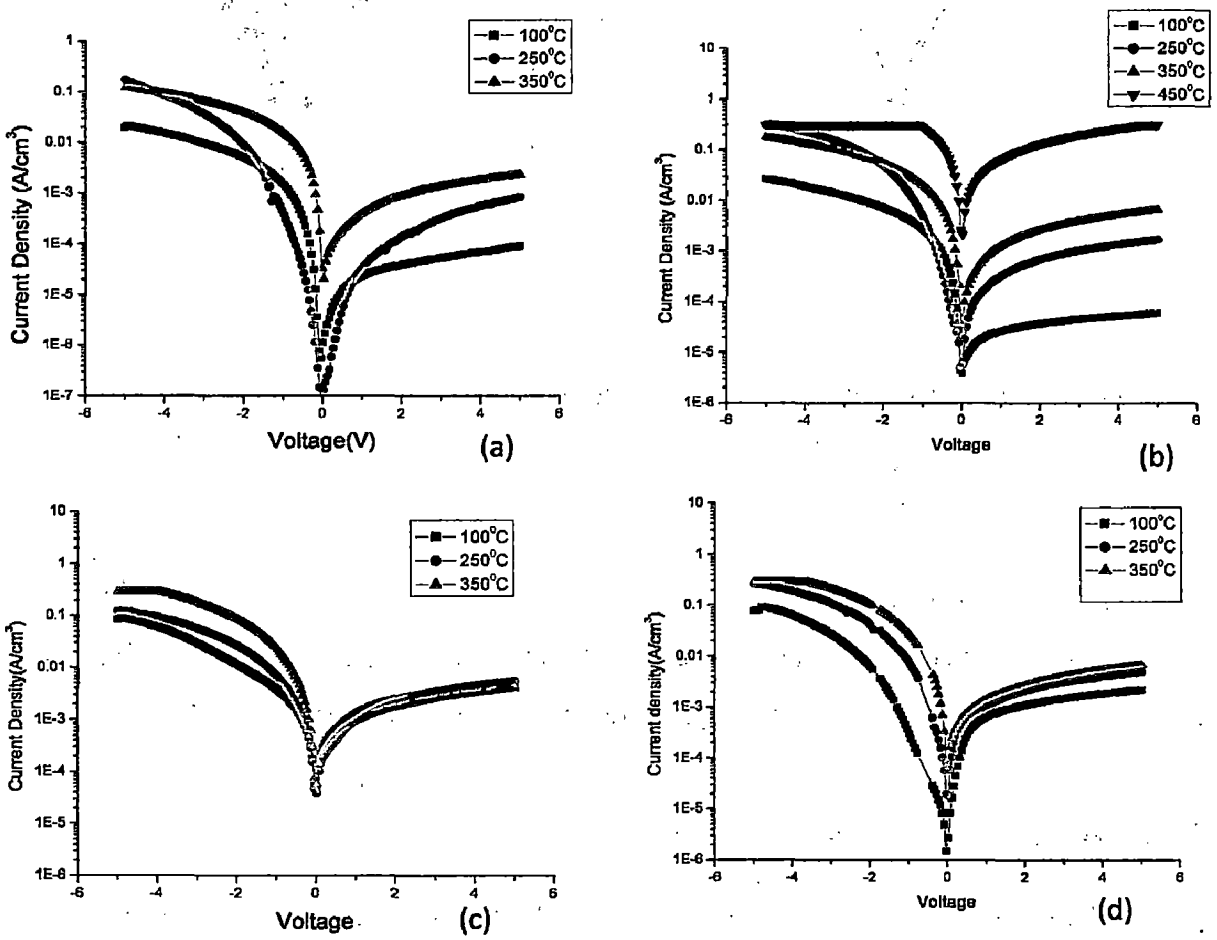
(g)



(h)

***Figure 3.5** Plots of variation of parameters with measurement temperature for Al/ ZrO_2/p-Si MIS capacitors at different annealing temperatures for sample S3: (a) Fixed oxide charge density (/cm^2), (c) Equivalent oxide thickness(cm), (e) flat band voltage (volts) and (g) threshold voltage (volts) and for sample S4: b) Fixed oxide charge density (C/cm^2), (d) Equivalent oxide thickness(cm), (f) flat band voltage (volts) and (h) threshold voltage (volts).*

Al/ZrO_2/P-Si MIS Capacitors deposited at lower O_2 flow rate shows better results in Capacitance –Voltage Measurement with lesser fixed oxide charges and low interface states. (Sample 2 has better results compared to sample1). Increase in O_2 flow rate shows increase in interfacial layer with in annealing due to high diffusion rates of oxygen which induces more interfacial layer due to formation of SiO_2 at ZrO_2 and Si interface.



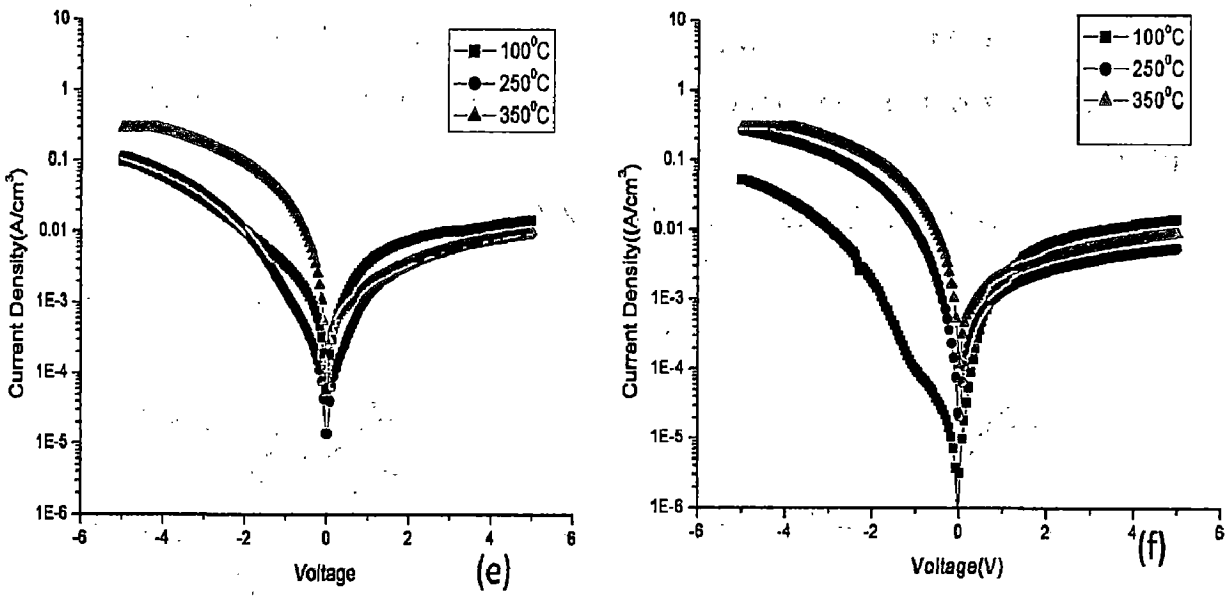


Figure 3.6 Variation of current density (A/cm^2) with supplied voltage (volts) for Al/HfO$_2$/p-Si MIC Capacitors sample S1: measurement at (a) at 15^{0}C (b) at 80^{0}C (c) at 100^{0}C and for sample S2: measurement at (a) at 15^{0}C (b) at 80^{0}C (c) at 100^{0}C.

3.3.3 Leakage current measurements

The dependences of leakage current on temperature are investigated to elucidate the electrical conduction mechanisms of high-k dielectric MIS capacitors.

(A) Al/HfO$_2$/P-Si MIS capacitors

Leakage characteristics of Al/HfO$_2$/p-Si MIS capacitors are measured at three different temperatures at room temperature, 80^{0}C and 100^{0}C.

From the graphs of leakage current with voltage, it is evident that leakage current is mainly due to Pool-Frenkel and Schottky emission. Due to presence of bulk traps inside dielectric pool Frenkel conduction is dominant at low electric fields (≤1.5MV/m). At high electric fields Schottky emission is the dominant mechanism.

Figure 3.6 (a) and (b) shows the leakage currents measured at room temperature for samples S1 and S2. They indicate increase in leakage current with increase in annealing temperature which results in due to crystallization of dielectric layer. Leakage current due to electron injection from substrate is higher compared to leakage current in metal gate injection indicating more conduction band offset between HfO$_2$ and Si interfaces than that of HfO$_2$/Al interface. Sample S1 exhibits more leakage compared to sample S2 for all annealing

conditions. Leakage currents are increased greatly with increase in crystallenity because grain boundaries inside dielectric provide more leakage paths. Increase in critical electric field, where the conversion of pool-Frenkel to Schottky takes place, is reported in case of annealed samples at 200^0C.

In Figure 3.6(c) and (d) the leakage currents measured at 80^0C for samples S1 and S2 are shown. The results show that leakage currents are mainly dominant by Schottky emission. At high temperatures effective fixed oxide charges are low due to decrease in scattering of fixed charges inside bulk. Same phenomenon is notice for measurement at 100^0C for both samples figured in 3.6(e), (f). They indicate samples which are annealed at 250^0C results large number of traps near Si and HfO_2 interface.

From the leakage characteristics it is identified that there is increase in leakage current with increase in annealing temperature and it is converting from bulk limited mechanism to interface limited mechanisms. Annealing at high temperature results in polycrystalline nature of dielectrics noticed from XRD results resulting leakage paths provided by formation of grain boundaries in dielectric layer.

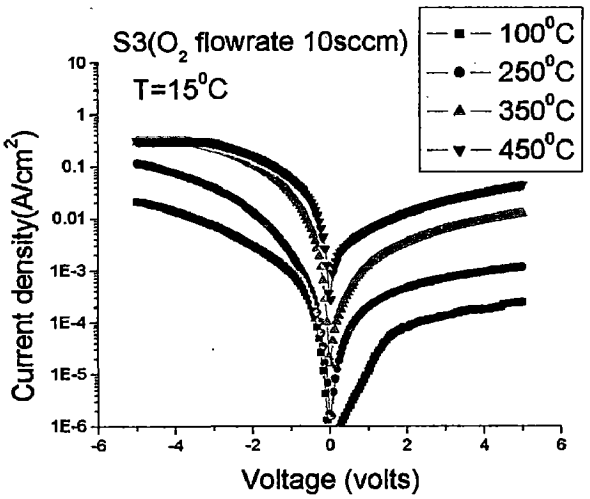
(B) Al/ZrO_2/p-Si MIS capacitor

Leakage characteristics for Al/ZrO_2/p-Si MIS capacitors prepared with different annealing temperatures are measured at room temperature, 80^0C and 100^0C. We identified Schottky and pool-Frenkel leakage mechanism in these high-k dielectric capacitors. Figure 3.7 exposes leakage characteristics of Al/ZrO_2/p-Si MIS capacitors for sample S3 and S4. All the curves signify increase in leakage current with increase in annealing temperature. For samples annealed at high temperature exhibits Schottky emission. In the same way at low electric fields and capacitors which are annealed at low temperatures exhibits pool-Frenkel conduction.

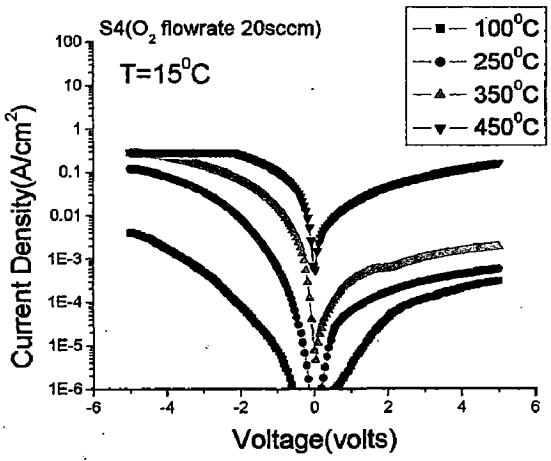
Figure 3.7(a) and (b) shows leakage current characteristics of sample S3 and sample S4 at different annealing temperatures. Leakage current increases with increase in annealing temperature and Schottky mechanism is dominant for high temperature annealed samples.

Figure 3.7 (c) and (d) shows leakage current characteristics of sample S3 and S4 at 80^0C in substrate electrode injection leakage current decreases with increase in annealing temperature resulting in the increase in interfacial layer and reduction in trap charges. At

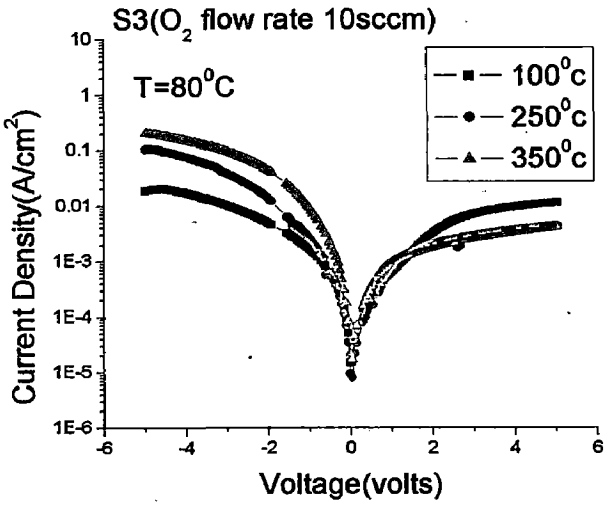
high temperature band bending effect at interfacial layer is significant. So Schottky mechanism is dominant for high temperature leakage measurements. Increase in annealing temperature reduces the number of effective traps, so trap assisted leakage decreases significantly with increase in annealing temperature. Injected electrons must possess high energy to overcome the barrier.



(a)



(b)



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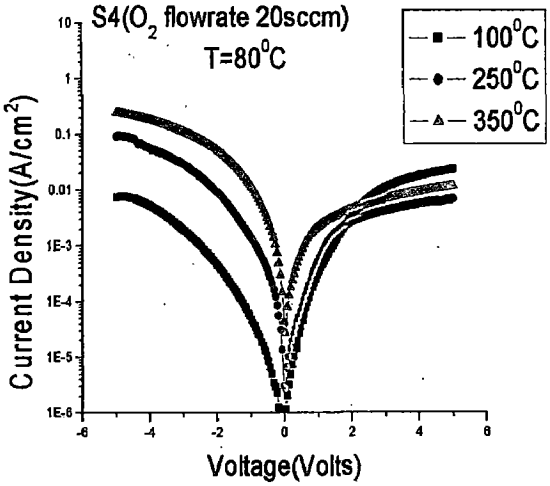

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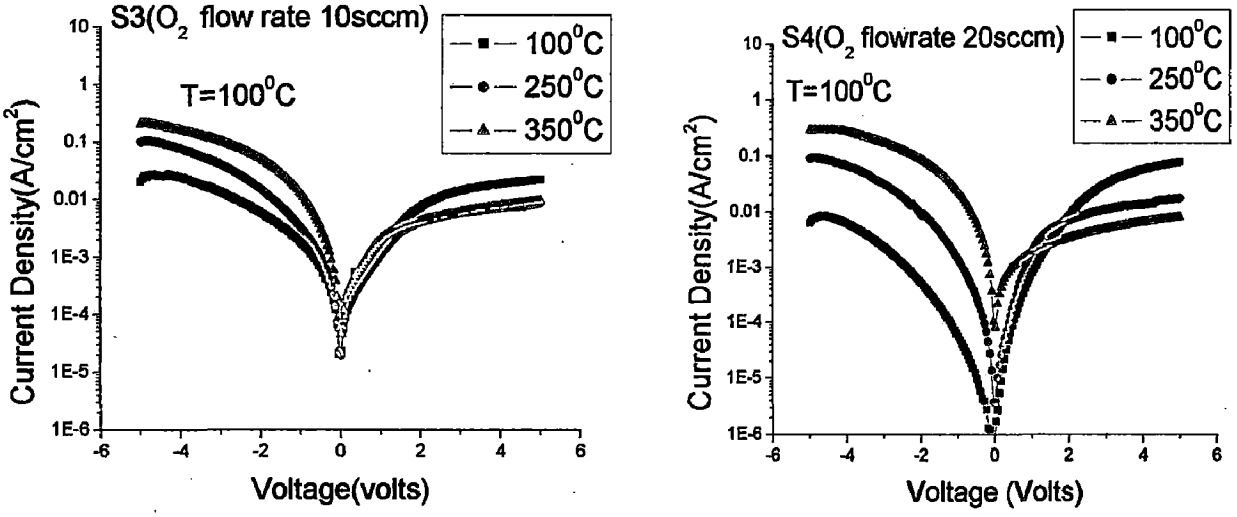

(e) **(f)**

***Figure 3.7** Variation of current density with supplied voltage for Al/ZrO_2/p-Si MIS Capacitors sample S1: measurement at (a) at 15°C (c) at 80°C (e) at 100°C and for sample S2: measurement at (b) at 15°C (d) at 80°C (f) at 100°C.*

Same effect is observed for samples measured at a temperature of 100°C. Results of sample S3 and S4 measured at 100°C are shown in Figure 3.7(e), (f). In case of metal gate injection of electron leakage current is mainly dominated by pool Frenkel at low electric field and at high electric field it is dominant Schottky emission. Increase in annealing temperature results in increase of leakage currents which is dominant by Schottky emission.

From the leakage characteristics it is identified that leakage current increases with annealing temperature and it is converting from bulk limited mechanism to interface limited mechanisms. Annealing in N_2 causes the reduction in number of fixed oxide charge traps inside dielectric material. It also results in formation of interfacial layer. Figure 3.8 shows band diagram which signifies leakage current due to Schottky emission form substrate, pool Frenkel conduction form substrate, and Schottky emission for metal to dielectric and pool Frenkel emission from metal to dielectric.

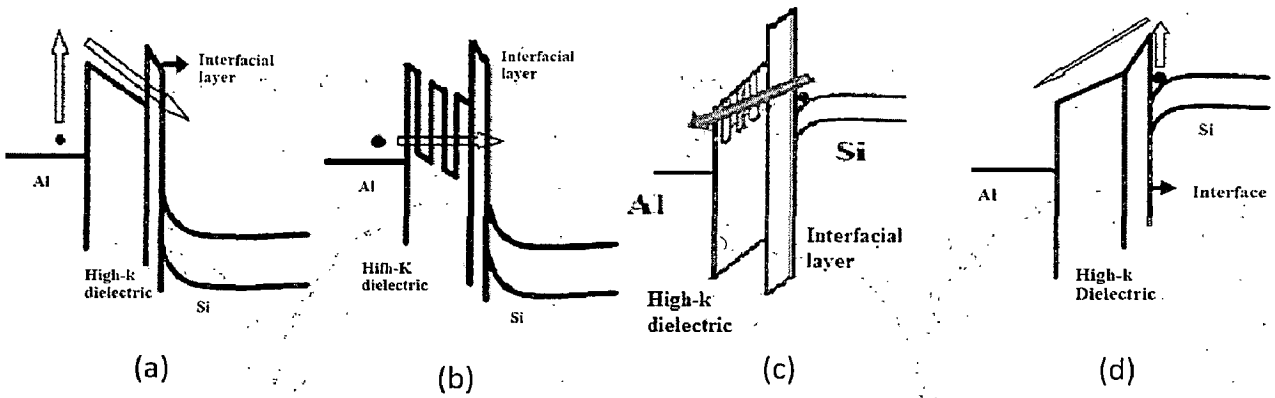

Figure 3.8 Band diagrams for Al/high-k/Si indicating different region indicating (a) Schottky emission in high E-field under metal gate injection (b)Pool-Frenkel emission in low electric fields at metal gate injection (c) Pool-Frenkel emission in low electric fields at substrate injection (d) Schottky emission in high E-field under substrate injection [2, 4].

3.4 Conclusion

Al/HfO_2/p-Si and Al/ZrO_2/p-Si MIS capacitors are fabricated using sputtering and evaporation techniques. Physical and electrical characterizations of these capacitors are done using XRD analysis and high frequency (100 kHz) C-V curves and leakage current characteristics. Changes in properties with variation in annealing temperature and measurement temperature are studied.

XRD analysis signifies that deposited thin films are amorphous in nature where as polycrystalline peak is noticed for HfO_2 coated films at 28.3^0 which indicates monoclinic phase of HfO_2 after annealing at 450^0C. Whereas ZrO_2 coated thins are observed to be amorphous in nature up to annealing at 450^0C.

High frequency Capacitance-Voltage (C-V) curves indicates reduction in fixed oxide charges with increase in annealing. In case of high temperature measurements interface trap charges effects the C-V curves studied by the dispersion and reduction in C_{ox} value of C-V curves. The effective number of fixed oxide charges reduces with increase in measurement temperature which signifies the movement of oxide trap charges near to dielectric interface with increase in annealing temperature. Same effect is noticed for all capacitors. But increase in annealing temperature reduces the effective interface trap charges also which results less dispersion in C-V curves.

From the leakage current characteristics it is identified those leakage current increases exponentially with annealing temperature. The leakage currents are mainly dominant by two mechanisms pool-Frenkel and Schottky emission. At low electric fields pool Frenkel conduction is dominant and in case of annealed samples due to reduction of oxide trap charges leakage current is mainly dominant by Schottky emission. Increase in annealing temperature results in diffusion of O_2 inside dielectric that causes formation of SiO_2 at interface. Compared to HfO_2, ZrO_2 based capacitors exhibits more diffusivity for O_2. Increase in O_2 content while deposition results in higher equivalent oxide thickness (EOT) due to formation of SiO_2 interface.

Finally Al/HfO_2/p-Si and Al/ ZrO_2/p-Si MIS capacitors with effective EOT of 6±0.5nm and 8±0.5 nm are fabricated and characterized at different measurement temperatures and at annealing conditions. With this study samples which are annealed at 350°C exhibits superior characteristics for both the cases of HfO_2 and ZrO_2 based capacitors with dielectric constants of ~21 and ~18.5 respectively. In the next following chapter we discuss reliability characteristics of these capacitors.

3.5 References

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CHAPTER 4

STUDY OF RELIABILITY ON $Al/HfO_2/p\text{-}Si$ AND $Al/ZrO_2/p\text{-}Si$ MIS CAPACIOTRS

4.1 Introduction

The reliability of oxides is typically tested by Constant Current Stress (CCS) and Constant Voltage Stress (CVS) to a MOS capacitor [1-5]. The thin dielectric layer gradually degrades until breakdown occurs. Breakdown is triggered when an accumulated damage reached a critical level. During oxide stress several phenomena can be observed: interface trap creation, negative and/or positive charge trapping, neutral electron trap creation and the generation of Stress Induced Leakage Currents (SILCs) [6].

During high field oxide stressing interface traps are created at substrate/oxide interface [6]. Their density can be obtained from C-V measurements. It has been claimed that the interface trap density D_{it} reaches a critical level, D_{itcrit}, at the moment of oxide breakdown [2, 4].

Breakdown phenomenon can be explained by plotting variation of fixed oxide charge with stress time [1, 5]. During constant current stress, locally enhanced field increases the leakage current density resulting in an increased electrical stress, which in turn leads to an increased positive charge trapping. In this way a positive feedback mechanism is initiated that finally results in positive charge trapping. Stress Induced Leakage Currents is illustrated by the variation of leakage current with respective voltage with different stress timing. The generation of trap charges is mainly explained by two basic models: anode hole injection model [7] and hydrogen release model [8].

In Case of high-k dielectrics charge trapping is the dominant reliability factor for various samples that we have tested. Stress Induced Leakage currents (SILCs) in $Al/HfO_2/p\text{-}Si$ and $Al/ZrO_2/p\text{-}Si$ after short and long constant current stress (CCS) and temperature aided constant current stress are investigated. The behavior of SILCs and quasi static C-V curves are plotted. Conduction mechanisms are also investigated.

4.2 Experimental Details

4.2.1 Substrate Preparation

Boron doped p-type Silicon substrates sliced in [100] direction is used to in this work. Substrates of area 1cm × 1cm are taken from the wafer. Substrates are cleaned with acetone, N_2, ultra sonic cleaner and 2% HF: H_2O. The procedure of cleaning is described in Appendix A. Prior to the deposition of dielectric material a thin (100-200nm) Aluminium layer is deposited on backside unpolished surface using Thermal Evaporation System. To form a strong ohmic contact substrates are annealed at 450^0C in N_2 ambient at pressure 100mbar for 15 minutes [11]. All substrates were mounted onto a plate with silver paint and loaded into the sputtering system. A portion of each substrate surface was covered in silver paint for thickness measurement after growth.

4.2.2 Film growth

Thin films of HfO_2 and ZrO_2 are deposited by Reactive Radio Frequency Magnetron Sputtering. The deposition parameters are described in table 4.1. The pressure inside the chamber was chosen 2 times higher in conventional ones. Due to high pressure inside the chamber the mean free path of Ar and O_2 gas is significantly low (around 0.05mm) [10] Therefore the sputtered and reflected particles emitted from the target collide with the gas medium, losing their energy etherealize within a short distance about 0.16cm for sputtered atoms and 0.27cm for reflected atoms [10]. The thermalization length is much smaller than the target-substrate distance (5cm) and the movement of sputtered particles is mainly due to diffusional process. Consequently, the energy deposited by sputtered atoms should be low preventing damage of substrates and the growing film is independent of processing gas.

Table 4.1 Sputtering parameters for deposition of HfO_2 and ZrO_2 films.

Parameters	HfO_2 sputtering	ZrO_2 sputtering
Target	2 inch 99.9% Hafnium	2 inch 99.9% Zirconium
Base Pressure (Torr)	2×10^{-6}	2×10^{-6}
Sputtering pressure(mTorr)	20	20
Ar gas flow (sccm)	20	20
O_2 gas flow(sccm)	20	20
Substrate temperature	200^0C	200^0C
Sputtering Power	RF power 50W	RF power 50W
Target Distance (cm)	5	5
Sputtering Time (min)	2	2

Increase in substrate temperature results in deposition of material is increased results in deposition of material in equilibrium with good adhesion properties. After deposition samples are annealed at 200°C for 30 minutes that helps in decrement of oxide charges.

After deposition of dielectric films, thin layer of aluminium of thickness 150-200nm is deposited on top of HfO_2 film through shadow mask using physical evaporation method. Masks are prepared by having a circular hole of radius 1mm.

4.2.3 Measurements

Fabricated Al/HfO_2/p-Si and Al/ZrO_2/p-Si MIS capacitors are subjected to electrical measurements. Constant current stress of 1mA in accumulation region is applied to MIS capacitors of area 3.14 $\times 10^{-2} cm^2$. Leakage current and capacitance voltage characteristics are measured at various stress timings at 10s, 100s, 1000s, 2000s, 5000s and 10000s. Same experiment is repeated along with high temperature stress at 80^0C.

4.3 Results and Discussions

4.3.1 Study of constant current stress on Al/HfO_2/p-Si MIS Capacitor

Figure 4.1 shows variation of high frequency (100 kHz) capacitance curve with voltage at different stress times. With the increase in stress time, capacitance curves shifts in negative direction indicating increase in positive fixed oxide charges. Stress current of -1mA stimulates increase in electric field across the dielectric layer leads to increase in current, resulting an increased stress, which in turn leads to positive charge trapping. In this way positive feedback mechanism is initiated that finally results in breakdown of device.

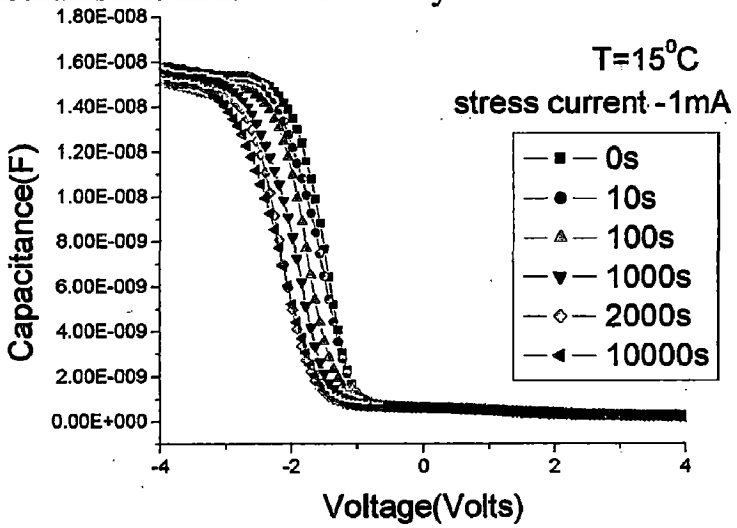


Figure 4.1 Variation of (high frequency 100 kHz) C-V curves for Al /HfO_2/p-Si at CCS of-1mA from metal gate at room temperature (15^0C).

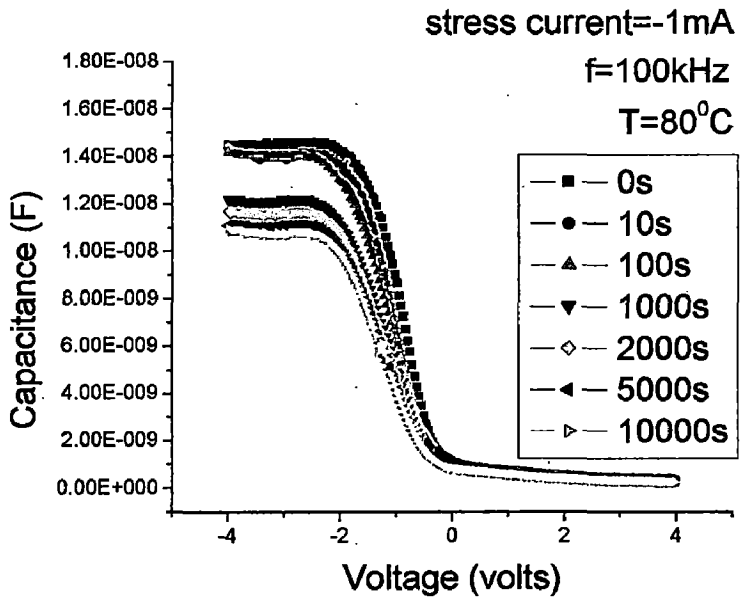
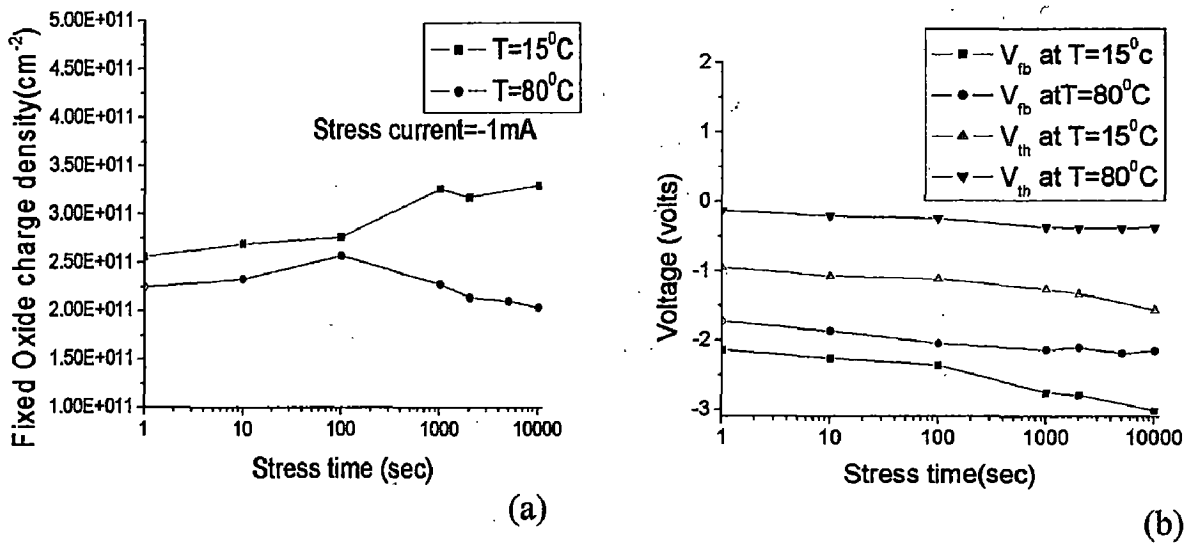


Figure 4.2 Capacitance (F)-Voltage (volts) characteristics of Al /HfO_2/p-Si CCS (-1mA at metal gate) at 80°C.

Figure 4.2 shows C-V characteristics of Al/HfO_2/p-Si MIS capacitor under constant current stress of 1mA in accusation region measured at 80°C temperature. From figure it is identified that increase in stress time results in shifting of curves in negative direction, which indicates increase in fixed oxide charges. Slope of C-V curve observed at midgap capacitance decreases due to thermal agitated constant current stress which signifies increase in interface trap charges. The increase in interface trap charges acts as a decapping layer which results decrease in Oxide capacitance (C_{ox}). A shift in flat band voltage in negative direction is studied.



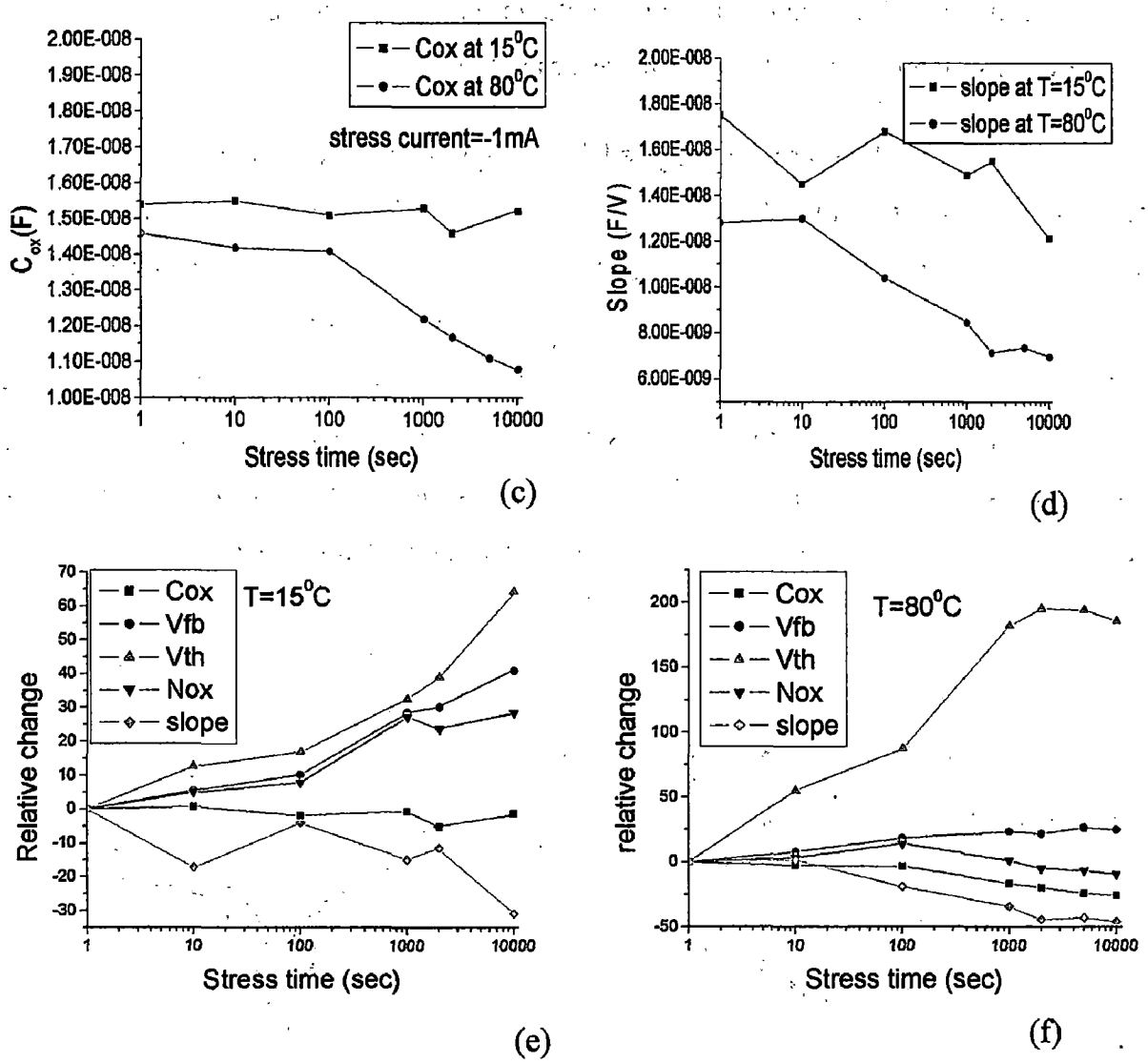


***Figure 4.3** Study of CCS on (a) fixed oxide charge N_{ox} (cm^{-2}) (b) fltaband V_{fb} (volts), threshold voltage V_{th} (volts) (c) Oxide Capacitance C_{ox} (F) (d) slope at midgap (F/V) at 15°C and 80°C and relative percentage change in C_{ox}, V_{fb}, V_{th} and slope for (e) measurement at 15°C (f) measurement at 80°C.*

Figure 4.3 (a) shows variation of fixed oxide charge density with stress time for constant current stress. At low temperature fixed oxide charge density increases with progressing of constant current stress and in case of high temperature CCS at longer stress it decreases with stress time. It points out increase in fixed oxide charges, generated due to constant current stress, move towards interface results in increase of interface trap density pointed out by increase in dispersion of C-V curves (Figure 4.2) and reduces the oxide capacitance C_{ox} (from Figure 4.3(c)). Because induced interface traps acts as decapping layer and reduces the dielectric capacitance of devices. Figure 4.3 (b) shows that constant current stress at low temperature results in decrease of flatband voltage and threshold voltage effectively compared to thermal aided constant current stress. Where as in case of temperature aided constant current stress increase traps near the interface. The difference

between flat band voltage and threshold voltage is higher compared to that in low temperature constant current stress and it increases with stress time.

Properties of SILCs are investigated by studying the variation in leakage current characteristics with stress time. Figure 4.4 (a) shows the effect of constant current stress of 1mA in accumulation region at room temperature. Primarily there are two major conduction mechanisms are noticed which are pool Frenkel in case of substrate injection and at low electric fields of metal gate injection and at high electric fields of metal gate injection signifies Schottky emission. This mechanism can be explained by the presence of large number of traps near the interface of dielectric and substrate. In case of metal gate injection primarily leakage current is dominant due to defects and at high electric field Schottky emission is dominant.

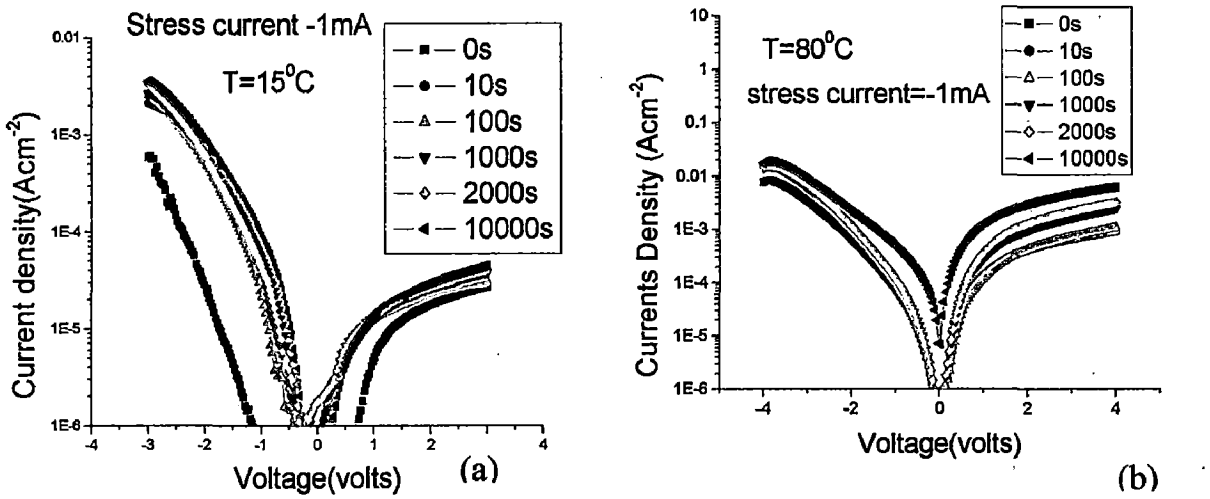


Figure 4.4 Variations of leakage current density (Acm^{-2}) characteristics in $Al/HfO_2/p$-Si capacitor with CCS (-1mA at metal gate) (a) Measurement at 15°C (b) Measurement at 80°C.

Figure 4.4(b) shows the deviation of leakage currents with respect to CCS of 1mA at 80°C. It points out that for substrate injection of electron, leakage current is mainly dominant by Pool-Frenkel conduction mechanism, due to presence of large number of fixed and/or interface traps inside the bulk, near dielectric and substrate interface. With progress in stress time results in more leakage current across the bulk. Whereas longer stress time causes leakage current is dominant by Schottky emission at high electric fields. In case of metal electrode injection, increase in stress time along with thermal stress results shift in critical electric field, (the electric field in which leakage mechanism shifts from bulk dependent to interface dependent), towards left side indicating the increase in current due to Schottky emission. Figure 4.5 shows the variation of leakage current at flat band voltage with increase in stress time of both CCS case and temperature aided CCS. It points out that films that are

stressed at room temperature exhibits more leakage current at shorter stress time compared to other. However for longer stress time temperature aided CCS exhibits large leakage currents.

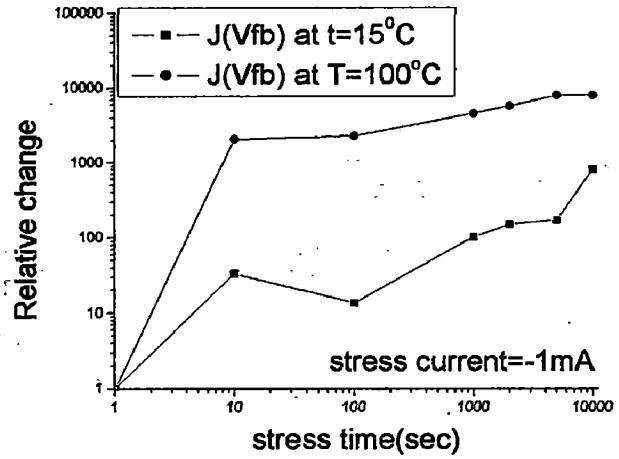


Figure 4.5 Variation of leakage current density (A/cm^{-2}) at flat band voltage with stress time for Al/HfO_2/p-Si at fixed CCS (-1mA from metal gate) at temperatures 15^{0}C and 80^{0}C.

4.3.2 Study of constant current stress on Al/ZrO_2/p-Si MIS Capacitor

Figure 4.6 shows the deviation in high frequency (100 kHz) C-V curves by the application of constant current stress of 1mA at room temperature. It clearly shows increase in stress time results in generation of positive oxide charge with the progression of stress. The value of oxide capacitance is almost constant which is independent of stress time. It clearly shows no additional interface trap generation.

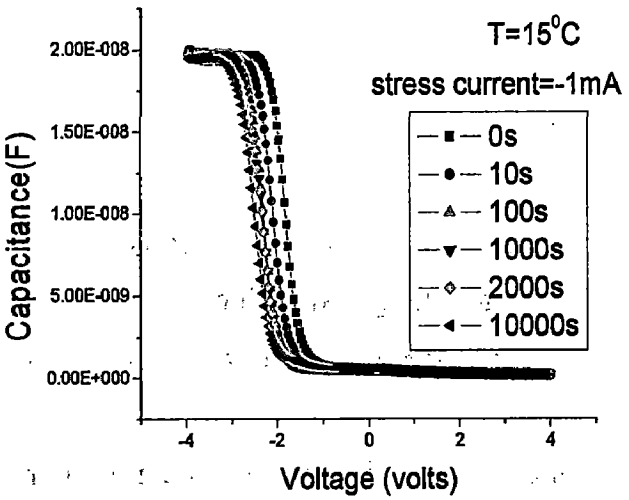


Figure 4.6 *Capacitance (F)-Voltage (V) plots for Al/ZrO_2/p-Si MIS structure under CCS at -1mA from metal gate.*

Figure 4.7 shows high frequency (100 kHz) C-V curves for application of thermal aided CCS at -1mA at 80^0C. It is identified that accumulation capacitance Cox is decreasing with the progression of stress. Capacitance curves are shifting in negative direction.

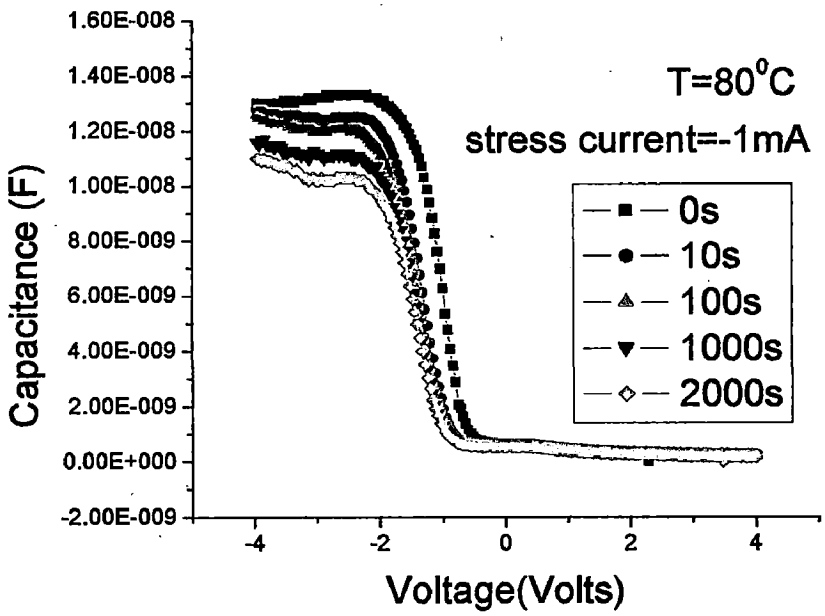


***Figure 4.7** Variation in capacitance-voltage curves for Al/ZrO_2/p-Si CCS of -1mA from metal gate at 80^0C.*

Figure 4.8(a) shows variation of effective fixed oxide charge density with stress time. At room temperature the number of oxide charges in ZrO_2 layer increases by the application of CCS as shown in figure. In case of thermal aided CCS study at shorter stress timing it increases with annealing. Where as in case of longer stress it exhibits decrease in fixed oxide charges.

Figure 4.8(b) shows variation of flat band voltage and threshold voltages with stress time. From the Figure, decrement in fltaband voltage and threshold voltage with CCS is noticed. Figure 4.8(c) shows variation of accumulation capacitance with increase stress time. It signifies increase in interface trap charges with increase in measurement temperature and CCS. In Figure 4.8 (d) maximum slope of C-V curve is calculated for both the case of CCS at room temperature CCS at 80^0C. With progress in stress time the slope of CV curve is decreased for both the cases and its values is lesser for the measurement at room temperature. Figure 4.8(e) and 4.8(f) shows variations relative % change in C_{ox}, V_{fb}, V_{th}, N_{ox} and slope of C-V curves. From the curves it is identified that degradation is mainly aided by shift in threshold voltage.

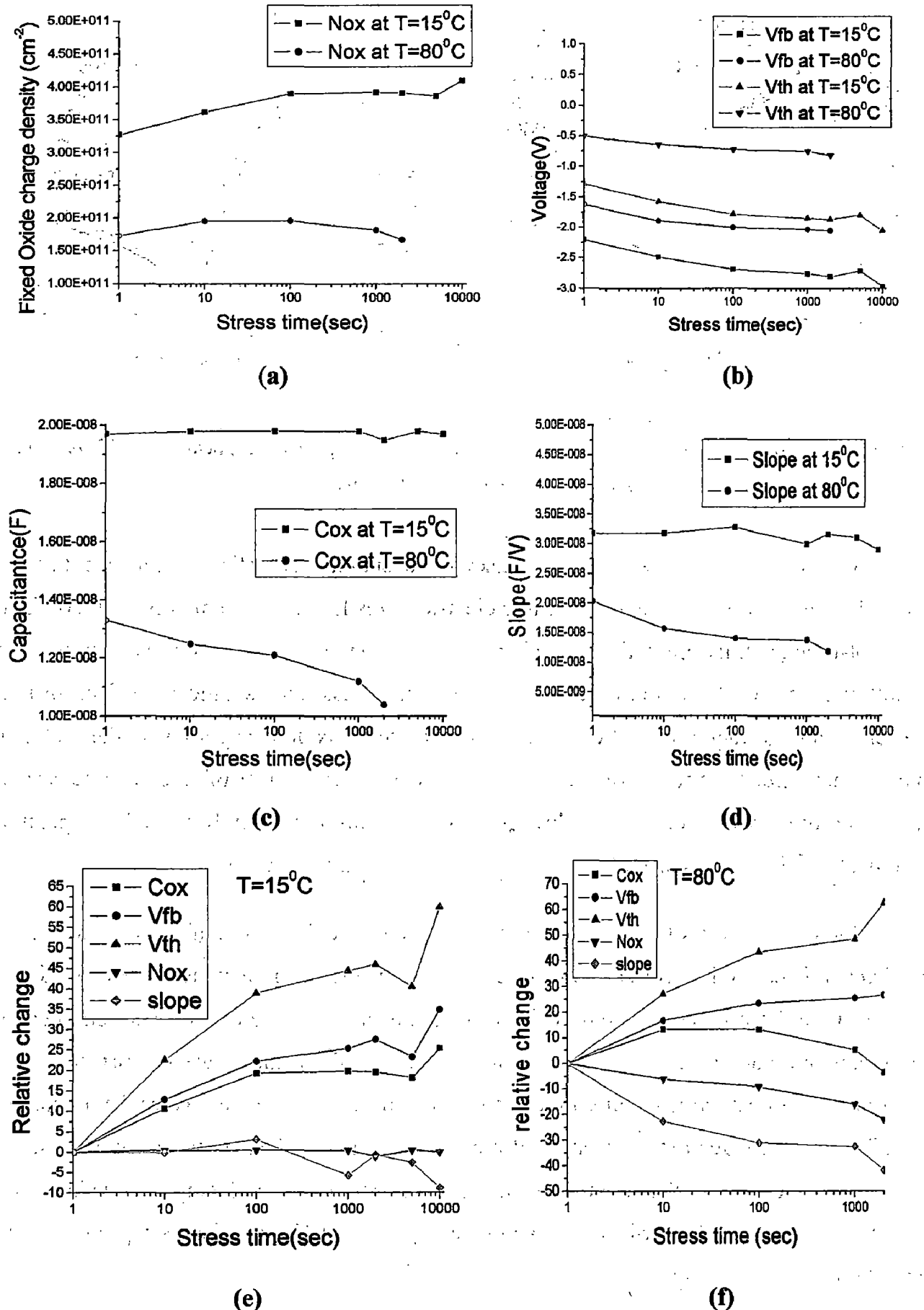


Figure 4.8 *Study of CCS on (a) fixed oxide charge N_{ox} (cm^{-2}) (b) flatband V_{fb} (V) , threshold voltage V_{th} (V) (c) Oxide Capacitance C_{ox} (F) (d) slope at midgap (F/V) at 15°C and 80°C and relative percentage change in C_{ox}, V_{fb}, V_{th} and slope for (e) measurement at 15°C (f) measurement at 80°C.*

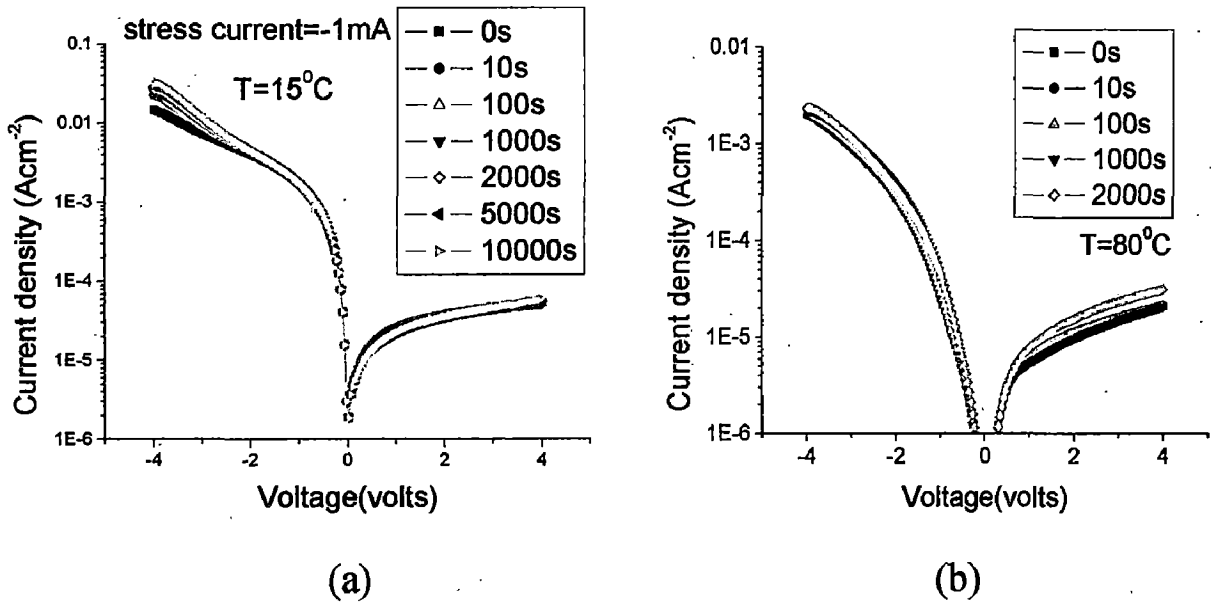
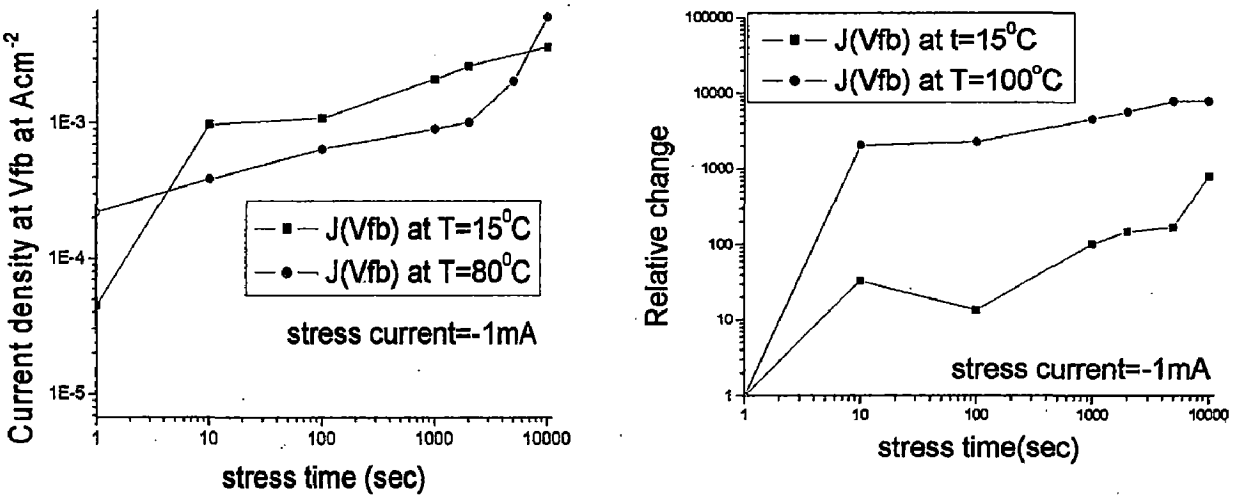


Figure 4.9 Deviation in leakage current characteristics for Al/ZrO₂/p-Si MIS capacitor with CCS of -1mA applied at metal gate (a) at 15°C (b) at 80°C.

Figure 4.9 shows discrepancy in leakage current characteristics with respect to CCS. From the curves it is identified that at low electric fields leakage current is mainly dominant by Pool-Frenkel bulk limited mechanism and at large electric fields it is dominant by Schottky emission. Variation in leakage current with stress time is almost constant for both the temperatures. Increase in stress results in increase in oxide charges inside the dielectric and the mean free time for carriers is lowered by increase in number of oxide charge carriers across the dielectric material. This lowering effect is observed mainly in high temperature current stress due to presence of large number of traps near the interface.

Increase in stress time results in critical electric field where shift in leakage current mechanism is pointed is shifted to higher electric fields indicating increase of leakage due to increase in bulk traps. The value of leakage current is higher in the case of electron injection from substrate compared to injection from metal gate. From the figure 4.9 (a) in case of substrate injection at large electric fields shows shift in leakage characteristics from Schottky to bulk limited conduction. The physical mechanism for this effect is not fully understood. However it is identified that degradation due to the effect of CCS and temperature aided CCS is less in case of Al/ZrO_2/p-Si MIS capacitors compared to HfO_2 based MIS capacitors under same fabrication conditions.



(a) (b)

Figure 4.10: Variation of leakage current density (A/cm^{-2}) at flat band voltage with stress time for Al/ZrO_2/p-Si at fixed CCS-1mA at metal gate (a) at 15°C (b) at 80°C.

In Figure 4.10 variation of leakage current density at flat band voltage with respective to CCS and CCS at high temperature is plotted. From both the curves it is observed that degradation is higher in case of CCS at room temperature. From the Figure 4.10 it is observed that relative percentage change in current at flat band voltage is higher in case of temperature aided CCS. The Stress Induced Leakage Current is comparative low in case of temperature aided CCS its relative change at flat band is higher.

4.4 Conclusion

In this chapter reliability studies on Al/HfO_2/p-Si and Al/ZrO_2/p-Si are explored. A constant current of -1mA is applied to the gate metal. Periodic measurement of leakage current and capacitance are performed to measure the discrepancy in the curves. From curves it is identified that increase in leakage current with increase in stress time. By the application of CCS at room temperature, following effects are studied. There is increase in fixed oxide charge, negative shift in flat band voltage and threshold voltage, increase in discrepancy of curves and increase in critical electric field. In case of temperature aided stress along with above mentioned effects decrease in oxide capacitance is also noticed.

However it is observed that ZrO_2 based MIS capacitors are more reliable compared to HfO_2 based MIS capacitors. And temperature aided CCS is the more degrading mechanism compared to CCS at room temperature.

4.5 References

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CHAPTER 5

STUDY OF RELIABILITY ON Al/ZrO_2/HfO_2/p-Si AND Al//HfO_2/ZrO_2/p-Si MIS CAPACIOTRS

5.1 Introduction

Mixing of oxides is a suitable technique to improve their electrical properties and structural properties on silicon [1-2]. HfO_2 based ternary oxides research is concentrated mainly on aluminates ($HfAlO_x$) [5], silicates ($HfSiO_x$) [4-5] and mixed oxide solid solutions of (HfO_2 and ZrO_2) [6-7].

Another approach for multicomponent dielectric layers is depositing them in laminated structures by using the precise layering capabilities of the deposition techniques such as ALD, sputtering and PLD. Laminate structures, are also called nanolaminates, and are proposed for improving electrical properties (permittivity, leakage current and breakdown) of oxides. Basic parameters of lamination, like the layer sequence and individual layer thickness and deposition ambient on the electrical and morphological properties of the ZrO_2-HfO_2 laminates. HfO_2 and ZrO_2 are so similar in many physical and chemical aspects that they are called twin oxides, and their similarity is attributed to their similar crystal structures.

Using the study of annealing (chapter 2) and reliability (chapter 3) of binary oxides HfO_2 and ZrO_2 as a dielectric material as a benchmark, laminate structures of ZrO_2 and HfO_2 are grown on p-type silicon by sputtering.

5.2 Experimental Details

5.2.1 Device fabrication

A thin layer of high-k dielectric material is deposited on polished cleaned substrate [Appendix A] through Reactive Radio Frequency Magnetron Sputtering [Appendix B]. In case of Al/HfO_2/ZrO_2/p-Si, on cleaned substrate a thin layer of ZrO_2 is deposited at 200^0C. The expected thickness of coating is 15-20nm. On top of ZrO_2 layer, after deposition, sample

is annealed at 200^{0}C for 30 minutes. On top of ZrO_2 layer HfO_2 film (expected thickness 15-20nm) is sputtered for 1minute. After deposition of HfO_2 samples are annealed at 200^{0}C for 25minutes. The recipe used for deposition of HfO_2 and ZrO_2 layers is shown in the Table 5.1. Similarly in case of Al/ZrO_2/HfO_2 MIS Capacitor On top of second dielectric, a layer of metal is deposited by Physical Vapor Deposition through evaporation process [appendix C]. A shadow mask having circular dots, each dot of radius 0.1cm is used to obtain a précised size. Expected thickness of coating is maintained to be 150-200nm. Prior to the deposition of dielectric, a stable ohmic contact is achieved between deposited metal on backside and silicon substrate. In our aluminium (Al) metal is used to form an ohmic contact. To form a stable ohmic contact after deposition of aluminium samples are annealed at 450^{0}C in nitrogen gas ambient of 10 bar of pressure for 15 minutes [3].

Table 5.1 Recipe used to sputtering of dielectric layer.

Parameters	**HfO_2 sputtering**	**ZrO_2 sputtering**
Target	2 inch 99.9% Hafnium	2 inch 99.9% Zirconium
Base Pressure (Torr)	2×10^{-6}	2×10^{-6}
Sputtering pressure(mTorr)	10	10
Ar gas flow (sccm)	20	20
O_2 gas flow(sccm)	20	20
Substrate temperature	200^{0}C	200^{0}C
Sputtering Power	RF power 50W	RF power 50W
Target Distance (cm)	5	5
Sputtering Time (min)	1	1
Insitu annealing	15 min at 100^{0}C in N_2	15 min at 100^{0}C in N_2
Expected thickness (nm)	15-25	15-25

5.2.2 Measurements

Fabricated Al/ZrO_2/HfO_2/p-Si and Al/HfO_2/ZrO_2/p-Si MIS capacitors are subjected to electrical measurements. Constant current stress of 1mA in accumulation region is applied to MIS capacitors of area 3.14 $\times10^{-2}$cm^2. Leakage current and capacitance voltage characteristics are measured at various stress timings at 10s, 100s, 1000s, 2000s, 5000s and 10000s. Same experiment is repeated at high temperature stress at 80^{0}C.

5.3 Results and Discussions

5.3.1 Study of constant current stress on $Al/ZrO_2/HfO_2/p\text{-}Si$ MIS capacitor

Figure 5.1 shows variation of high frequency (100 kHz) capacitance curve with voltage at different stress times. With the increase in stress time, capacitance curves shifts in negative direction indicating increase in positive fixed oxide charges. Along with that Threshold voltage is not varying as flat band voltage which shows increase in spreading of C-V curve by increasing voltage this can be modeled by increase in interface charges is large compared to increase in fixed oxide charge. The oxide charge inside the capacitor increases with increase in stress time. Stress current of -1mA stimulates increase in electric field across the dielectric layer leads to increase in current, resulting an increased stress, which in turn leads to positive charge trapping. In this way positive feedback mechanism is initiated that finally results in breakdown of device.

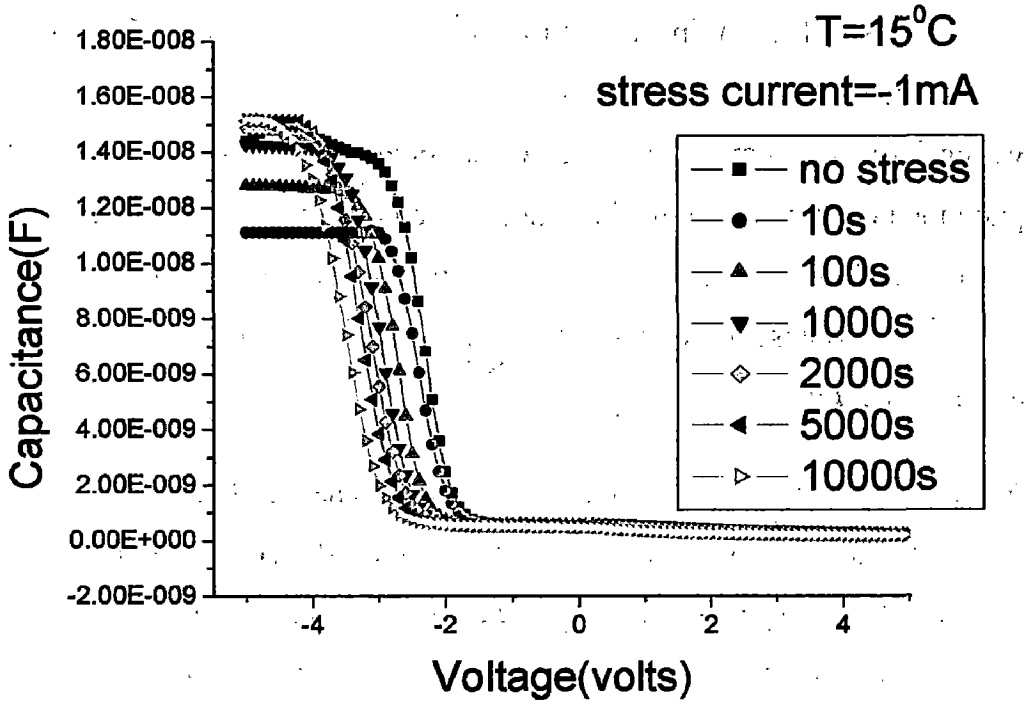


Figure5.1 Variation of high frequency capacitance (F) Vs voltage for $Al/ZrO_2/HfO_2/p\text{-}Si$ at CCS of -1mA from metal gate.

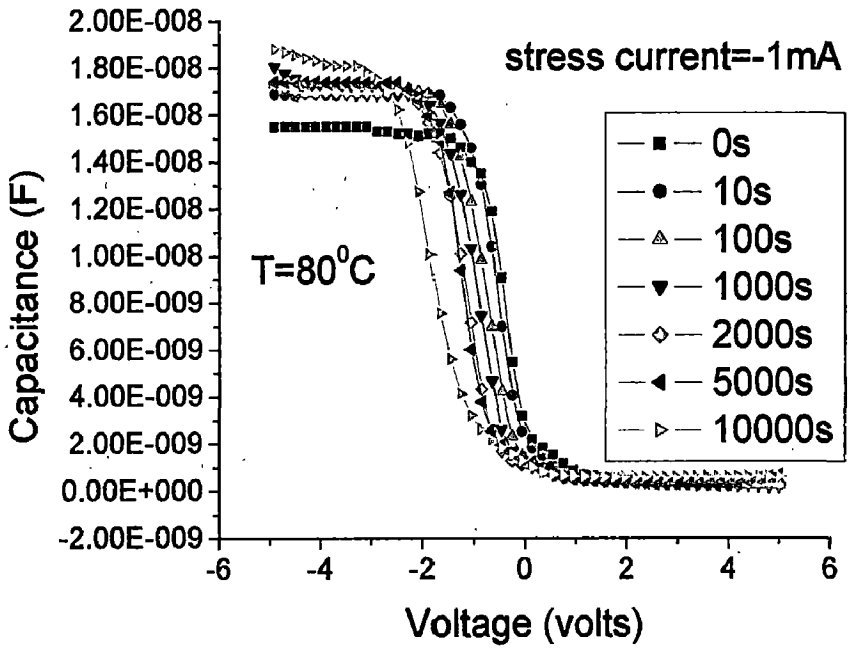


***Figure 5.2** Variation for high frequency (100 kHz) C-V curves of Al/ZrO_2/HfO_2/p-Si MIS Capacitor with a CCS of -1mA at 80°C.*

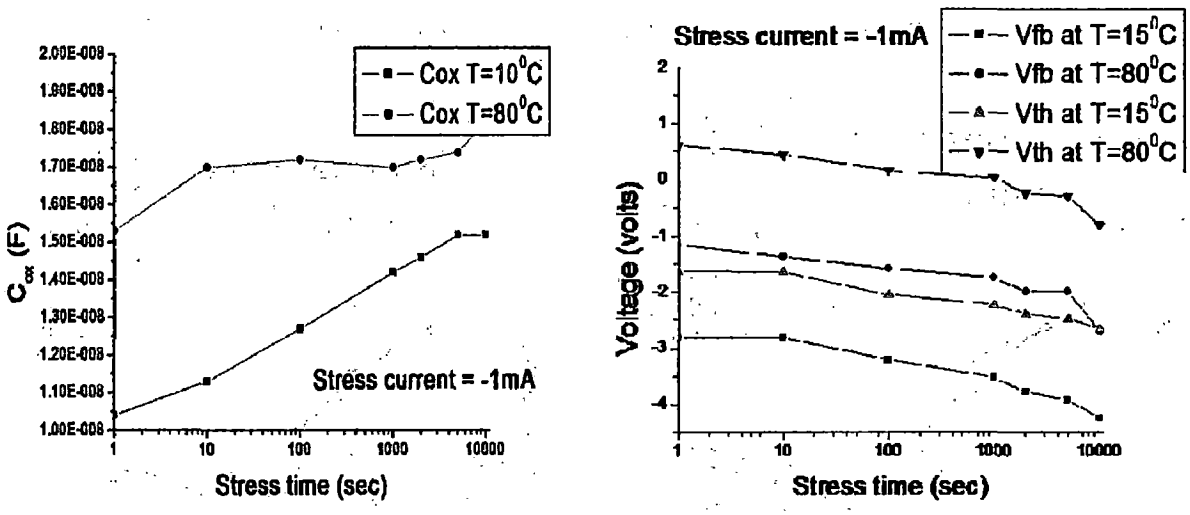
Figure 5.2 shows C-V characteristics of Al/ZrO_2/HfO_2/p-Si MIS capacitor under constant current stress of 1mA in accusation region measured at 80°C temperature. From Figure it is identified that increase in stress time results curves are shifting in negative direction, which indicates increase in fixed oxide charges. Slope of C-V curve observed at midgap capacitance decreases due to thermal agitated constant current stress which signifies increase in interface trap charges. The increase in interface trap charges acts as a capping layer which results increase in Oxide capacitance (C_{ox}). A shift in flat band voltage in negative direction is studied.

Figure 5.3 (a) shows variation of fixed oxide charge density with stress time for constant current stress. At low temperature fixed oxide charge density increases with progressing of constant current stress and in case of high temperature CCS at longer stress function, the rate of increase is comparatively less . It points out increase fixed oxide charges, generated due to constant current stress, move towards interface results in increase of interface trap density pointed by increase in dispersion of C-V curves (fig 5.2) and reduces the oxide capacitance C_{ox} (from Figure 5.3(c)). Because induced interface traps acts as capping layer and increases the dielectric capacitance of devices.

Figure 5.3.(b) shows constant current stress at low temperature results in decrease of flatband voltage and threshold voltage effectively compared to thermal aided constant current stress. Where as in case of temperature aided constant current stress increase traps near the interface. The difference between flat band voltage and threshold voltage is higher compared than that of low temperature constant current stress and it increases with stress time.

From the Figure 5.3 it is observed that the capacitor has large amount of fixed oxide charges and they are increasing rapidly with increase in stress. Along with the interface of HfO2 with silicon the interface layer between both ZrO_2 and HfO_2 acts as sources for fixed oxide charges. And the number of oxide charge carriers increasing rapidly with increase in stress.

Study for SILCs is performed by studying the variation in leakage current characteristics with stress time. Figure 5.4.(a) shows the effect of constant current stress of 1mA in accumulation region at room temperature. Primarily there are 2 major conduction mechanisms are noticed which are pool Frenkel in case of substrate injection and at low electric fields of metal gate injection. At high eclectic fields of metal gate injection signifies Schottky emission. This mechanism can be explained by the presence of large number of traps near the interface of dielectric and substrate. In case of metal gate injection primarily leakage current is dominant by defect oriented and at high electric field Schottky emission is dominant.



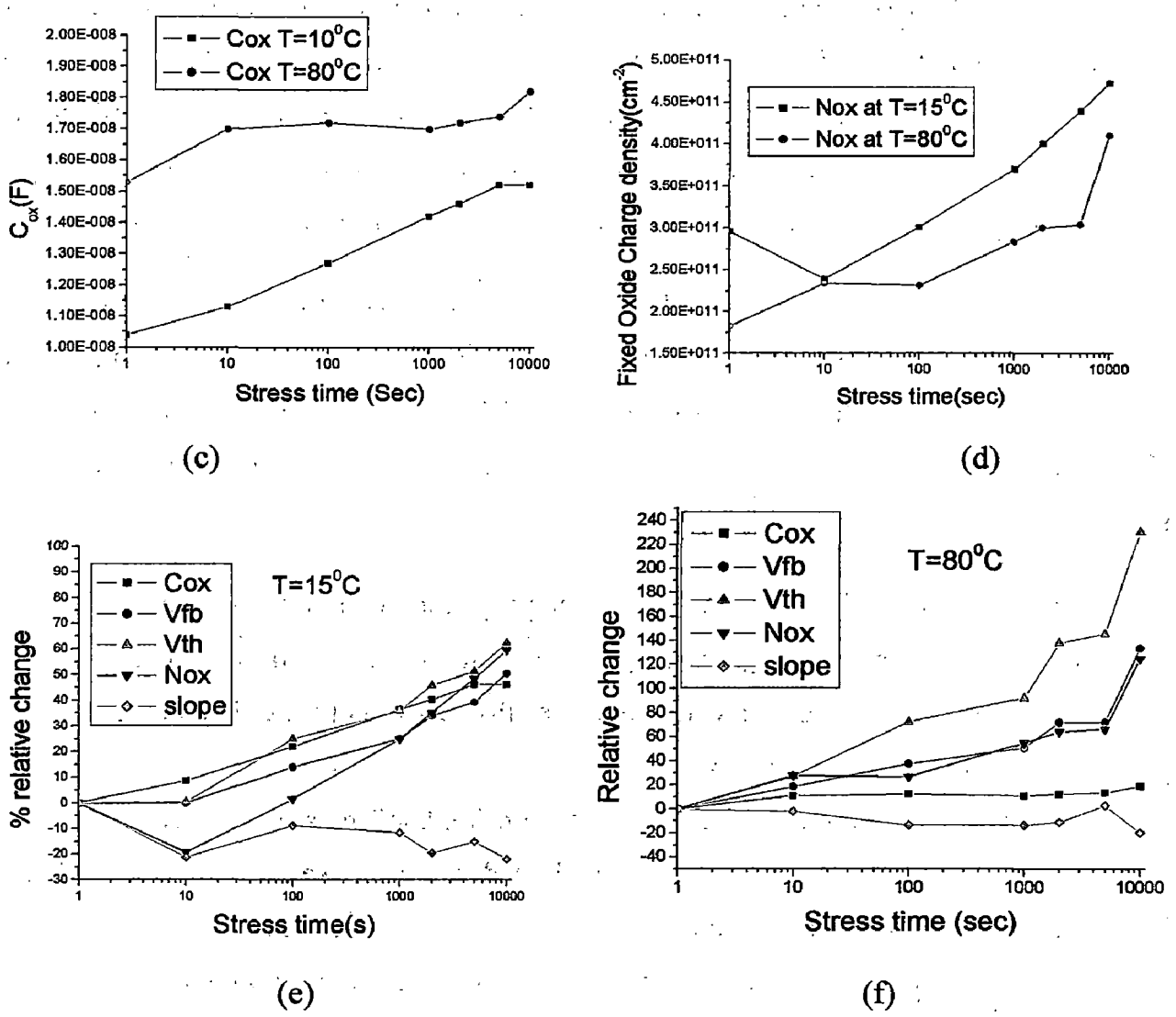


Figure 5.3 *Study of CCS(-1mA) on Al/ZrO_2/HfO_2/p-Si (a) fixed oxide charge N_{ox} (b) flatband V_{fb}, threshold voltage V_{th} (c) Oxide Capacitance C_{ox} (d) slope at 15°C and 80°C and relative percentage change in C_{ox}, V_{fb}, V_{th} and slope for (e)measurement at 15°C (f)measurement at 80°C.*

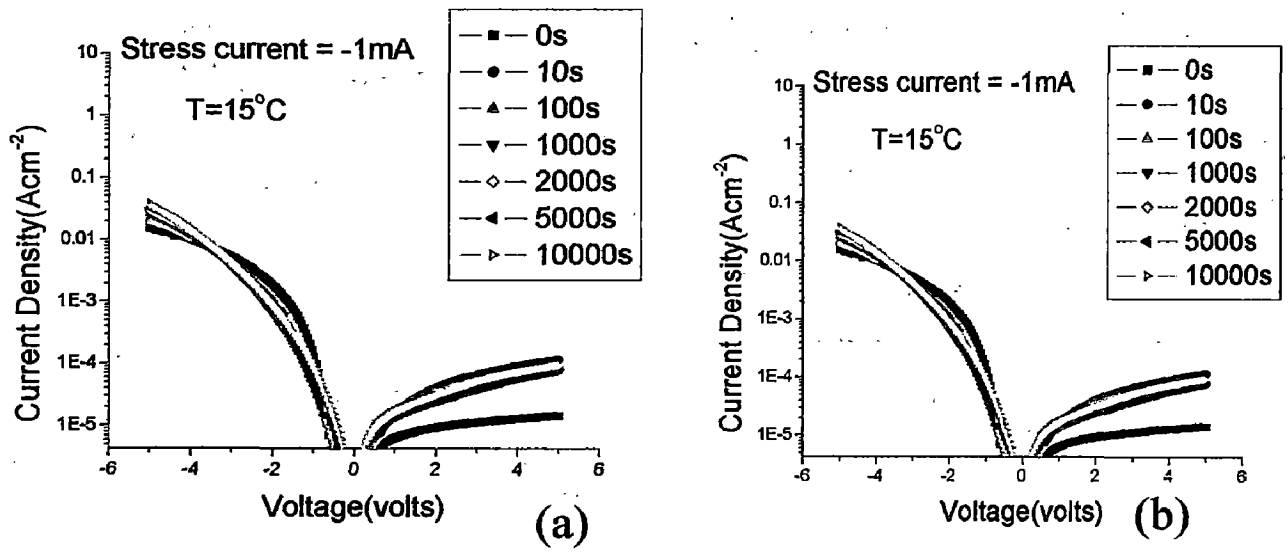


Figure 5.4 *variations of leakage current characteristics in Al/ZrO_2/HfO_2/p-Si capacitor with CCS (-1mA applied at metal gate) (a) at 15°C (b) at 80°C.*

Figure 5.4(b) shows the deviation of leakage currents with respect to CCS of 1mA at 80^0C. It points out that for substrate injection of electron (application of positive voltage); leakage current is mainly dominant by Schottky conduction. Due to generation of large number of fixed and/or interface traps inside the bulk, dielectric and substrate interface. The critical field shifts towards right side indicating the decrease in current due to scattering effect of induced fixed oxide charges.

Figure 5.5 shows the variation of leakage current at flat band voltage with increase in stress time of both CCS cases. It indicates that leakage current increase exponentially with stress time however the electric field required to provide accumulation is also increasing with stress. Due to decrement in effective fixed oxides at 80^0C the leakage current occurring at particular electric field is reduced with temperature.

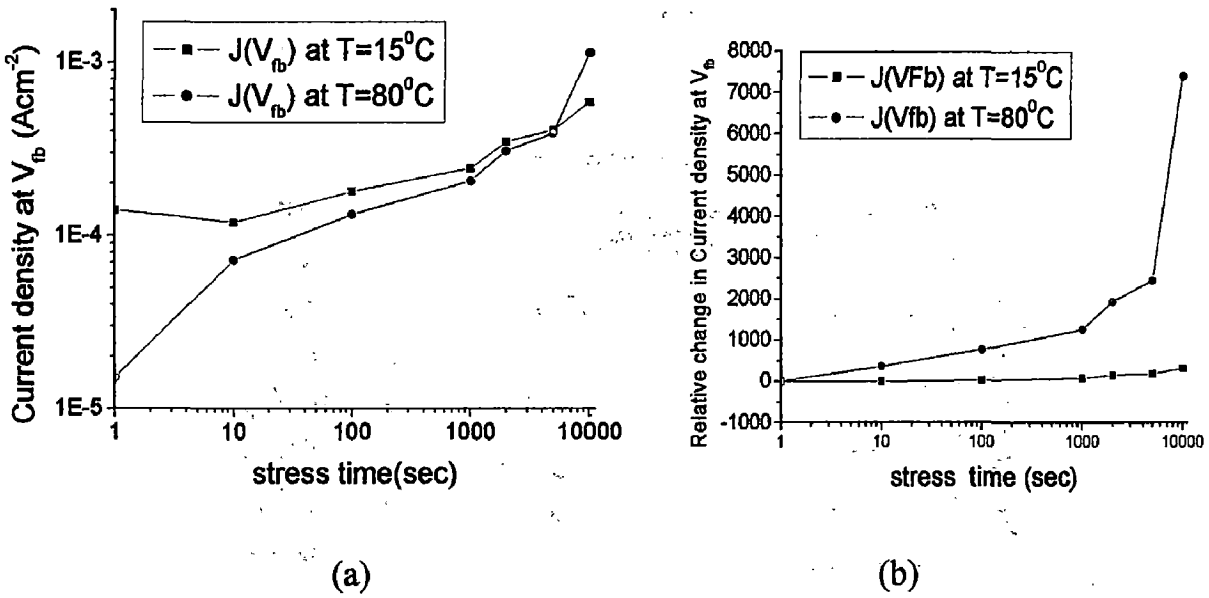


Figure 5.5 Variation of leakage (a) current density(Acm^{-2}) (b) relative change in current density at flat band voltage with stress time for Al/ZrO_2/HfO_2/p-Si at fixed CCS and thermal accelerated CCS at 80^0C.

5.3.2 Study of constant current stress on Al/HfO_2/ZrO_2/p-Si MIS Capacitor

Figure 5.6 shows the deviation in high frequency (100 kHz) C-V curves by the application of constant current stress of 1mA in accumulation region at room temperature. It clearly shows increase in stress time results in generation of positive oxide charge with the progression of stress. The variation in oxide capacitance is small and constant which is independent of stress time. It clearly shows less content of interface trap generation. The increase in oxide trap charges is increasing at high rate with stress.

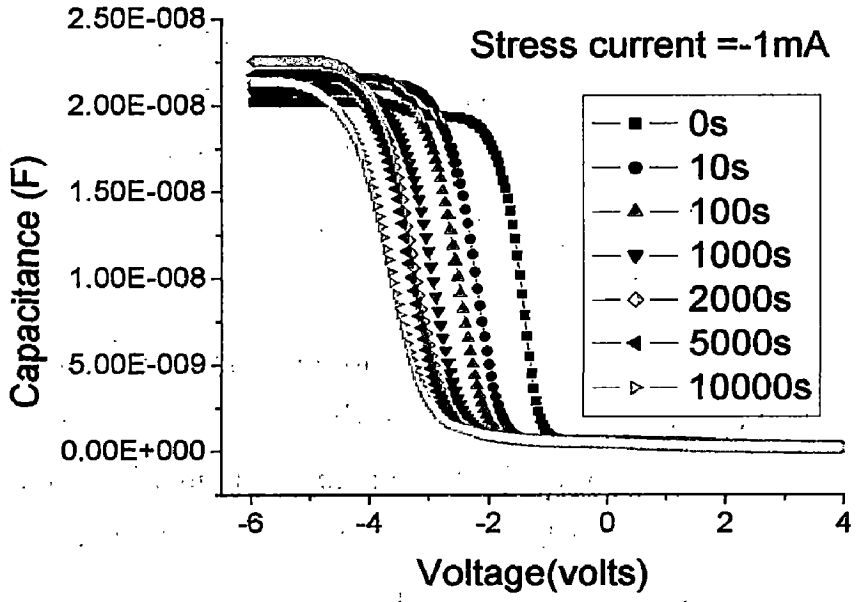


***Figure 5.6** Capacitance (F) - Voltage (V) plots for Al/HfO_2/ZrO_2/p-Si MIS structure under CCS at -1mA at temperature 15^{0}C.*

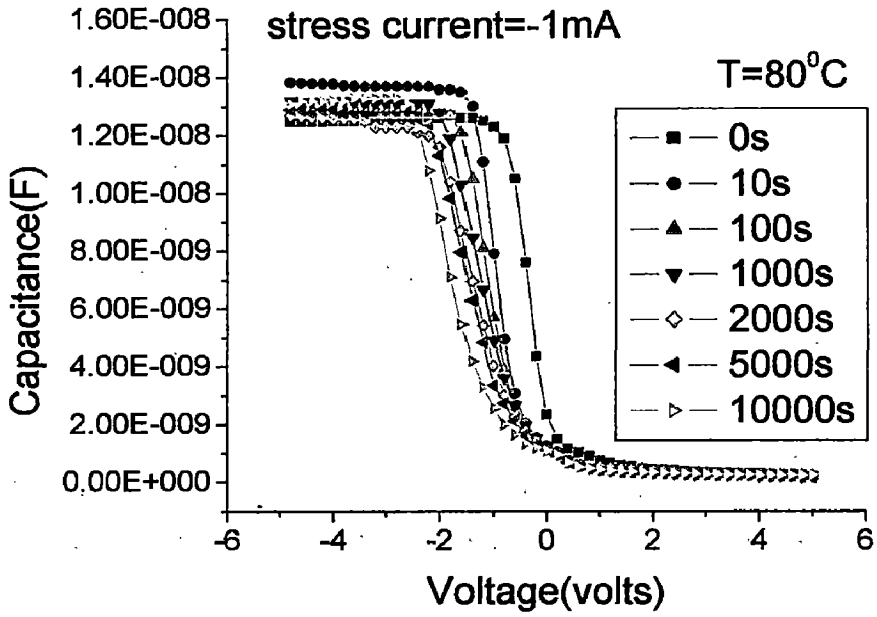
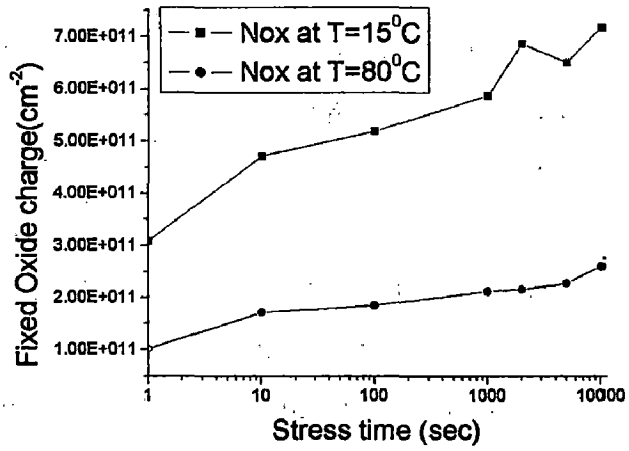
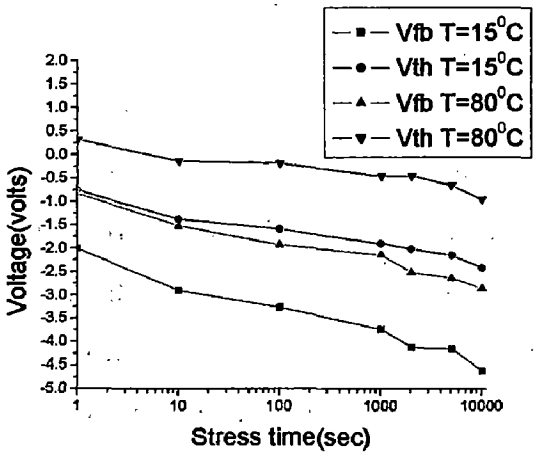


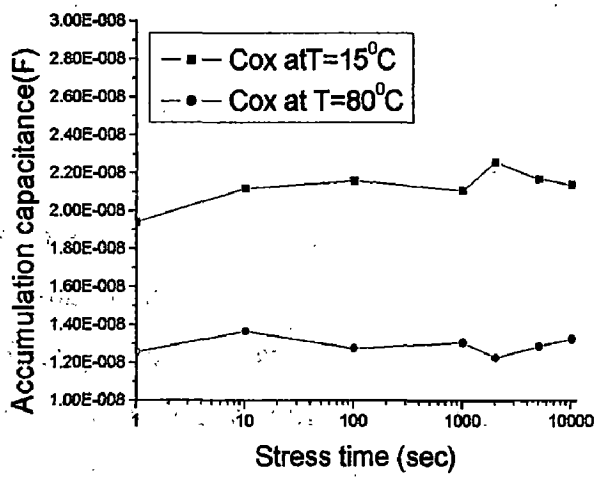
***Figure 5.7** Variation in Capacitance (F)-Voltage (V) curves of Al/HfO_2/ZrO_2/p-Si MIS structures for CCS at -1mAfrom metal electrode at 80^{0}C.*



(a)



(b)



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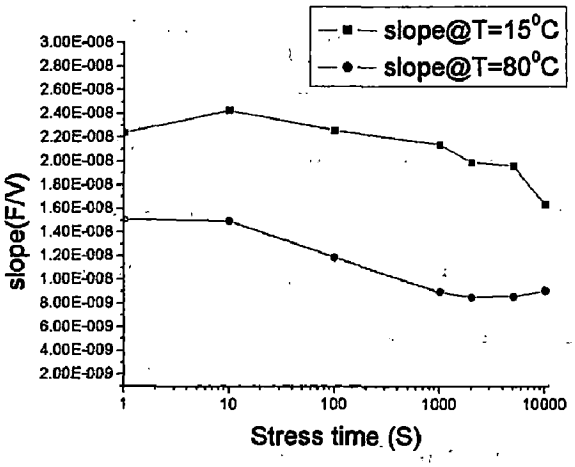
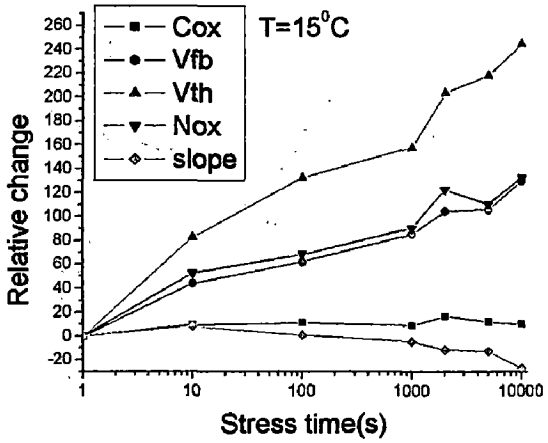
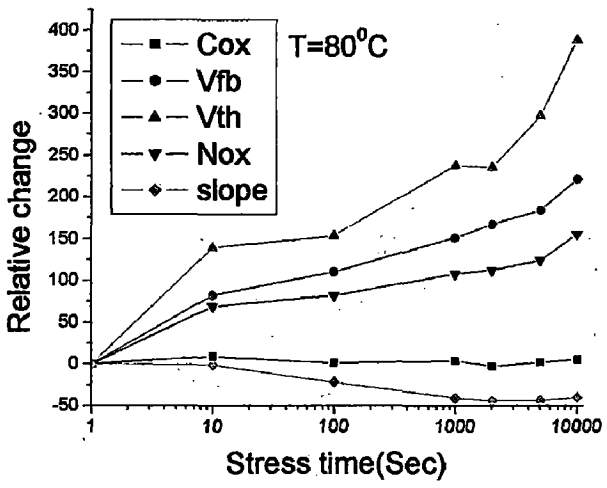


(d)



(e)



(f)

***Figure 5.8** Variation in (a) fixed oxide charge N_{ox} (b) flat band V_{fb}, threshold voltage V_{th} (c) Oxide Capacitance C_{ox} (d) slope at 15°C and 80°C and relative percentage change in C_{ox}, V_{fb}, V_{th} and slope for CCS=-1mA at (e) 15°C (f) 80°C of Al/HfO_2/ZrO_2/p-Si MIS from metal gate.*

Figure 5.7 shows high frequency (100 kHz) C-V curves for application of thermal aided CCS at -1mA at 80^0C. It is identified that accumulation capacitance Cox is increasing with the progression of stress. Capacitance curves are shifting in negative direction. Spreading of C-V curves indicate the increase in interface trap charges at 80^0C. Figure 5.8 (a) shows variation of effective fixed oxide charge density with stress time. At room temperature the number of oxide charges in dielectric layer increases rapidly by the application of CCS as shown in figure. In case of thermal aided CCS study the effective number of fixed oxide charges is less almost decreased to half. But from 5.8(b) the shift in flat band voltage and threshold is high in both cases. And the difference between those voltages increases with stress. This can also be observed form Figure 5.8(c) indicating that increase in effective number of interface traps. Figure 5.8(c) shows variation of accumulation capacitance with increase in stress time. It signifies increase in interface trap charges with increase in measurement temperature and CCS. In Figure 5.8 (d) maximum slope of C-V curve is calculated for both the case of CCS at room temperature CCS at 80^0C. With progress in stress time the slope of CV curve is decreased for both the cases and its values is lesser for the measurement at room temperature. Figure 5.8(e) and 5.8(f) shows variations relative % change in C_{ox}, V_{fb}, V_{th}, N_{ox} and slope of C-V curves. From the curves it is identified that degradation is mainly aided by shift in shift in fixed oxide charge traps and interface traps. Degradation in temperature aided CCS is drawn by the interfacing trap charges. As well as in the case of low temperature CCS it is drawn by fixed oxide charge degradation.

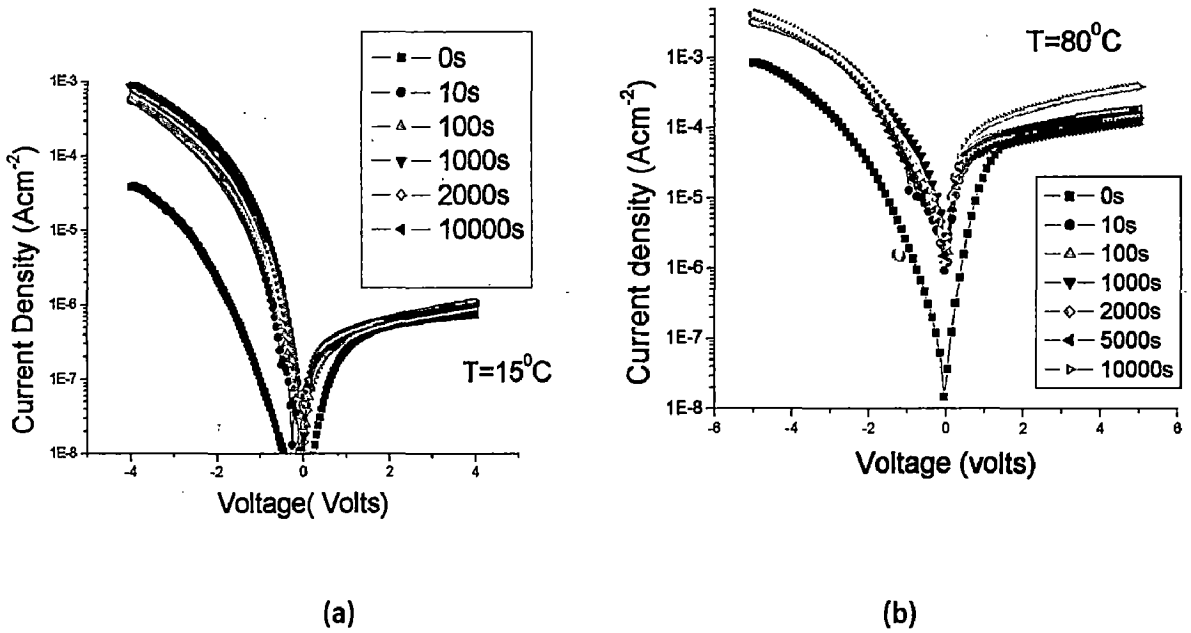
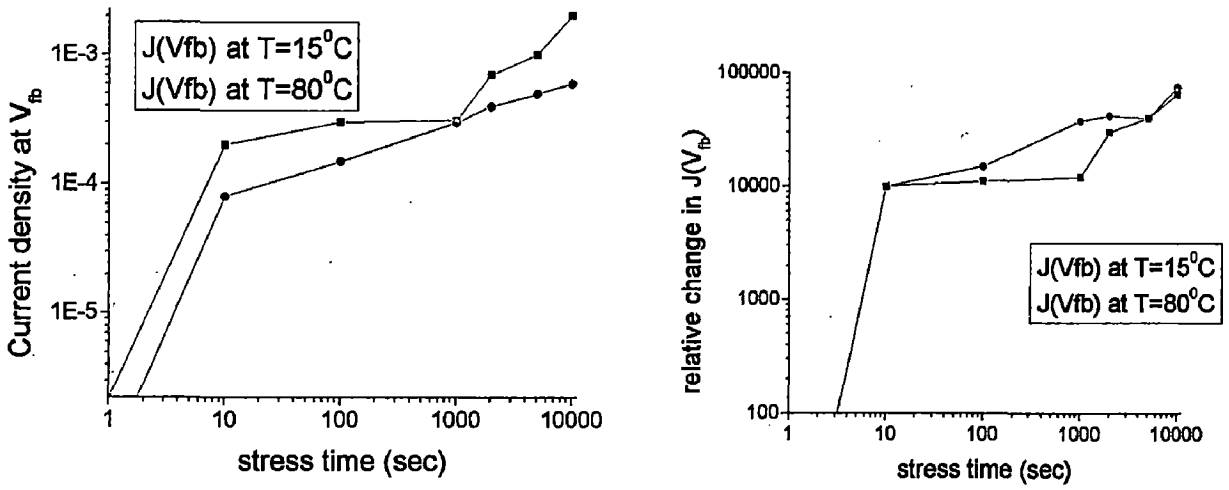


Figure 5.9: *Deviation in leakage current characteristics for Al/HfO_2/ZrO_2/p-Si MIS capacitor with temperature aided CCS of -1mA (a) Measurement at 15^0C (b) Measurement at 80^0C.*



(a) (b)

***Figure 5.10** Variation of leakage current density at flat band voltage with stress time for Al/HfO_2/ZrO_2/p-Si at fixed CCS of -1mA from metal gate at (a) T=15°C (b) T=80°C.*

Figure 5.9 shows discrepancy in leakage current characteristics with respect to CCS. From the curves it is identified that at low electric fields leakage current is mainly dominant by Pool-Frenkel bulk limited mechanism and at large electric fields it is dominant by Schottky emission. For CCS very short pulse of constant current within 10 sec creates defects which can be sufficient for trapping/detrapping of charges in severe. Further increase in stress time shows increase in stress time and then after that no drastic change in curves is observed. But the critical field where the carriers with which a leakage current is changed from one mechanism to another is increasing with increasing in electric field. In case of high temperature stress no leakage current same effect is observed.

The value of leakage current is higher in the case of electron injection from substrate compared to injection from metal gate. From the Figure 5.9(b) in case of substrate injection at large electric fields shows shift in leakage characteristics. The physical mechanism for this effect is not fully understood.

Figure 5.10 shows the percentage increase in current at flat band voltage. Because of adding new fixed oxide charges flat band voltage is increasing in such a way that. The electric field across the dielectric is to overcome the effect of fixed oxide field charges. Because of increase in electric field the leakage current across the dielectric increases drastically.

By comparing the Figures of 5.10 we identified that though the leakage current inside is very low because of stress apply it increases drastically. However it is identified that degradation due to the effect of CCS and temperature aided CCS is less in case of $Al/ZrO_2/p$-Si MIS capacitors compared to HfO_2 based MIS capacitors under same fabrication conditions.

5.4 Conclusions

In this chapter reliability studies on $Al/ZrO_2/HfO_2/p$-Si and $Al/HfO_2/ZrO_2/p$-Si are explored. A constant current of -1mA is applied to the gate metal. Periodically measurement of leakage current and capacitance are performed to observe the discrepancy in the curves. From the reliability characteristics following conclusions are made

- Firstly Multi layer gate structures of $Al/ZrO_2/HfO_2/p$-Si and $Al/ZrO_2/HfO_2/p$-Si are fabricated using electrical sputtering. The effective dielectric constant of those capacitors is measured from high frequency C-V characteristics as 15.5 ± 0.4 and 21 ± 0.5.
- By the application of CCS at room temperature for both capacitors more or less, following effects are studied. Those are increase in fixed oxide charge density, negative shift in flat band voltage and threshold voltage, increase in discrepancy of curves and increase in critical electric field Along with it accumulation charge is increased with increase in stress. .
- In case of temperature aided stress the devices degraded rapidly.
- From the leakage current measurements, it is identified that, the electric field inside the dielectric is so high such that sudden increase in current is reported below 10 seconds. After that increase in leakage current is very less. After that is leakage current is mainly dominated by Schottky emission which is controlled by interface control mechanism, but not by bulk dependent mechanism.
- From high frequency C-V characteristics huge shift in threshold voltage is reported Due to presence of large electric field and non-ideal interface between two amorphous HfO_2 and ZrO_2 layers.

5.5 References

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[6] Znag H, Solanki R, and Roberts B, "High Permittivity Thin Films Nano Laminates", vol.87, Issue 4, 2009.

[7] Conley J. F., "Methods to Deposit a Stacked High", US Patent 6,686,212, 2004.

CHAPTER-6

CONCLUSION

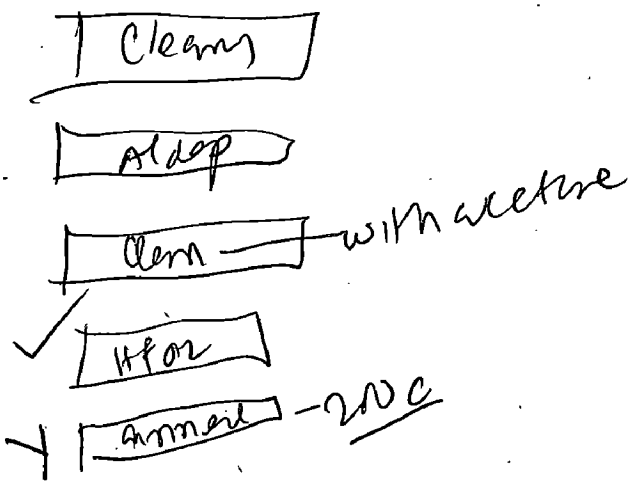
High-k Metal Insulator Semiconductor Capacitors Al/HfO_2/p-Si, Al/ZrO_2/p-Si, Al/HfO_2/ZrO_2/p-Si and Al/ZrO_2/HfO_2/p-Si are fabricated on boron doped silicon [100] substrates using Reactive RF Magnetron sputtering system. Amount of oxygen used in during deposition is varied to determine their effect on leakage current and capacitance voltage characteristics. X-Ray diffraction is used for micro structural characterization.

MIS Capacitors Al/HfO_2/p-Si and Al/ZrO_2/p-Si are annealed in presence of Nitrogen, at different temperatures. From the analysis using XRD on both the deposited HfO_2 and ZrO_2 films shows amorphous structure after deposition using sputtering and at low temperature annealing. Poly-crystalline nature in monoclinic structure is achieved in case of HfO_2 based structures. In case of ZrO_2 based devices no peak related to polycrystalline nature is reported. Temperature dependent leakage current and capacitance voltage measurements are allowed for extraction of dielectric constant and amount of fixed oxide charge present inside the dielectric. From the C-V measurements dielectric constants of 13 and 14.2 are reported in case of HfO_2 based MIS capacitors which are deposited at low oxygen and high oxygen contents. In case of ZrO_2 based structures dielectric constants of 14 and 15.8 are reported for ZrO_2 based structures for low and high oxygen contents. From electrical measurements it is identified that increase in annealing reduces the amount of fixed oxide charges present inside the dielectrics. Increase in measurement temperature results increase in interface charges. It also effects in enhancement of dielectric constant with annealing temperature due to readjustment of atoms. However increase in polycrystalline nature decreases the dielectric constant. This effect is reported in case of HfO_2 after annealing at 350^0C. From the leakage measurements mainly pool Frenkel and Schottky mechanisms are reported for both ZrO_2 and HfO_2 based structures. Increase in annealing temperature reduces the critical electric field which is observed by temperature dependent leakage measurements.

Based on the previous study fabrication parameters are adjusted and new structures of Al/HfO_2/p-Si and Al/ZrO_2/p-Si are fabricated. Dielectric constants of 22 and 19.5 are

reported in case of HfO_2 and ZrO_2 based structures respectively. Electrical reliability of $Al/HfO_2/p\text{-}Si$ and $Al/ZrO_2/p\text{-}Si$ are studied by effect of temperature dependent constant current stress on leakage current and C-V measurements. Increase in stress time results increase in positive oxide charge inside the dielectric. In case of high temperature CCS decrease in oxide capacitance is reported for both structures. From leakage measurements increase in critical electric field is noticed due to increase in scattering effect of induced oxides inside dielectric. Stress induced leakage currents are reported to be less indicating better reliability of $Al/ZrO_2/p\text{-}Si$.

Based on the previous study, MIS capacitors with laminated structures of HfO_2 and ZrO_2 are fabricated. Electrical reliability of these structures is exerted using effect of temperature dependent CCS on leakage current and fabricated structures. From C-V characteristics Dielectric constants of 20 and 15.5 are reported for $Al/HfO_2/ZrO_2/p\text{-}Si$ and $Al/ZrO_2/HfO_2/p\text{-}Si$ interface. Though there have a high dielectric constant, a huge amount of fixed oxide charge is reported due to the presence of interface layer between ZrO_2 and HfO_2 along with interface layer between HfO_2(or ZrO_2) and silicon. In case of Temperature aided CCS rapid degradation in leakage characteristics are reported. From the leakage current analysis it is reported that the critical electric field across the dielectric increases with increase in stress time.



APPENDIX A
WAFER CLEANING

A sequence of chemistries is typically used to clean silicon wafers. Fallowing steps are allowed to clean the silicon wafer from organic, metal impurities and native oxide.

Prior to the experiment circular disc wafer is cut down into pieces in the size of 1cm×1cm by using graphite cutter (Figure A1 (a)). General procedure that is used for dissertation leaning throughout this s contains following steps:

- Dust particle removal: A clean filtered N_2 gas with high flow rate is used to blow away dust particles. It has done for 2-3 minutes at room temperature.
- General clean: General cleaning is accomplished by using acetone at room temperature. It will remove organic and plastic impurities. 2-10 minutes of clean is recommended. Strong rinse in Distilled Ionized (D I) water is requiring after this step.
- Particle removal: An ultra sonic clean (Figure A1 (b)) in an acetone is used, It will remove certain organic and metal surface contamination. 2-10 minute clean is recommended. Strong rinse in DI water is required after this cleaning step.
- Oxide Removal: A 60-120 seconds dip in 2:98 HF: DI water will remove the native oxide layer and any contamination from the wafer surface. HF is extremely dangerous and must be handled with great care. It also shows the cursive nature with glass, so Teflon beakers and Teflon twisers are used. Strong rinse in DI water is required after this cleaning step.
- Heating: Wafers are heated to 80^0C using oven (Figure A.1.b) to remove the content of water on silicon. This process should be carried out for 5-10 minutes.

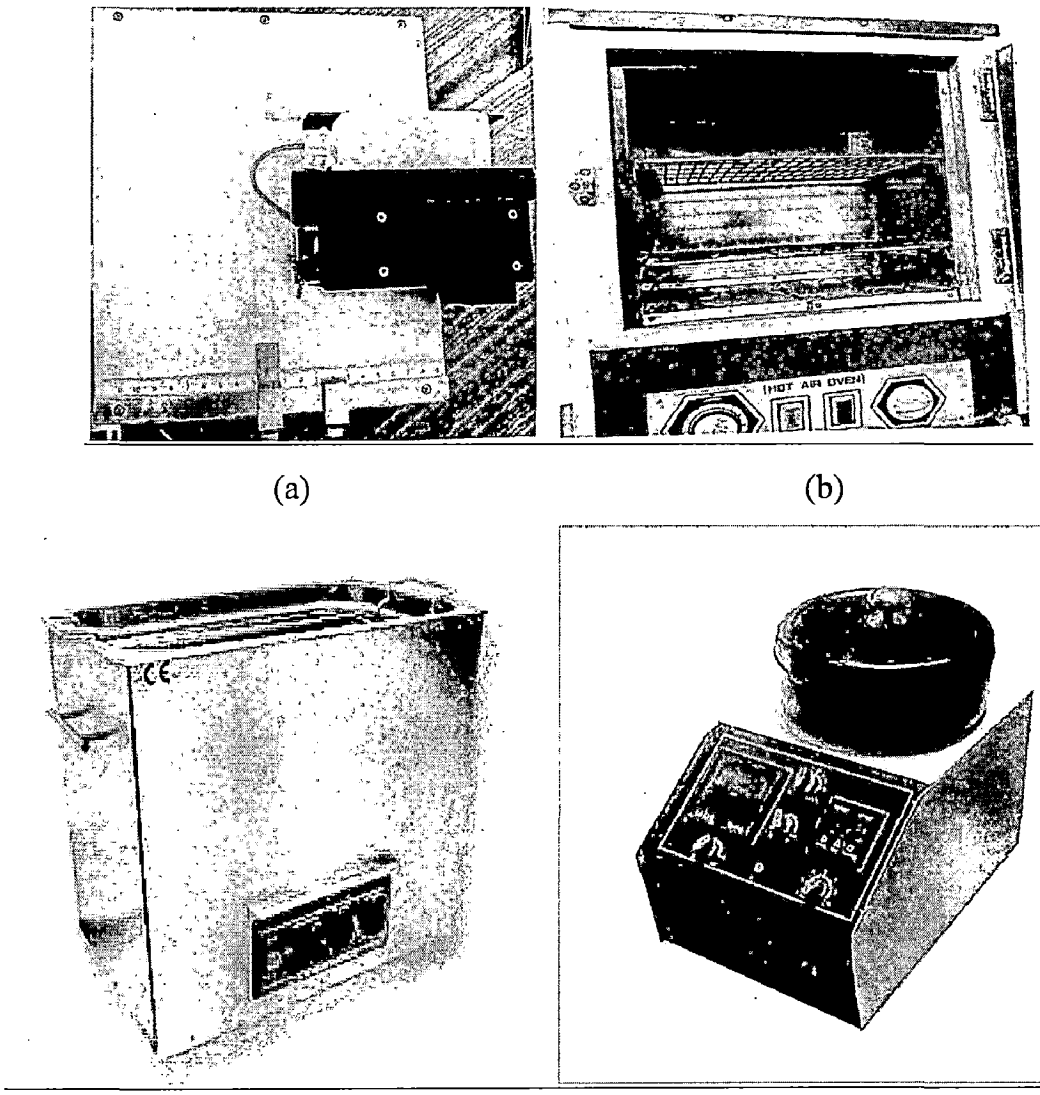


Figure A.1 Equipments used in out lab for cleaning (a) Wafer cutter (b) Heater (c) Ultra sonic cleaner (d) Spin coater

A2. References

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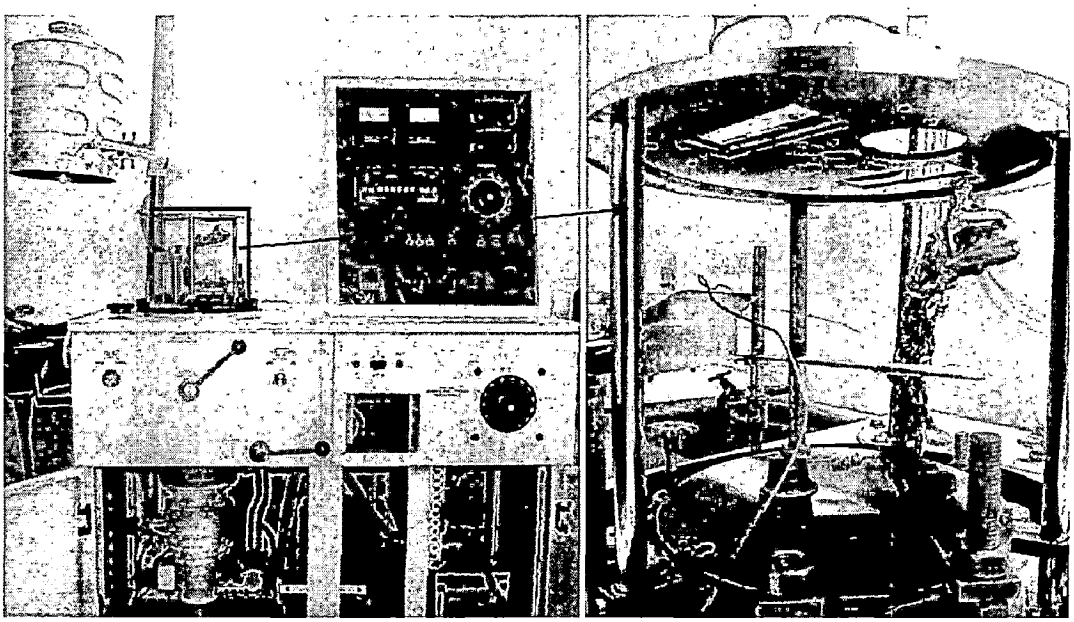
APENDIX B

DEPOSITION OF METALS USING EVAPORATION BY VACUM COATING UNIT

Deposition of metals through evaporation technique carried out by following steps for physical vacuum coating system. The physical mechanism is described in chapter 2.2. The Vacuum coating unit described in this thesis is shown in Figure B.1



(a) (b)

Figure B.1 (a) Evaporation equipment used in our lab (b) Evaporation chamber

The apparatus consists of a glass cylinder vacuum chamber with a rotary vacuum pump, an oil vapor diffusion pump and pressure gauge. An evaporation source is mounted within the glass chamber. The source consists of twisted tungsten wires connected to a 60A current source at one end and the other end connected to earth. A small piece of aluminium wire is wound around the tungsten, which becomes very hot when the current source is turned on. Since tungsten has a melting point of 3410^0C and aluminium has a boiling point of 2467^0C at atmospheric pressure, so the aluminium will boil before the tungsten begins to

melt (in fact both these temperatures are reduced at low pressure. our system operating pressure is 10^{-5} mbar, thus Al begins to evaporate at 900^0C and violently evaporates at 1200^0C. Aluminium vapor quickly fills the space because low pressure allows less collision of molecules and condensate on any cold surface forming a metallic film. The procedure that we follow for deposition of metals is described here.

B.1 Starting the vacuum system

1. The diffusion pump takes about 15 minutes to warm up so it is a good idea to do this early.
2. Before we start, check with a demonstrator that the water flow is turned on. The water provides essential cooling for the diffusion pump.
3. Switch on the main power and the coater unit on by one.
4. Switch on the rotary pump ("pumps" switch to "rotary on").
5. Open the backing valve to the diffusion pump ("diffusion pump backing valve" switch to "open").
6. Switch on the diffusion pump ("pumps" switch to "diffusion pump").

There should now be four red lights showing on the circuit diagram on the top panel of the unit (rotary pump, pump valve, backing valve and diffusion pump) and also the "power on" light at top left. If any other lights are observed ask a demonstrator to check the system. After 15 minutes the diffusion pump should be warmed up. The vacuum system will then be on stand-by for pumping the chamber. In the mean time the silicon substrates can be prepared.

B.2 Substrate preparation

Thin film growth and adhesion is fundamentally related to the substrate surface conditions. It is therefore crucial to thoroughly clean the substrate before the deposition process. In industry this is often done by plasma etching impurities from the surface. Silicon substrates are cleaned properly with nitrogen gas, acetone, ultrasonic clean and etching with dilute HF. The different steps followed in cleaning process are described in Appendix A.

1. Clean two glass microscope slides thoroughly with acetone and tissue and allow drying.

2. Now remove the stainless-steel lid of the vacuum chamber. This can be difficult and it is important not to damage the glass cylinder. This is done by holding the sides of the lid and pulling vertically upward. When the lid is at least 5cms clear of the top of the glass cylinder, rotate the lid around to the left and allow it to slide back down the support post.
3. The alligator clips and crystal monitor may still be inside the chamber from a previous experiment. For reference, make a quick diagram of the arrangement in our logbook, so we will know how to reinstall them in part A.5. Reach inside the cylinder and remove them both by loosening the blocks from the posts. The crystal monitor is unplugged by gently pulling the plug out of its socket at the base of the chamber. Place these parts aside until later.
4. Using some tissue paper "moistened" with acetone, clean the inside of the glass vacuum chamber on the side closest to we and the rear side nearest the window, so we can see what is going on inside the chamber. If we want to clean the glass plate thoroughly unscrew the screws using alignment keys with proper and equal force should be applied on all screws. Otherwise due to unequal pressure glass plate will break down.
5. Aluminium oxidises quickly and is chemically un-reactive, but it is still good practice to avoid inhalation of metal dust.
6. Undo the evaporation holder earth lead.
7. Loosen the evaporation holder at the support post and slide it up and remove it from the chamber.
8. Twist a 3 cm piece of aluminium wire around the tungsten wire. If the tungsten wire is broken it will need to be replaced. The tungsten becomes thermally embrittled and susceptible to breakage after several heating and cooling cycles. Take care not to damage the ceramic insulator if we need to replace the tungsten wire.
9. Place the cleaned shadow mask and glass bottom and top of silicon wafer in the centre of the circular substrate holder, tight the mask screw such that the mask structure can't be disturbed.
10. Return the evaporation unit to the chamber. We want to connect the evaporation unit between the earth post and either post 2 or 3. If any of the posts is in the wrong place then simply unscrew it and move it.
11. Now tighten the tungsten evaporation unit in place about 10 cm above the glass slides.

12. Replace the lid of the vacuum chamber.

B.3 Chamber evacuation

The chamber is now ready to be evacuated. The pumps should by now be warm enough to operate.

1. Close the diffusion pump backing valve. This should not be left closed for more than about ten minutes.
2. Check that the black air inlet valve at the bottom of the panel is screwed shut and that the gas inlet switch beside it is off.
3. Open the chamber roughing valve and observe the pressure. The pressure should begin to reduce after about 30 seconds. If not, check the lid is properly down, or asks a demonstrator to help.
4. When the gauge shows a pressure of 1×10^{-1} mbar or less, close the roughing valve.
5. Open the backing valve, returning the vacuum system to stand-by.
6. Open Chamber Isolation Valve. It is important that the pressure is below 1×10^{-1} mbar when the valve is opened.
7. When the pressure in the chamber drops to below 1×10^{-4} mbar the system is ready to begin the evaporation process. We will need to change the detector on the pressure gauge to see the pressure below 1×10^{-3} mbar.

B.4 Evaporative deposition of aluminium electrodes

Evaporation is achieved by resistively heating the tungsten electrode. If the current through the tungsten is too high the tungsten will break and we will have to start again after replacing it.

1. Check that the "Source A Control" knob is set to zero.
2. Switch "Source A Select" to "Cont. on". The source A light should illuminate. If not then we probably connected to the "Source B" post. In this case go to the "Source B Control" knob.
3. Turn the Heater to LT mode.
4. Turn the control knob until the tungsten filament just begins to glow red after a few seconds. If this process is not observed or slow at 30 A, the current can be increased

slightly however the control knob should not be turned above 50 A. If the filament has been used many times it will become brittle and may break in which case it will need to be replaced. While we increase the current we will observe decrease in pressure indicating the presence of impurities on tungsten and they are evaporating at less temperature compared to aluminium. If the vacuum inside the chamber is less than 1×10^{-4} mbar then stop the heating of tungsten and increase the vacuum inside chamber by controlling diffusion valve.

5. After a few seconds of the tungsten glowing we should observe the aluminium wire begins to melt and evaporate. When the inside of the glass tube turns silver/black so that the evaporation unit is no longer visible the current control knob should be returned to zero.
6. Switch off the source ("Source A select" to "off").
7. Close the chamber isolation valve, which returns the vacuum system to stand-by (four red lights).

The chamber is now ready to be vented. It is important that the chamber is isolated from the pumping system before air is admitted or the diffusion pump may be damaged. Double check that the chamber isolation valve light is NOT on. The air inlet valve is located on the bottom panel of the instrument. Slowly open the valve to admit air into the chamber. The evaporation unit will be VERY HOT for a number of minutes after the deposition process. Wait at least 10 minutes before we open the chamber lid, and then remove the evaporation unit, the glass tube and the glass slides.

We should now have our substrate is deposited with aluminium contacts according to the mask that we have chosen.

B.5 References

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APPENDIX C

THIN FILM DEPOSITION USING REACTIVE MAGNETRON SPUTTERING

Deposition of Materials using Reactive Magnetron Sputtering is carried out by four major steps

1. Starting up the system
2. Performing Deposition
3. Post deposition insitu annealing
4. Stopping the sputtering system

Each step requires complete understanding and should be handled with so carefully. It is suggestible to do experiment in the presence of lab associate. The sputtering system used in this thesis is shown in Figure C1.

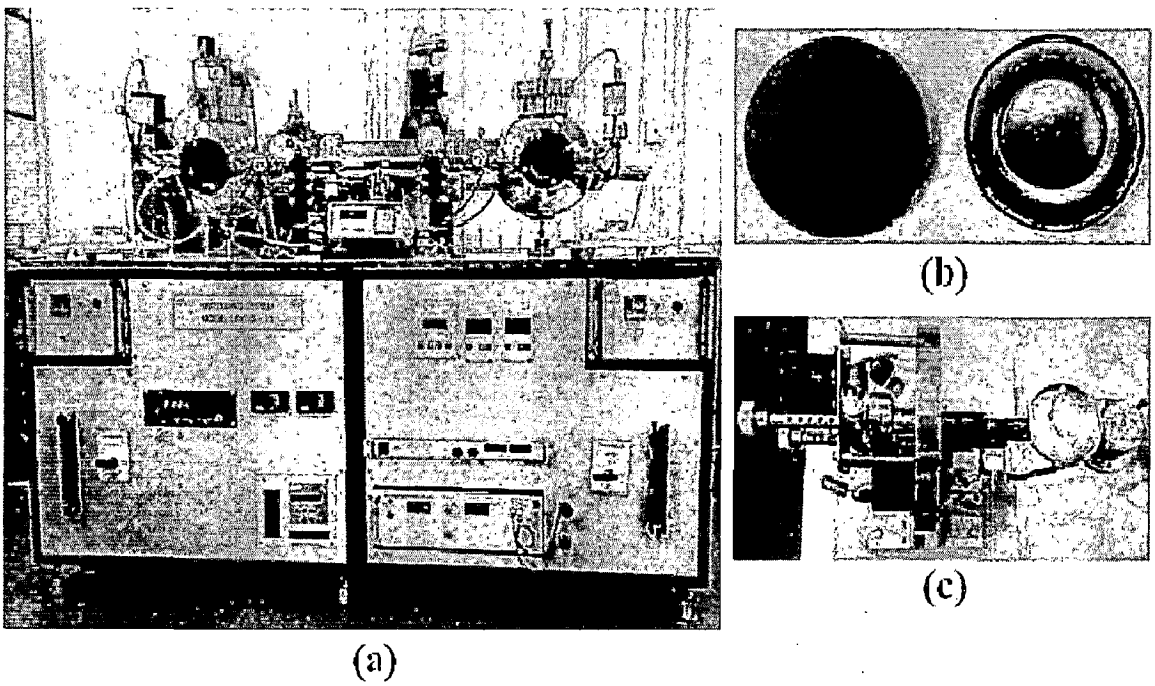


Figure C.1 *(a) DC/RF magnetron sputtering unit set up in our nano science lab.*
(b) New & used sputtering target.
(c) Substrate holder/heater.

C.1. Starting up the sputtering system

1. Release the vacuum inside the chamber: To do this relapse gas valve connected to sputtering chamber. Then after open the gate valve which connects the vacuum pump system to chamber.

2. Cleaning the chamber: Open the chamber from its face and clean the chamber with acetone, N_2 gas and tissue paper. This will improves the quality of our deposition by reducing contamination of other materials.

3 Replacing the target: Remove the target gun from system and place it on target stand. Gently remove the target gun face shielding and unscrew the nuts to remove the previous target material .Select the target material that we want does sputter. Before using the target, clean it with acetone and N_2 gas. Place the previous target material in corresponding named container. Clean the target shielding, screws and face of target gun with acetone and scrubber. Fix the face and shutter tightly in such a way that the target shielding will not have a physical contact (electrically) with the target material. Check the continuity test with multimeter between pins of target power supply. If it is showing short circuit, then readjust the target shielding and recheck it. Place the target gun inside the chamber and recheck the continuity test. While placing, the O-ring should not be displaced from its position. Any small adjustments in O-ring relapses air inside evacuation. Adjust the distance between target and substrate by our requirement.

4 Cleaning of Si Substrates: Si wafers are cleaned thoroughly with N_2 gas, acetone, propane, ultrasonic cleaning and heater. Etch the substrates with dilute hydro fluoric acid (2%V) for 2 minutes. The detailed procedure of cleaning is described in Appendix C.

5 Placing Substrates inside the chamber: Place the samples on substrate holder with silver paste. Place the cleaned shadow mask on top of the wafer.

6 Closing the Sputtering chamber: Close the chamber door. Make sure that there are no dust particles between contacts between door and chamber. Close the gas valve. Recheck wither steps 1-5 are performed correctly. Turn on the rotary pump and gauge meter. Gauge meter shows pressure inside the chamber. When the pressure goes

down near 0.1 Torr start turbo pump (the blinking green light will be turned to continuous green). Set the turbo molecular pump into full range mode (846 cycles/s) and the go to the standby mode (546 cycles/sec) during deposition. Wait for 1 hour to create sufficient vacuum in the order of 10^{-6} Torr. If we need to increase temperature for our deposition turn on the heater set the programmed for particular temperature through PID controller.

C.2. Performing Deposition

7. Creating environment for sputtering: After creation of vacuum inside the chamber turn it into standby mode and switch on the chillier. Chillier cools the target gun which will be heated during sputtering.
8. Supplying gases to chamber: Connect the required gas pipes from the cylinder to the gas inlet. Adjust the Mass Flow Controller for providing required gas flow rates (Don't turn on gas flow now). Release the gases from cylinders.
9. Evacuating pipes: Turn on the gas flow from MFC. When the speed of turbo molecular pump reaches a speed of 546 cycles/sec, close the gate valve 80% (not fully) and opens the gas inlet such that atmospheric air inside the pipes comes inside the chamber. Close the gas inlet when the vacuum gauze shows pressure inside the chamber in the order of 10^{-1} torr (generally it will complete with in fraction of seconds). Open the gate valve slowly waits for 5 minutes. Repeat this process 2-3 three times. This process is called Throttling.
10. Setting the parameters: Close the gate valve and open the gas inlet fully to apply the gas into the chamber. Set the working pressure by controlling and observe the pressure on gauze meter. Check the continuity test on target again and connect power supply to target and turn on power. Make sure that shutter is closed before turning on the deposition.
11. Performing deposition: Apply the required amount of power. This will generate the plasma inside the chamber. In case if we need RF power for the deposition of dielectric films turn on the RF power supply and matching unit. Adjust the matching circuit by controlling manually after setting it proper matching and reset into manual mode. Wait until plasma sustains. Go for presputtering on shutter and remove the shutter and the sputtering will starts. Start the timer of ours.

12. Stopping deposition: When it is over turnoff the power supply and after 5 min turn off the gas flow and close gas inlet, MFC and cylinders.
13. Insitu annealing: If we want to perform annealing in a particular gas ambient, connect it chamber and control MFC for gas flow. Open the gas inlet and control the gate valve to get sufficient pressure inside the chamber. Set the temperature and rise of temperature from the controller.

C.3. Closing the sputtering system

14. When it is over stop the heater and close gate valve fully and stop the gas flow from gas inlet, MFC and cylinder.
15. Switch off turbo from turbo controller. After 5 minutes switch off the rotary pump.
16. When the temperature reaches to 40°C (meanwhile turbo will went off). Release air inside to chamber and open the door to take down out of samples.
17. Open the gas valve from chamber which ensures further vacuum creation if we needed.

APPENDIX D
ELECTRICAL CHARECTERIZATION

D.1 Introduction

Characterization of semiconductor devices in wafer stage requires highly precision measurement devices. To observe the leakage currents and device capacitances Source Measure Units (SMU) and LCR meters are required. Automation of measurements should be performed to minimize the miscalculations by the manual handling. This can be accomplished by LabVIEW programming [5].

LabVIEW is a graphical programming language that uses icons instead of lines of text to create applications [5]. In contrast to text-based programming languages, where instructions determine program execution, LabVIEW uses dataflow programming, where the flow of data determines execution. In LabVIEW, we build a user interface with a set of tools and objects. The user interface is known as the front panel. We then add code using graphical representations of functions to control the front panel objects. The block diagram contains this code. In some ways, the block diagram resembles a flowchart. LabVIEW programs are called Virtual Instruments, or VIs, because their appearance and operation imitate physical instruments, such as oscilloscopes and multimeters. Every VI uses functions that manipulate inputs from the user interface or other sources and display that information or move it to other files or other computers.

D.2 Current-Voltage (I-V) Measurements

For measurement of I-V, Keithley 2636A SMU (Figure D.4b) is used. Keithley 2636A SMU is a dual channel SMU [6]. In operation each channel can act as a voltage source, a current source, a voltage meter, a current meter, and an ohmmeter. It offers wide dynamic range: 1fA to 10A and 1uV to 200V. It is controlled automatically by LabVIEW programmed Virtual Instruments (VIs). Figure D.1 shows the front panel diagram of current - voltage measurement system that we have developed. It can provide different types of sweep voltage/currents as shown in Figure D.2 and measure both voltage and currents.

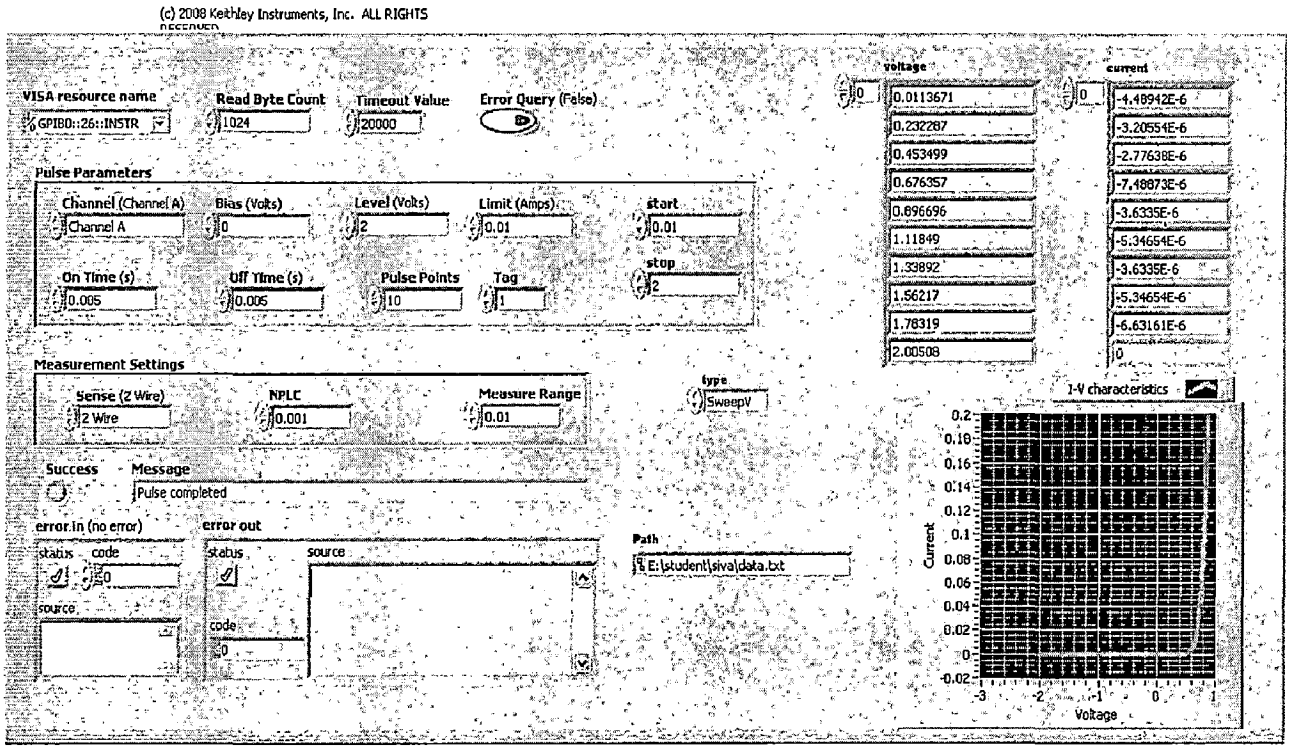


Figure D.1 *Front panel of LabVIEW program used for current-voltage measurements.*

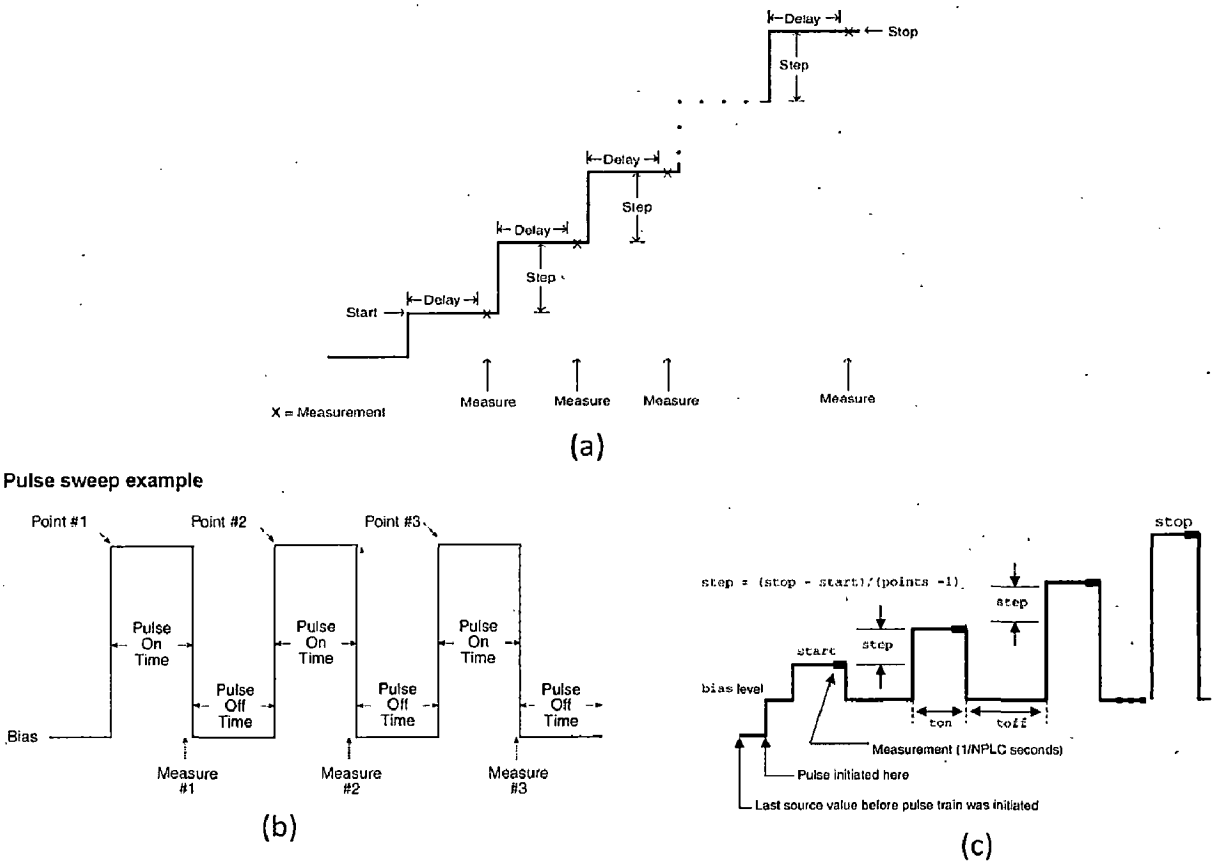


Figure D.2 *Various types of sweep inputs used for I-V characterization*

(a) Linear Sweep (b) Fixed pulse sweep (c) pulsed continues sweep [6].

(A) Linear staircase sweep

As shown in Figure D.2, this sweep type steps from a start voltage or current value to an ending (stop) value. A measurement is made at each step after a specified delay period (settling time). The step size is determined by the start and stop levels, and the number of sweep points:

Step size = (stop value – start value) / (points - 1)

When this sweep starts, the output will go to the start source level. The output will then change in equal steps until the stop level is reached. The delay parameter determines the time duration before the measurement at each sweep step.

(B) Fixed pulse sweep

A fixed pulse sweep outputs fixed voltage or current pulses. When this sweep executes, the output will go from the bias level to the "on" level of the first pulse. The time duration at each pulse level is determined by the programmed on time while the period between pulses is determined by the programmed off time.

(C) Continuous pulse sweep

As shown in Figure this sweep type starts from start voltage, end at stop voltage, and returns to a bias level between the pulses. Each pulse step will be on for t_{on} time and then at the bias level for t_{off} time. Compliance limit points the maximum allowable measurement value during the entire sweep. The pulse train will be comprised of specified pulse-steps.

With the different type of sweeps, which are controlled from the shown front panel observation of the I-V measurements are highly efficient with in short time.

D.3 Capacitance-Voltage Measurements

4300 Wenkerr precision LCR meter (Figure D.4(c), 20 Hz to 100 kHz, in conjunction with Keithley 2636A (figure D.4(b)) Source Measure Unit (SMU),Eurotherm Temperature Controller(figure 4.4(d))and a probe setup (Figure 4.4(a)) are used to carry out the high frequency characterization of the MOS capacitor.

D.3.1. Experimental Procedure

After appropriate, open correction, voltage was applied to the MOS (chuck, in case of C-V) which consisted of a dc voltage (-5 Volts to 5 Volts, 10ms delay time, 5 mV step size) on which a very small ac voltage, Vpp ~ 10 mV, with frequency 100kHz is superimposed. The response was measured with a vector ammeter and a vector ammeter, which are included in the analyzer setup. The compliance was set to 100 mA. The response was modeled as the response from a parallel combination of capacitance and parasitic resistance, which is later corrected for, in the calculations. The whole commands are given by LabVIEW program developed by us.

D.3.2 Equivalent Circuit

Figure D.3 below shows the equivalent circuit for the MOS capacitor. For an NMOS, at negative dc bias, the majority carriers, (holes) pile up at the oxide semi-conductor interface [1, 3]. Under these conditions the state of the system can be changed very rapidly. For typical semiconductor doping, the majority carriers, the only carriers involved in the operation of the accumulated device can equilibrate with a time constant on the order of 10^{-10} to 10^{-13} sec. Consequently, at probing frequencies ~ 100 kHz, the device follows the applied a.c signal quasi-statically, with the small a.c signal adding or subtracting a small ΔQ on the two sides of the oxide. Hence, C_{ox} gives the net capacitance in the accumulation mode.

Under the depletion mode, the NMOS is characterized by a –Q charge on the gate and a +Q depletion layer charge in the semiconductor. The depletion layer charge is related to the withdrawal of majority carriers from an effective width W adjacent to the oxide-semiconductor interface, and hence charge state in the system can be changed rapidly.

For all probing frequencies, this situation is analogous to two parallel plate capacitors, C_{ox} and C_{dep} are in series. Once inversion is achieved, an appreciable number of minority carriers pile up near the oxide-semiconductor interface in response to the applied dc bias. The d.c. width of the depletion layer tends to maximize at Wd_{max}. The inversion layer charge fluctuates in response to the ac signal. If the measurement frequency is very low, the minority carriers can be generated or annihilated in response to the a.c signal. C_{ox} gives capacitance in the inversion mode. If on the other hand, the

measurement frequency is high, generation–recombination process will not be able to supply or eliminate minority carriers in response to the a.c signal and the situation is equivalent to C_{ox} and C_{dep} (max width) in series, which makes Capacitance minimum at all inversion biases.

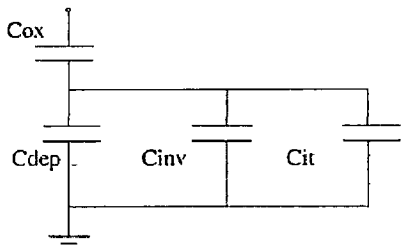


***Figure D.3** Simple capacitance equivalent circuit for MOS structure*

D.3.3 Extraction of parameters from high frequency C-V curves

After generating a C-V curve, we can compensate the measurements for series resistance. The series resistance (R_{SERIES}) can come from either the substrate (well) or the backside of the wafer. For wafers typically produced in fabs, the substrate bulk resistance is fairly small (<10Ω) and has negligible impact on C-V measurements. However, if the backside of the wafer is used as an electrical contact, the series resistance due to oxides can significantly distort a measured C-V curve. This extra series resistance particularly affects HF-CV curves, because the high-frequency capacitance calculations are based on amplitude change and phase shift. The extra series resistance cannot be reduced to a simple two-element (series or parallel) model that the HF-CV analyzer can use to calculate capacitance and conductance.

However, we can compensate for this series resistance via post-test calculations using the formulas below [7] which are based on the simplified three-element model.

$$Cc = \frac{(G_m + w^2 C_M^2)}{a^2 + w^2 C_M^2} C_M \qquad \text{(D.1)}$$

$$Gc = \frac{(G_m + w^2 C_M^2)}{a^2 + w^2 C_M^2} G_M \qquad \text{(D.2)}$$

In these equations, C_M is the measured capacitance and Cc is the corrected capacitance G_M is the measured conductance and G_C is the corrected conductance,

$$a = G_M - (G_M^2 + w^2 C_M^2) R_{Series} \qquad \text{(D.3)}$$

R_{SERIES} is the series resistance, and w is the angular frequency (radians sec^{-1}). R_{SERIES} may be calculated from the capacitance and conductance values that are measured while biasing the DUT (device under test) to the accumulation region. Use the following equation:

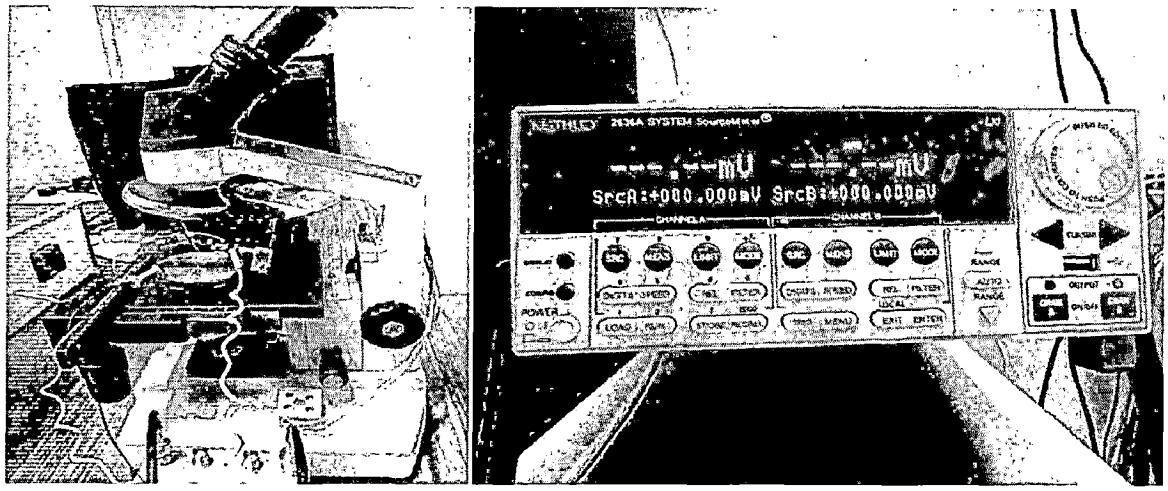
$$R_{SERIES} = \frac{(\frac{G_M}{wC_M})^2}{(1+(\frac{G_M}{wC_M})^2]G_M} \qquad \text{(D.4)}$$

Using the equations D.1, D.2 and D.3 accurate Capacitance-Voltage measurement is done.

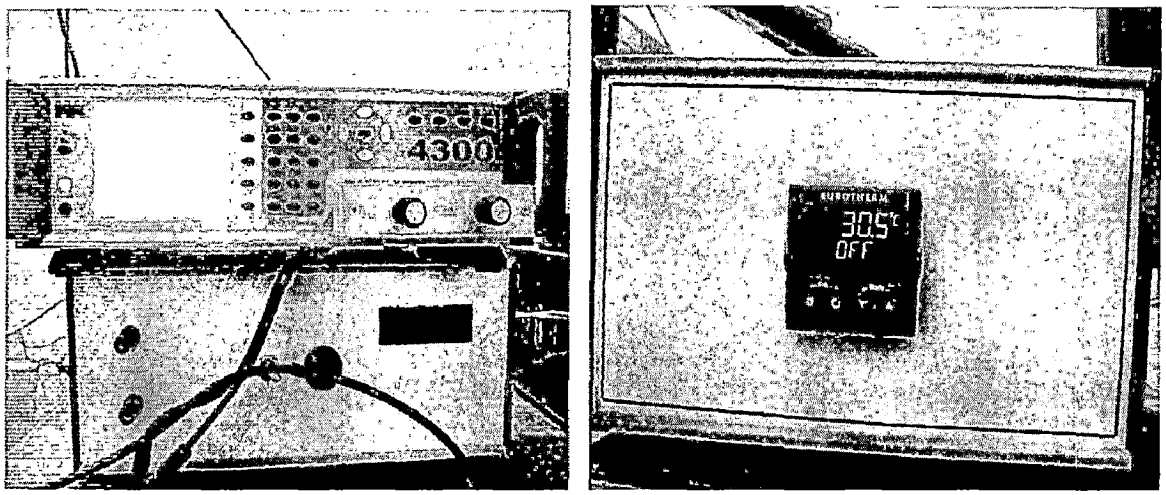
After extracting accurate capacitance and series resistance the following parameters and equations are used to calculate fixed oxide charge density, equivalent oxide thickness and mobile oxide charge density. [1, 2, 3, 4, and 8]

- Thickness of insulator(t_I) — 30nm (surface profilometry measurements)
- Permittivity constant of air(ϵ_o) — 8.834×10^{-14} F/cm
- Charge of electron(q) — $q=1.61\times10^{-19}$ coulombs
- Mass of electron(me) — $m_e = 9.1 \times 10^{-31}$ kg
- Boltzmann constant(k) — 1.38×10^{-23}
- Dielectric constant of SiO_2(ϵ_{SiO2}) — 3.91
- Dielectric constant of Si (ϵ_{Si}) — 11.8
- Electron affinity (χ_{Si}) — 4.15 volts
- Energy band gap (E_{gSi}) — 1.1eV at (27^0C)
- Temperature(T) — T=273+measurement temperature in °C
- Thermal velocity(υ_T) — $\upsilon_T = 100 \times \sqrt{\frac{qT}{m_e}}$ cm/sec
- Thermal Voltage(Vt) — $V_t = \frac{kT}{q}$ volts
- Intrinsic Concentration(n_i) — $n_i = 3.10 \times 10^{16} T^{3}/_{2} e^{-0.603/V_t}$ atoms/cm^3
- Doping Concentrating (N_A) — 2×10^{15} atoms/cm^3
- Accumulation capacitance (C_{ox}) — $C_{OX} = \frac{C_{OXFARWARD}+C_{OXBACKWARD}}{2}$ Farads
- Area of cross-section (A) — $A = \pi r^2 = \pi \times (1 \times 10^{-2})^2 = 1 \times 10^{-4} cm^2$
- Dielectric constant (ϵ_{HfO2}) — $\frac{A}{C_{OX}} = \frac{t_I}{\epsilon_I} = \frac{t_I - t_{SiO2}}{\epsilon_{high-k}} + \frac{t_{in}}{\epsilon_{SiO2}}$

- Inversion Capacitance (C_{inv}) $C_{inv} = \frac{C_{invFARWARD}+C_{invBACKWARD}}{2}$ Farads
- Depletion Capacitance (C_{dep}) $C_{dep} = \frac{C_{OX}C_{inv}}{C_{ox}+C_{inv}}$ Farads
- Max. Depletion width (W_{dmax}) $W_{Dmax} = \frac{A\epsilon_{Si}\epsilon_O}{C_s}$ centimetres
- Bulk function ($\varnothing_B$) $\varnothing_B = V_t log\left(\frac{N_A}{n_i}\right)$ volts
- Lambda(λ) $\lambda = \sqrt{\frac{V_t\epsilon_{Si}\epsilon_o}{qN_A}}$ centimeters
- Flatband capacitance $C_{FB} = \frac{C_{OX}\epsilon_{si}\epsilon_O A/\lambda}{\left(C_{OX}+\epsilon_{Si}\epsilon_o A/\lambda\right)}$ Farads
- Midgap depletion width(W_{dmid}) $W_{dmid} = \sqrt{\frac{2\varnothing_B\,\epsilon_{Si}\epsilon_o}{qV_t}}$
- Midgap Capacitance (C_{mid}) $C_{FB} = \frac{C_{OX}\epsilon_{si}\epsilon_O A/w_{Dmax}}{(C_{OX}+\epsilon_s\epsilon_o A/w_{Dmax})}$ Farads
- Midgap Voltage(V_{mid}) (Interpolating from C-V curve) Volts
- Flatband voltage(V_{fb}) $V_{fb} = \frac{V_{fbforward}+V_{fbbackword}}{2}$ volts
- Threshold Voltage(V_{th}) $V_{th} = V_{fb} + 2\varnothing_b + \frac{qN_AW_{dmaxB}A}{C_{OX}}$ volts
- Work function of Al(ψ_{Al}) 4.08 volts
- Work function of Si (ψ_{Si}) $\psi_{Si} = X_{Si} + \frac{E_g}{2q} + \square_b$
- Work function difference (ψ_{ms}) $\psi_{ms} = \psi_{Al} - \psi_{Si}$
- Charge defects combined(N_T) $N_T = \frac{(-V_{fb}+\psi_{ms})C_{OX}}{qA}$ cm^{-2}
- Sigma(σ) $10^{-15}cm^2$
- Generation life time of carriers(τ_g) $\tau_g = \frac{10^6}{\sigma v_T N_T}$ milliseconds
- Fixed Oxide charge density (N_{fox}) $N_{fox} = \frac{C_{OX}}{q}(-V_{midgap} + \psi_{ms} + \varnothing_b + \frac{qN_aW_{Dmid}}{C_{ox}})$
- Interface charge density (N_{it}) $Nit=N_T-N_{fox}$ cm^{-3}



(a) (b)



(c) (d)

Figure D.4 *Instruments used for electrical characterization*
(a) Prober (b) Keithley 2636A (c) Wenkerr LCR 4300(d) Euro therm 3210

D.4 References

[1] Robert F.Pierret, "*Semiconductor Device Fundamentals*", Willey New York, 1998.

[2] Muller S. and Theodore Kamini, "*Device Electronics For Integrated Circuits*", 2001.

[3] Streetman and Banerjee, "*Solid State Electronic Devices*", Persons, 2009.

[4] Size S.M., "*Physics of Semiconductor Devices*", John Wiley & Sons, 2005.

[5] National Instruments, "Introduction to LabVIEW programming", *http://www. Ni.com/LabVIEW.*

[6] Keithley Instruments, "User Manual for Keithley 2636A", *http://www.keithley .com/K2636A/downloads.*

[7] WenKerr Instruments, "User Manual for WenKerr 4300".

[8] Nicollian E. H. and Brews J. R., "*MOS (metal oxide semiconductor) Physics and Technology*", 2005.

MATLAB Program

1. MATLAB Code to extract the parameters from the experimental CV characteristics.

```
%CV analysis
%date: 9th Jun 2011
%program to extract CV data for Nano electronics lab
  import ('C:\CV DATA\Siva ---- Wednesday\HFCV\sio2\unannealed-1\Data.xlsx ');

voltage = Data(:,1);
cp_FORWARD= D03(:,2);
rp_BACKWORD=D03(:,3);
len = length(voltage);

% calculate series correction
w = 2* pi * (10 ^ 5 ); % frequency
for i =1:1:len
      cs(i) = cp(i) + 1 / ( w *w * cp(i) * rp(i) * rp(i) ) ;
and


% splitting the data , to get forward and backward curves

voltage_forward(1:len/2)=voltage(1:len/2);
voltage_backward(1:len/2)=voltage(len/2+1:len);
cs_forward(1:len/2) = cs(1:len/2);
cs_backward(1:len/2)= cs(len/2+1:len);
rp_forward(1:len/2)= rp(len/2+1:len);
rp_backward(1:len/2)= rp(len/2 +1:len);

% reversing the voltage , to get data for gate voltage (we were applying
% voltage to the substrate)

for i = 0: len/2 -1
```

```
   voltage_forward(i+1) = - voltage_forward(i+1) ;
    voltage_backward(i+1) = -   voltage_backward(i+1);

end

% plot capacitance per unit area

diameter = 300* (10^ (-4)); % in cm
area = (pi /4 )* (diameter ^ 2 );
 cs_forward = cs_forward /area ;
cs_backward = cs_backward /area ;

   i=1:1:len/2;
   plot(voltage_forward ,cs_forward ,'g',voltage_backward,cs_backward,'m')
   grid on
% calculate accumulation capacitance in farads
cox_accumulation1= max(cs_forward);
cox_accumulation2= max(cs_backward);
 cox_accumulation = 1/2 * ( cox_accumulation1 + cox_accumulation2)

% calculate thickness of oxide

epsilon_sio2 = 3.5;
epsilon_air = 8.85 * (10 ^ (-14) );
 thickness_oxide = (10 ^ (7))* epsilon_sio2 * epsilon_air / cox_accumulation % in nm

% calculate inversion capacitance in farads

c_inversion1= min(cs_forward);
c_inversion2= min(cs_backward);
 c_inversion = 1/2 * ( c_inversion1 + c_inversion2) % in farads
% calculate max depletion width
c_s = (c_inversion)*(cox_accumulation) / ( cox_accumulation - c_inversion) % in farads
```

```
epsilon_si = 11.8 ;
max_depletion_width = (10 ^ (7))* epsilon_si * epsilon_air / c_s; % in nm
 max_dep_width_cm = (epsilon_si * epsilon_air )/ c_s
% calculate doping concentration
boltzman_constant = 1.38* (10 ^ (-23));
temperature = 298; % in Kelvin
intrinsic_concentration =  (1.5*10 ^ (10)); % in cm -3
charge = 1.6 * (10 ^ (-19)); % in cm-3
vt = (boltzman_constant * temperature)/charge ;
Na = 10 ^ 15 ;                                          % initial assumption
error=1;
iteration=0;
 % applying iteration method to evaluate Na
 while (abs(error) >= 0.000002 )
bulk_function = vt * log (Na / intrinsic_concentration );
dep_width = sqrt((4 * bulk_function * epsilon_si * epsilon_air) / (charge * Na) );
error = max_dep_width_cm - dep_width ;
if (error > 0)
Na = Na - 0.5*10 ^ 14 ;
else
Na =Na + 0.5*10 ^ 14;
iteration=iteration +1;
end
end
% calculate debye length
lambda = sqrt ( (vt * epsilon_si * epsilon_air) / (charge * Na ) ) % in cm
% calculate C_FB
C_FlatBand= 1 / (lambda/( epsilon_si * epsilon_air ) + (1/cox_accumulation))
% calculate C_midgap
 bulk_function = vt * log (Na / intrinsic_concentration );
 dep_width_midgap = sqrt((2 * bulk_function * epsilon_si * epsilon_air) / (charge * Na)
)
 C_midgap= 1 /((dep_width_midgap/ (epsilon_si * epsilon_air)) +
(1/cox_accumulation))
```

```
    % calculate V_mg
  voltage_fit = -2.5:0.01:0;
 imax = length(voltage_fit);
 voltage_mg1 = interp1(cs_forward , voltage_forward ,  C_FlatBand);
 voltage_mg2 = interp1(cs_backward , voltage_backward ,  C_FlatBand);
 voltage_midgap = (voltage_mg1 + voltage_mg2 )/2
 % calculate V_fb
  voltage_fit = -2.5:0.01:0;
  imax = length(voltage_fit);
  voltage_fb1 = interp1(cs_forward , voltage_forward ,  C_FlatBand);
 voltage_fb2 = interp1(cs_backward , voltage_backward ,  C_FlatBand);
  voltage_flatband = (voltage_fb1 + voltage_fb2 )/2
 % to calculate the threshold voltage
  Voltage_threshold = voltage_flatband + 2 * bulk_function  +(charge* Na*
max_dep_width_cm / cox_accumulation )
 % to calculate charge defects
 work_func_al = 4.08;
 work_func_si = 4.05;
 work_function = work_func_al - work_func_si ;
 charge_defect_combined =(1/1.6)* (10 ^(19))*(-voltage_flatband + work_func_al -
work_func_si )* cox_accumulation
% to calculate generation lifetime of carriers
sigma = 10 ^ (-15); % in cm2
thermal_velocity = 10 ^ 7 ;% in cm_sec-1
tow_g  = (10 ^ 6 )*(1 / (sigma * thermal_velocity * charge_defect_combined ))
% to calculate generation current , Jgen
Jgen = (10^6)*(charge * max_dep_width_cm * intrinsic_concentration  / tow_g)
% to calculate fixed charge density
Qf = (cox_accumulation /charge)*(-voltage_midgap + work_function + bulk_function
+(charge*Na *dep_width_midgap / cox_accumulation))
% to calculate interface charge density
Qit =  charge_defect_combined - Qf
```

2. MATLAB Code to generate the ideal CV characteristics

```
% ideal curve
NA = input('Please input the bulk doping in /cm3 = NA');
xo = input('Please input the oxide thickness in cm , xo = ');
global UF
e0 = 8.85 * (10 ^(-14)) ;
q = 1.6 * (10 ^ (-19) );
k = 8.617 * (10^ (-5));
ks = 11.8;
ko = 3.9;
ni = 1.0*(10^10);
T =300 ;
kT =k *T ;
UF = log(NA/ni);
LD = sqrt((kT*ks*e0)/(2*q*ni));
US = UF - 21 : 0.5 : UF +21 ;
F = sqrt(exp(UF).*(exp(-US) + US -1) +exp(-UF).*(exp(US)-US -1));
VG = kT* (US + (US./abs(US)).*(ks*xo)/(ko*LD).*F);

%low frequency curves;
M = length(US);
nn=0;

for s=1:M
DENOML = exp(UF).*(1- exp(-US(s))) +exp(-UF).*(exp(US(s))-1);
WL(s) = (US(s)./abs(US(s))).*LD.*(2*F(s))./DENOML ;
cL(s) = 1.0 ./(1+ (ko*WL(s))./(ks * xo));
end

%high frequency curves
for  s= 1:1:M

    if US(s) <= 3
```

```
        cH(s) = cL(s);
      end

      if US(s) > 3
        INTG = QUAD('cvintegral', 3 , US(s) ,0.001);

        d =(exp(US(s)) -US(s) -1 )./(F(s).* exp(UF).*INTG);
        DENOMH =exp(UF).* ( 1- exp(-US(s))) + exp (-UF).*((exp(US(s))-1)./(1+d));
        WH(s) = LD.*(2*F(s))./DENOMH;
        cH(s) = 1.0 / ( 1 + (ko*WH(s))./(ks*xo));
      end
  end
plot(VG , cL)
Figure
plot(VG,cH)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 function y = cvintegral(x)
global UF
F = sqrt(exp(UF).*(exp(-x) +x -1) +exp(-UF).*(exp(x) -x-1));
y= (1 -exp(-x)).*(exp(x)-x-1)./(2*F.^3);
```

3. MATLAB Code to calculate the stretch out, smear and Dit

```
C_normalised = cs_backward / cox_accumulation ;
%to see the stretch out
i=1:1:len/2;
Figure(1)
   plot(voltage_backward ,C_normalised ,'g')
   grid on
   hold on
 i=1:1:M
   plot(VG,cH,'r')
% to calculate stretch out
 VidealFB = interp1(cH*cox_accumulation,VG ,C_FlatBand)
 stretchout = VidealFB - voltage_flatband ;
 Qff = stretchout * cox_accumulation / charge
```

```
% to see the smear out
voltage_backward_1(1:len/2) = voltage_backward(1:len/2) + stretchout
figure(2)
i=1:1:len/2;
plot(voltage_backward_1 ,C_normalised ,'g')
grid on
hold on
i=1:1:M;
plot(VG,cH,'r')
% to calculate smear
Cinterpolated = 0.3 : -0.01 : 0.1 ;
 z = 1:1:length(Cinterpolated);
Videal = interp1(cH,VG,Cinterpolated) ;
Vexp =  interp1(C_normalised, voltage_backward_1, Cinterpolated);
deltaV = (Videal - Vexp);
surface_pot_ideal = interp1(VG , US , Videal);
surface_pot_exp = interp1(VG , US , Vexp);
surface_pot = surface_pot_ideal - surface_pot_exp;
Dit = (cox_accumulation * (deltaV))/charge;
figure
plot(Videal,deltaV)
%%%%%%%%%%%
```