# DIGITAL PHASE LOCKED LOOP DESIGN

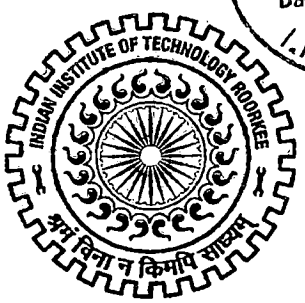
A DISSERTATION

*Submitted in partial fulfillment of the*
*requirements for the award of the degree*
*of*
MASTER OF TECHNOLOGY
in
ELECTRONICS AND COMMUNICATION ENGINEERING
(With Specialization in Semiconductor Devices & VLSI Technology)

By

**SRAVANKUMAR SREERAM**



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JULY, 2010

## CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation report entitled, **"DIGITAL PHASE LOCKED LOOP DESIGN"** towards the partial fulfillment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in **Semiconductors Devices and VLSI Technology (SDVT),** submitted in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work carried out during the period from July 2009 to July 2010, under the guidance of **Dr. Sudeb Dasgupta, Assistant Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee.**

The content of this dissertation has not been previously submitted for examination as part of any academic qualifications.

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# ABSTRACT

Phase Locked Loops (PLLs) have been widely used in radio, telecommunications, computers other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as micro processors and can generate high frequency clocks using frequency multipliers.

In this thesis, we present the design of Digital Phase Locked Loop (DPLL), which has low-power consumption and fast locking considerations. The previously proposed circuits for various units of PLL were modified for better performance and characteristics. Here we first systematically analyzed the working of basic PLL and its inner blocks from aspects of theoretical analysis and circuit operation. Based on the circuit architecture, both classifications and comparisons are made. Then we propose a high speed phase frequency detector. The proposed phase frequency detector is simple in its structure and has no glitch output as well as better phase characteristics. The speed of the proposed phase frequency detector is up to 16 GHz. Charge pump current is aimed at 150 μA and the output-frequency range of the oscillator is from 3.7GHz to 6.8GHz for 425-625mV control voltage range. The simulated PLL will use 100 MHz reference frequency. The lock time of proposed PLL is less than 0.45μs and average power consumption is 3.2 mw.

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# 1 INTRODUCTION

## 1.1 What is a PLL?

A PLL is a circuit that causes a particular system to track with another one. More precisely, a PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in frequency as well as in phase. In the synchronized state often called locked state the phase error between the oscillator's output signal and the reference signal is zero, or remains constant.

If a phase error builds up, a control mechanism acts on the oscillator in such a way that the phase error is again reduced to a minimum. In such a control system the phase of the output signal is actually locked to the phase of the reference signal. That is why it is referred to as a phase locked loop.

Phase locked loops are often used because they provide filtering to the phase or frequency of a signal that is similar to what is provided to voltage or current waveforms by ordinary electronic filters. Clocks are used in high performance digital systems to sequence operations and provide synchronization between various functional units. Requirement of higher data rates and high performance have forced technology scaling, due to which we are moving towards higher clock frequency.

Clock skew and jitter poses a major frequency limitation and hampers the performance of synchronous circuits. As the clock frequency increases, clock skew and jitter minimization in clock distribution network becomes more and more significant. Also, due to interconnection problems, there is a need for on chip frequency multiplier/clock generator in high performance microprocessors.

In the field of communication the growing demand of wireless communication systems, like cordless, cellular phones etc., for voice and data have led to the increase in the level of integration of RF transceivers. It led to the implementation of all the RF functions in CMOS technology because of its low cost and high level of integration. All the applications consist of a RF local oscillator (LO) block to down convert entire RF band to an intermediate frequency (IF). For an integrated transceiver the phase noise and spurious tone of this LO block is very critical and should be kept low.

Conventionally Phase Locked Loops (PLLs) are used in all the above mentioned applications namely: in clock distribution networks for skew minimization, as a clock generator in high speed systems and also in local oscillators of communication system.

### 1.2 Historical background

The French engineer Henri de Belliscize is considered to be the inventor of the PLL. His very first implementation goes back to the year 1932. De Bellescize published his vacuum tube circuit in the French journal Londe Electrique. The actual schematic is given below

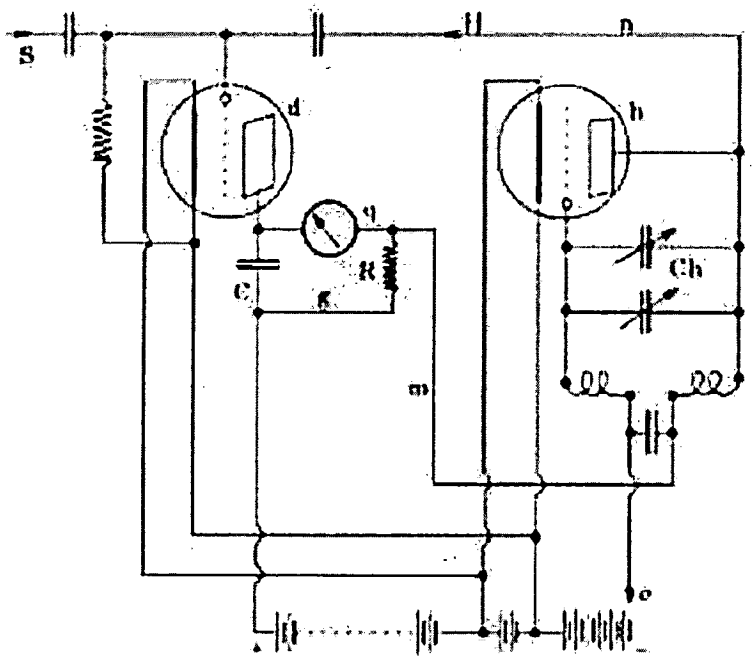



Figure 1.1 De Bellescize's PLL circuit of the year 1932

The tube on the right side of the figure 1.1 in combination with the LC tank circuit forms an oscillator. The output signal of the oscillator [labeled H] is capacitively coupled to the grid of the tube on the left. The reference signal [labeled S] is also fed via another capacitor to that grid. Because the grid voltage-anode current characteristic of electron tubes is nonlinear, the anode current contains a product term that is, a signal proportional to S×H. The circuit around the left tube is a multiplier type phase detector.

When the circuit is locked, this product is a measure of phase error that is the phase difference between the signals S and H. The parallel RC circuit in the anode is the loop filter. The voltage drop across the loop filter is therefore proportional to the phase error. That voltage applied to the anode of the right tube is now the difference of the battery voltage (e)

and the voltage drop across resistor R that is, the phase error modulates the anode voltage of the oscillator. Because the frequency generated by the oscillator is an almost linear function of anode voltage, the oscillator is a VCO indeed.

This brilliant invention was widely ignored by most engineers for about 20 years. One of the first large scales industrial applications of the PLL (back in the 1950s) was the color subcarrier recovery in color TV receivers. Somewhat later frequency synthesizers built from PLLs were used to generate a raster of frequencies in the local oscillator of FM receivers. The real breakthrough of the PLL came with desktop computers and with the PC, where PLLs are used for many types of data synchronization –for instance, reading digital data to and from floppy disks, hard disks, modems, tape drives, and the like. One of the largest applications today is probably the mobile phone, where the PLL is used again for frequency synthesis.

### 1.3 Classification of PLLs

#### 1.3.1 Linear PLL

The first PLL ICs appeared around 1965 and were also purely analog devices. An analog multiplier was used as the phase detector, the loop filter was built from a passive or active RC filter, and the well-known voltage-controlled oscillator (VCO) was used to generate the output signal of the PLL. This type of PLL is known as the linear PLL (LPLL) today.

#### 1.3.2 Digital PLL

In the years that followed, the PLL drifted slowly but steadily into digital territory. The very first digital PLL(DPLL), which appeared around 1970, was in effect a hybrid device: only the phase detector was built from a digital circuit(for instance, from an EXOR gate or a JK flip-flop), but the remaining blocks were still analog. That is why it is a semi analog circuit.

#### 1.3.3 All digital PLL

A few years later, the "all digital" PLL (ADPLL) was invented. The ADPLL is exclusively built from digital function blocks; hence it doesn't contain any passive components like resistors and capacitors.

### 1.3.4 Software PLL

PLLs can also be implemented "by software." In this case, the function of the PLL is no longer performed by a piece of hardware, rather by a computer program. This type of PLL is referred to as SPLL.

## 1.4 Working principle of PLL

The basic block diagram of PLL is shown in Figure 1.2. It consists of three basic functional blocks:

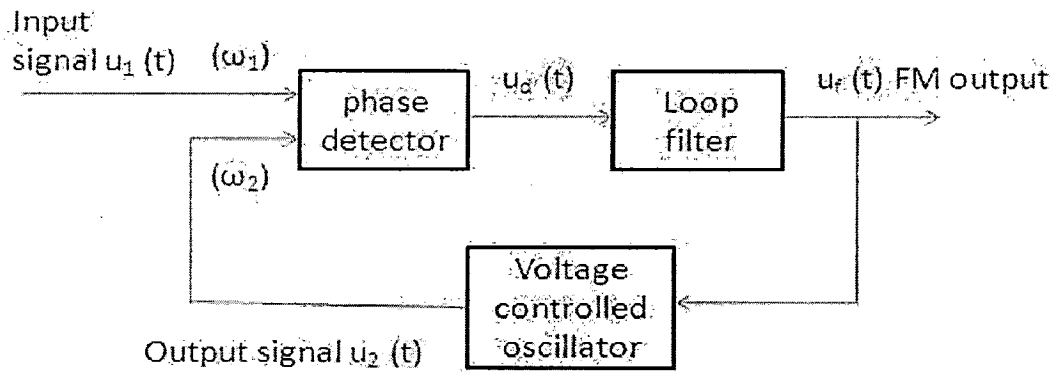



Figure 1.2 basic block diagram of PLL

First let us assume that the angular frequency of the input signal $u_I(t)$ is equal to the center frequency $\omega_o$. The VCO then operates at its center frequency $\omega_o$. As we see, the phase error theta e is zero. If $\theta_e$ is zero, the output signal $u_d$ of the PD must also be zero. Consequently the output signal of the loop filter $u_f$ will also be zero. This is the condition that permits the VCO to operate at its center frequency.

If the phase error $\theta_e$ were not zero initially, the PD would develop a nonzero output signal $u_d$. After some delay the loop filter would also produce a finite signal $u_f$. This would cause the VCO to change its operating frequency in such a way that the phase error finally vanishes.

Assume now that the frequency of the input signal is changed suddenly at time to by the amount $\Delta\omega$. As shown in figure 1.3, the phase of the input signal then starts leading the phase of the output signal. A phase error is built up and increases with time.

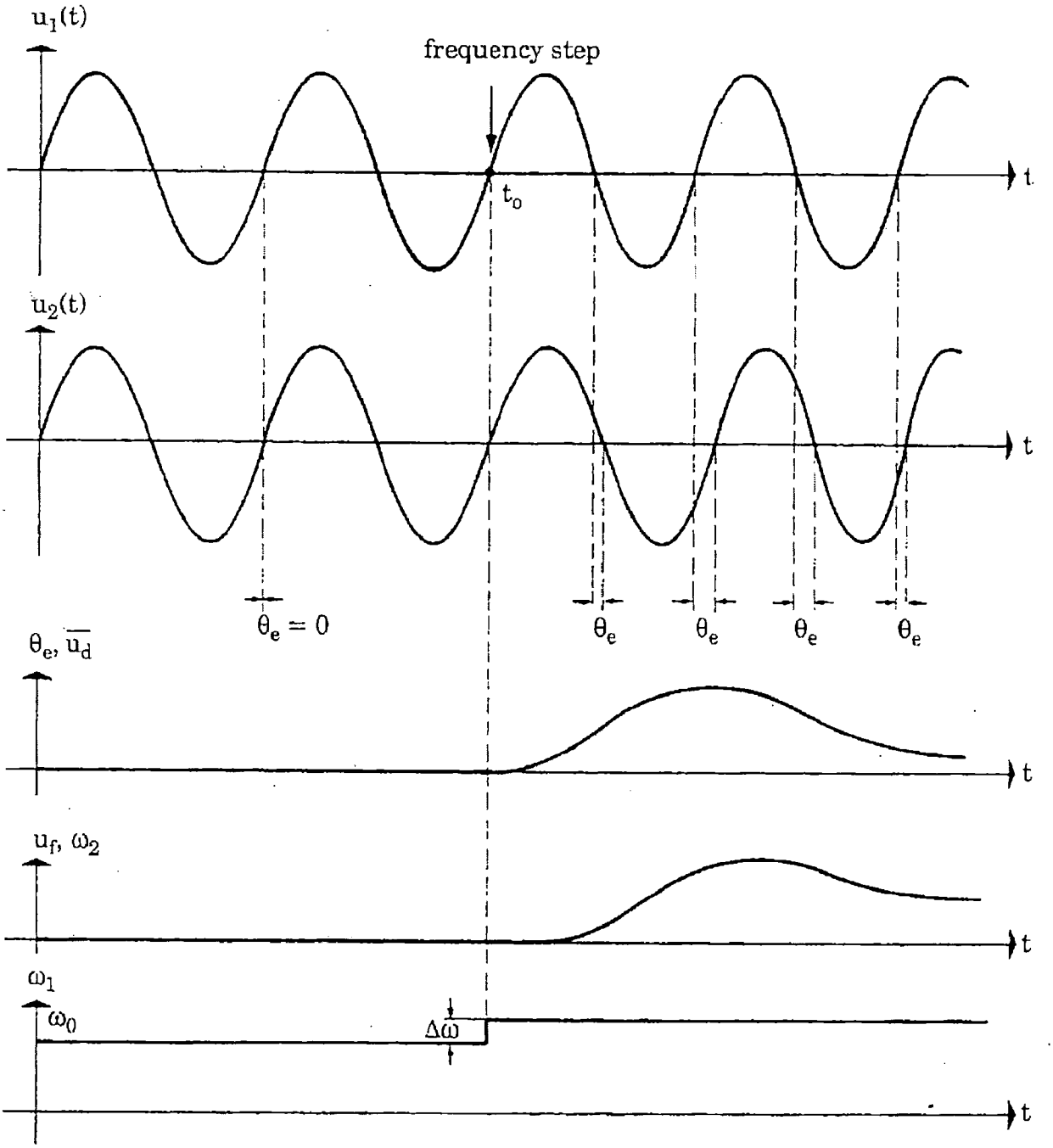



Figure 1.3 Waveforms of reference signal $u_1$ (t); VCO output signal $u_2$ (t); signals $\theta_e$, $\bar{u}_d$ as a function of time; angular frequency $\omega_2$ of VCO and loop filter output signal $u_f$ as a function of time; angular frequency $\omega_1$ of the reference signal $u_1$ (t).

The PD develops a signal $u_d$ (t), which also increases with time. With a delay given by the loop filter, $u_f$ (t) will also rise. This causes the VCO to increase its frequency. The phase error becomes smaller now, and after some settling time the VCO will oscillate at a frequency that is exactly the frequency of the input signal. Depending on the type of loop filter used, the final phase error will have been reduced to zero or to a finite value [7].

The VCO now operates at a frequency that is greater than its center frequency $\omega_0$ by an amount $\Delta\omega$. This will force the signal $u_f(t)$ to settle at a final value of $u_f = \Delta\omega / ko$.

### 1.5 Architecture of proposed PLL

The basic building blocks of the proposed PLL are phase frequency detector, charge pump, loop filter, voltage controlled oscillator and frequency divider.

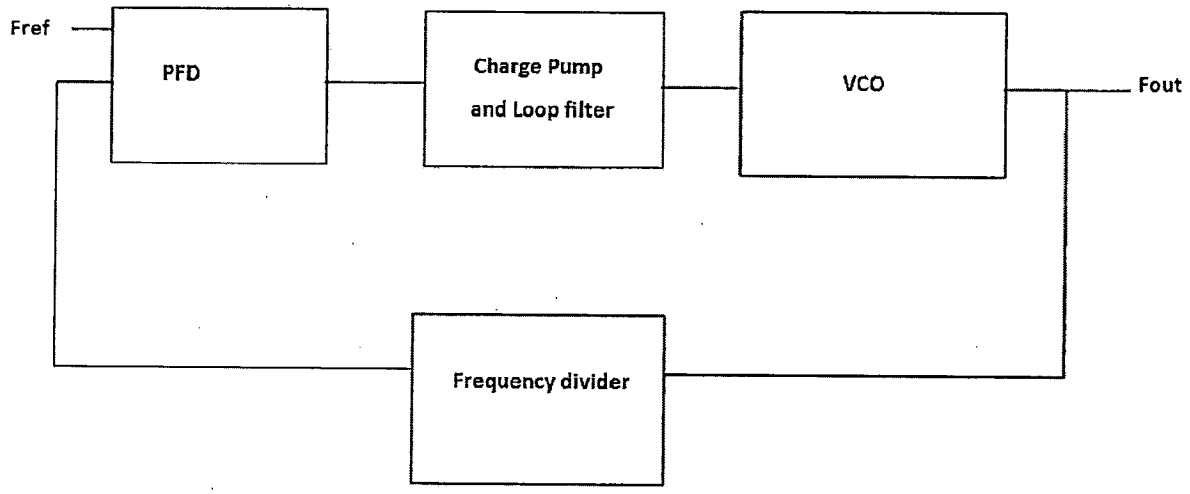



Figure1.4 Block diagram of the proposed PLL

#### 1.5.1 Phase detector (PD):

The phase detector is also known as phase comparator. Its main function is to detect and amplify the phase difference between the input signal and output of the voltage controlled oscillator. The output of phase detector is given by

$$u_d = K_d \theta_e \tag{1.1}$$

Where $K_d$ represents the gain of the phase detector. The physical unit of $K_d$ is volts per radian. The graphical representation of equation is shown below

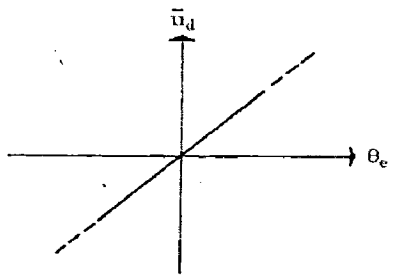



Figure 1.5 Transfer characteristics of phase detector

### 1.5.1a Phase frequency detector

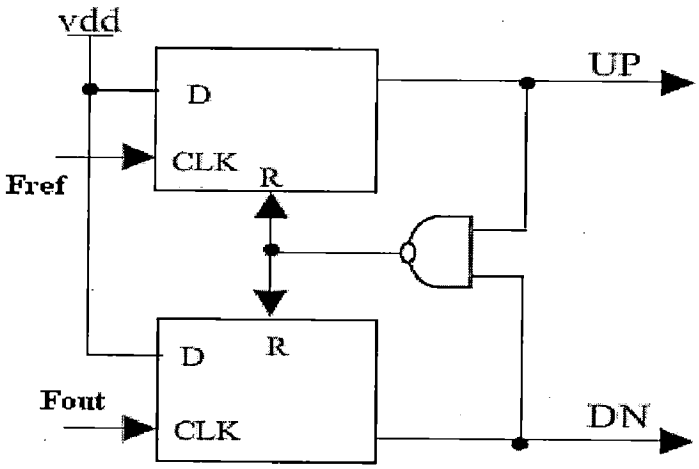



Figure 1.7 Phase frequency detector

The purpose of the phase detector is to detect the phase difference of the two signals applied at its input. Conventionally an EX-OR gate or a J-K flip flop was used as a phase detector [2]. They have a poor linearity range. An EX-OR gate can resolve phase differences in +/- $\pi/2$ range and JK flip flop in +/-$\pi$ range. Also, in EX-OR gate the output is duty cycle dependent. The most widely used phase detector is a tri-state phase detector as shown in figure 1.7. It is independent of duty cycle of the inputs. It consists of two D flip flops and a NAND gate in its reset path. The reset path must provide a sufficient width reset pulse in order to avoid dead zone (explained later). The leading edge of $\mathbf{F_{ref}}(\mathbf{F_{out}})$ sets UP (DN) pulse which is reset by lagging edge of $\mathbf{F_{out}}(\mathbf{F_{ref}})$. Figure (1.8a-1.8c) shows the output waveforms of the PD for all the three possible cases.

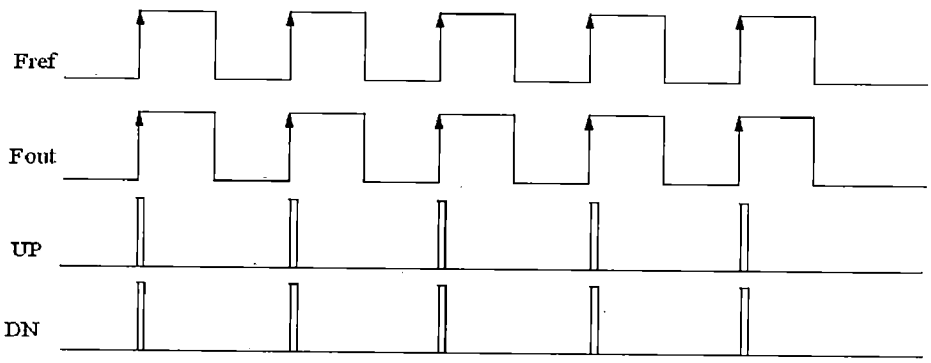



Figure 1.8a Waveforms for Fref and Fout in phase

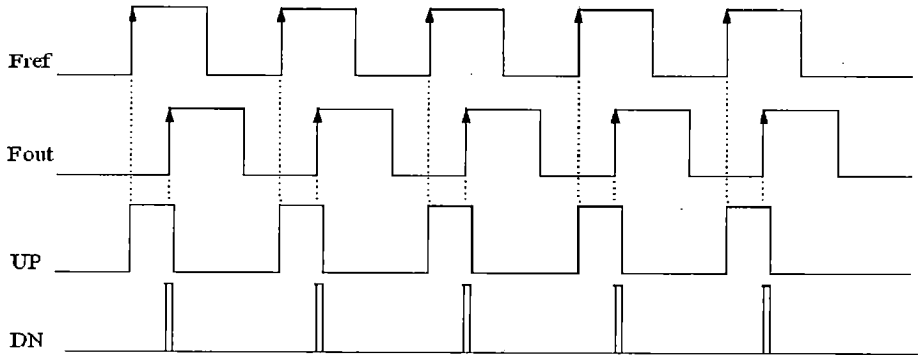



Figure 1.8b Waveforms for Fref leading Fout in phase

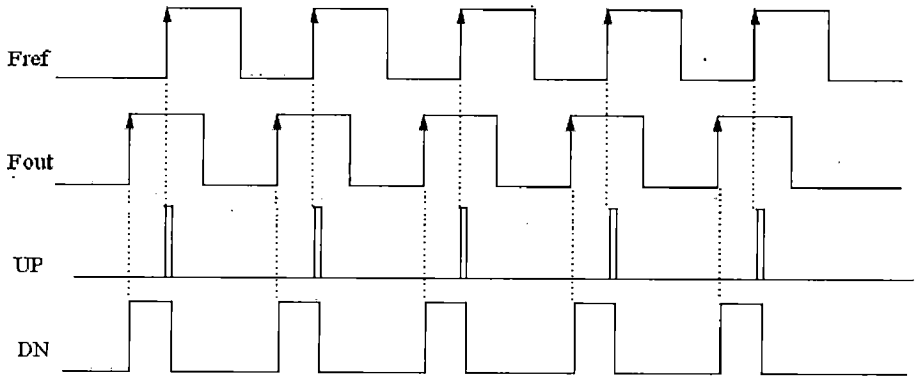



Figure1.8c Waveforms for Fref lagging Fout in phase

Depending on the operation described above the PFD can be in one of the three states:

- UP = 0, DN = 0 ---------- state-0
- UP = 0, DN = 1 ---------- state-2
- UP = 1, DN = 0 ---------- state-1

The state UP=1, DN=1 is prevented due the presence NAND gate that forces the PD to state 0 when such condition arises. The state diagram of the tri-state PD can be drawn as shown in figure 1.9.

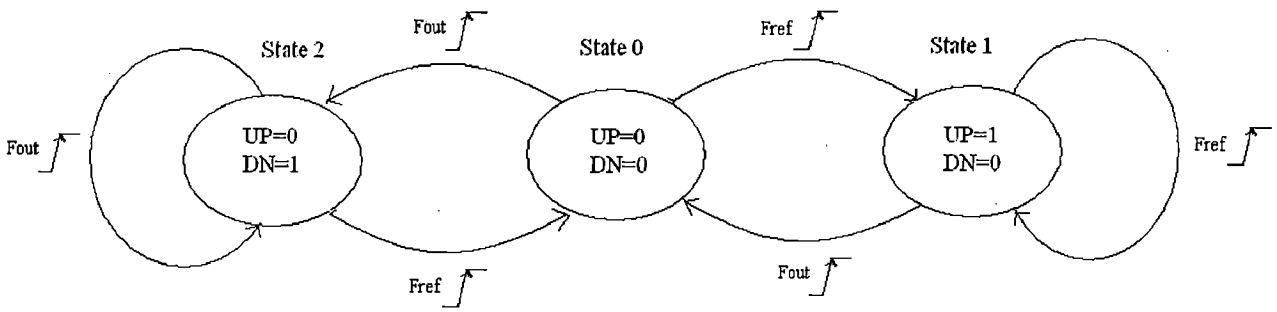
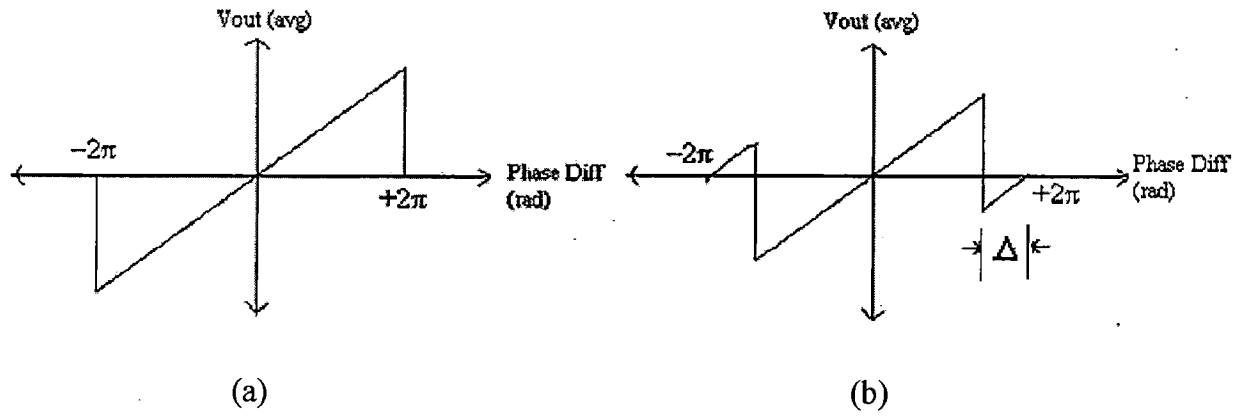



Figure 1.9 State diagram of tri-state PD

If the PD is in state 0, then a transition on $F_{ref}$ will take the circuit to state 1, where the state values are UP = 1 and DN= 0. The circuit remains in this state until a positive transition occurs at the $F_{out}$ and the PD returns to state 0. The transition from state 0 to state 2 is same as transition from 0 to 1 state. The only difference is that a positive transition at $F_{out}$ occurs instead at $F_{ref}$.

**Phase characteristics of tri-state PD**

The tri-state PD has a linearity range of +/- $2\pi$. Figure 1.10 shows the ideal and practical characteristics of tri-state PD [3].




(a) (b)

Figure 1.10 Phase characteristics of tri-state PD (a) ideal (b) practical

As seen from figure 1.10 the PD's phase characteristic is ideally linear for the entire range of input phase differences from $-2\pi$ to $2\pi$. However due to delay of the reset path, the linear range is less than $4\pi$ . This is because; when the phase difference is nearing $2\pi$ ($F_{out}$ lagging with respect to $F_{ref}$) the next leading edge of $F_{ref}$ arrives before the flip flops are reset due to finite reset delay. The reset overrides the new $F_{ref}$ edge and does not activate UP signal. The subsequent $F_{out}$ edge causes a DN signal. This effect appears as a negative output for phase difference higher then $(2\pi-\Delta)$ where $\Delta = 2\pi.T_p/ T_{ref}$.

$T_p$ - reset pulse width

$T_{ref}$ - period of the reference signal ($F_{ref}$)

The non ideal PD gives wrong information periodically. Maximum frequency of operation is given by [4].

$$F_{max}= 1/ 2\, T_p \qquad (1.2)$$

### 1.5.2 Charge pump and Loop filter:

The output signals of the phase detector are up and down signals which are given as inputs for the charge pump, control the flow of charge pumping into or out of the capacitor. Charge pump converts the digital signal into analog signal. The output of charge pump consists of a dc component and a superimposed ac component. The later is undesired so it is canceled by the loop filter. In most cases a first order, low pass filter is used. We can use higher order low pass filter also.

As the charge pump output will have the higher frequencies which are unwanted ripples, they are filtered out by the loop filter. Because the loop filter must pass the lower frequencies and suppress the higher, it must be a low pass filter. In most PLL designs a low pass filter is used. The different types of loop filters used in most PLL circuits are active lead lag filters and passive lead lag filters.

Most PLLs are considered as second order PLLs. The loop filter had one pole, and the VCO has a pole at s=0, so the whole system had two poles. If the phase detector directly controls the VCO output then the PLL will become first order, but these are rarely used because they offer little noise suppression. Because the hold range is naturally much higher than the natural frequency of the second order PLL, the first order PLLs offer larger bandwidth and hence tracks phase and frequency variations of the input signal very rapidly.

Due to its high bandwidth, the first order PLLs does not suppress noise superimposed to the input signal. Because this is an undesirable property in most PLL specifications, the first order PLL's are rarely utilized where noise suppression is not a primary concern.

Because higher order loop filters offer better noise cancellation, loop filters of order 2 and higher are normally used in critical applications. But it is much more difficult to obtain a stable higher order system than a lower-order one.

### 1.5.3 Voltage controlled oscillator (VCO):

It generates the frequency signal depending on the control signal that is the output of the loop filter. It oscillates at an angular frequency, which is determined by the output signal of the loop filter. The angular frequency is given by

$$\omega_2(t) = \omega_o + K_o u_f(t) \tag{1.3}$$

Where $\omega_o$ is the center frequency of the VCO and $K_o$ is the VCO gain. Its graphical representation is given as follows.

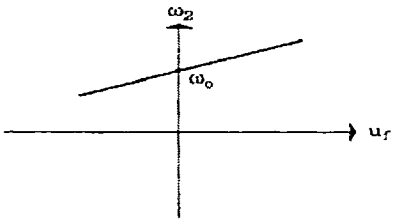



Figure 1.11 Transfer characteristics of VCO

In PLLs, two fundamentally different types of controlled oscillators are used relaxation oscillators and resonant oscillators. Relaxation oscillators are found in many PLL ICs built from standard CMOS technology. They cover a relatively restricted range of frequencies—from zero to about 50MHz. For higher frequency applications, up to the microwave region, oscillators with resonant tank circuits come into play. Some of these are implemented with discrete transistors and discrete passive components others are built with microwave-integrated circuits.

### 1.5.4 Frequency divider:

Frequency divider is a circuit whose output frequency is a fraction of the frequency of its input. For example frequency divider takes an input signal of a frequency, $f_{in}$, and generates an output signal of a frequency:

$$f_{out} = \frac{f_{in}}{n} \tag{1.4}$$

Where $n$ is an integer. Phase locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. Frequency dividers can be implemented for both analog and digital applications.

# 2 PHASE FREQUENCY DETECTOR

The phase detector is the foremost unit of a phase locked loop. Its purpose is to detect phase difference between the two signals applied at the input. A tri-state phase detector, mentioned in chapter 2, has an advantage of better linearity range from $-2\pi$ to $+2\pi$ and is the most widely used phase detector in phase locked loop. Due to this we incorporate a tri-state phase detector in our phase locked loop. The most important design considerations for a tri-state phase detector are:

- Dead Zone
- Power Consumption
- Maximum frequency of operation

Dead zone, resulting in undetectable phase difference between the inputs, can be minimized by designing the circuit such that, there exists a finite reset pulse width, when the two input signals are exactly in phase. The reset pulse width should be wide enough to just turn on the charge pump. Also, it should not be too wide, as in that case it would limit the maximum frequency of operation (eqn.(1.2)) and cause more ripples on the control voltage line (due to inherent current mismatch). The power consumption can be kept minimum by using minimum number of transistors and using lower supply voltage.

## 2.1 Conventional Phase Detector

Figure 2.1 shows one of the conventional phase detectors, which is implemented using static CMOS technology. As seen, this PD consists of D type flip flop made up of NAND gates [1].

This PD has severe limitations. It consists of large number of NAND gates, which corresponds to an excessively large number of transistors and thereby requiring a large chip area. Also, large number of transistors results in large power consumption.

In order to overcome its limitation a pre-charge type (PT) phase detector was proposed by Kondoh *et al* [5] as shown in figure 2.2. It worked on dynamic CMOS technology, utilizing the voltage generated at various nodes. However, the error detecting range of this phase detector was limited to $-\pi$ to $+\pi$.

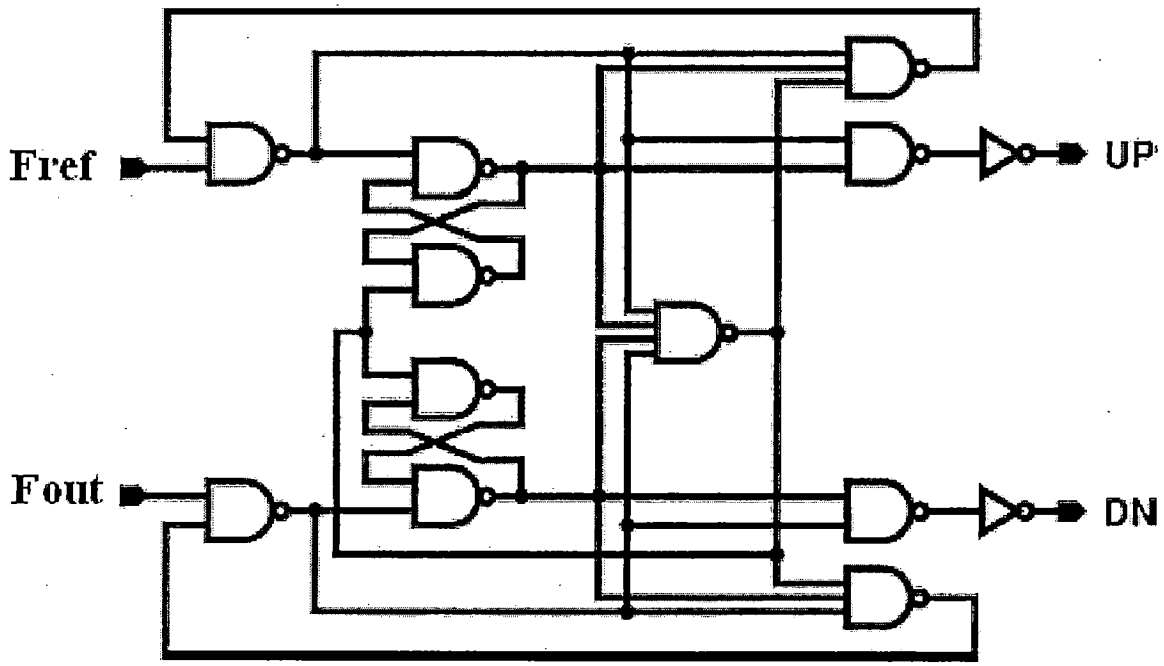



Figure 2.1 Conventional phase detector using NAND gates[1]

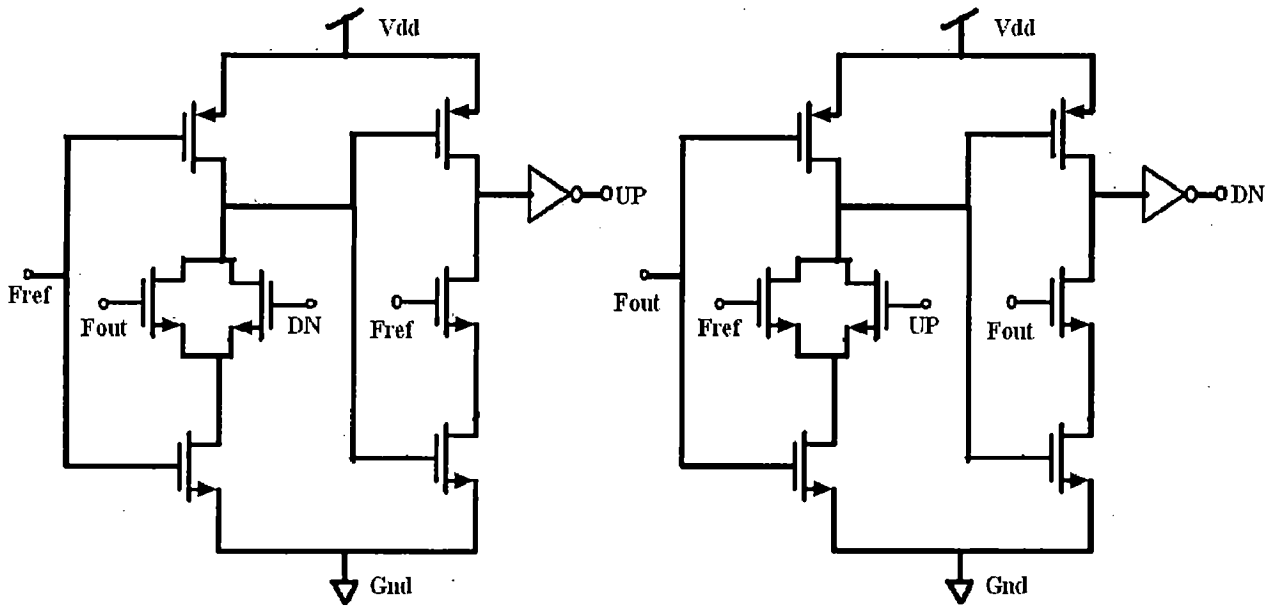



Figure 2.2 Pre-charge type phase detector [5]

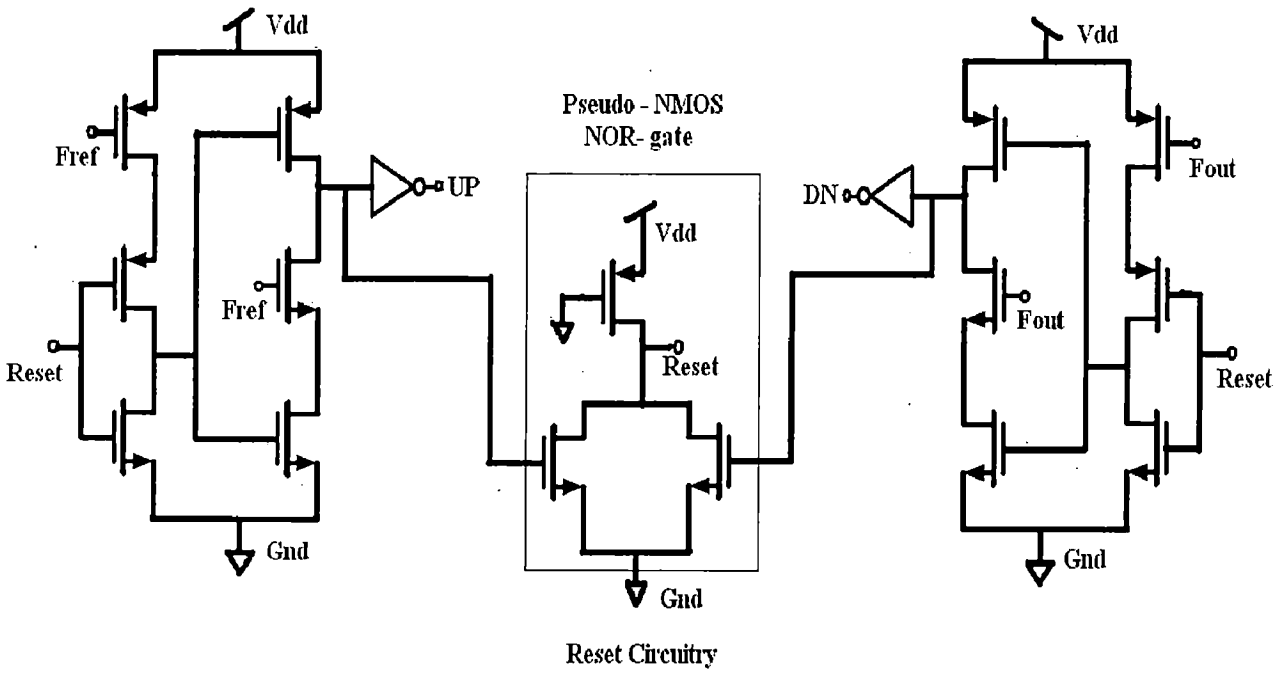



Figure 2.3 Phase detector using TSPC type D flip flop [6]

This limitation is removed by phase detector proposed by Lee *et al* [6]. It again works on dynamic CMOS technology and uses a TSPC-type D flip flop structure. It has good performance characteristic in terms of dead zone and provides a linearity range of $-2\pi$ to $+2\pi$, but requires an additional reset circuitry consisting of a pseudo-NMOS NOR gate. The pseudo-NMOS NOR gate makes the operation fast, but consumes static power when the NOR gate output is low and also the logic becomes ratioed.

## 2.2 Phase Detector Incorporated in Proposed PLL

The phase detector incorporated in the proposed PLL is shown in figure 2.4. It works on dynamic CMOS technology and is similar to the previously mentioned PD. It removes the reset circuitry which was required by the PD of figure 2.3, without sacrificing on its performance.

**Working:**

Initially both Fref and Fout are low therefore the transistors m1 and m7 are on (P-MOS). Due to this node A and node B gets charged to Vdd and hence switching off transistors m4 and m10. This also results in switching on of N-MOS transistors m6 and m12.

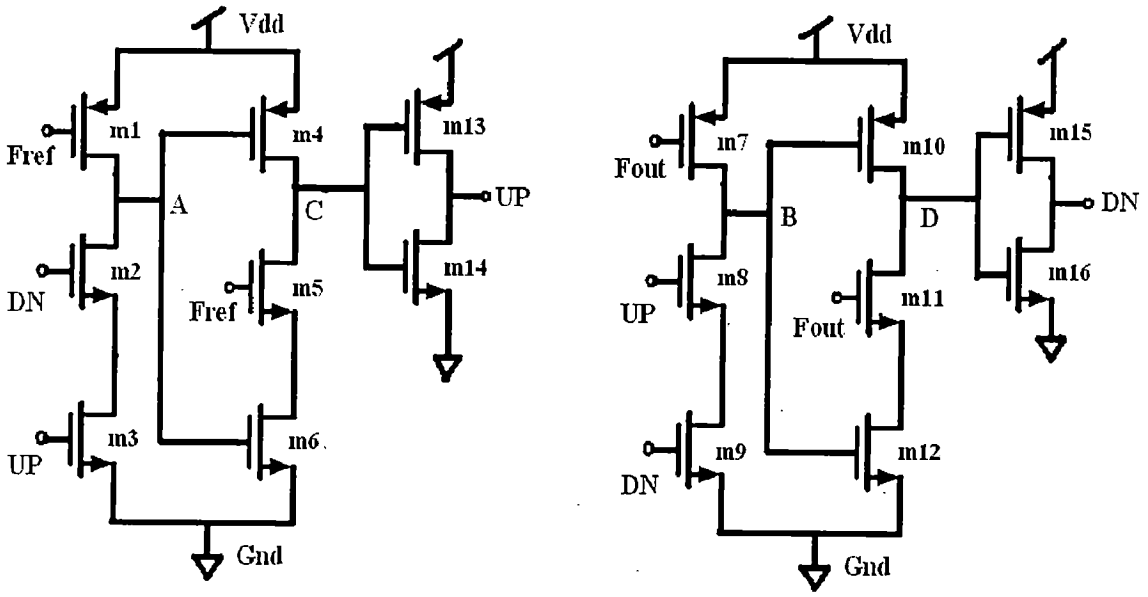



Figure 2.4 Phase Frequency Detector

Consider the case when Fref lead Fout in phase. When rising edge of Fref (leading in phase) arrives, it causes N-MOS transistor m5 to turn on and hence creating a low resistance path from node C to ground (m6 already on). Thus, node C discharges to ground potential and thereby causing UP to go high instantaneously. This high UP signal switches on m3 and m8. The circuit will remain in this state, even if Fref goes low. This is because node C is prevented from being pulled up as m4 is off (due to charges at node A).

Now, when rising edge Fout (lagging in phase) arrives DN signal goes high by similar mechanism as explained before. When this DN signal becomes sufficiently high, transistors m2 and m9 are turned on causing a low resistance path for node A and node B. Therefore, node A and node B discharges to ground potential, which results in P-MOS transistors m4 and m10 turning on. Due to this node C and node D are pulled up and causing UP and DN signal to go low. Exactly the reverse happens when Fout leads Fref. When both $F_{ref}$ and $F_{out}$ are in phase, reset pulses are obtained at UP and DN signals.

Thus, the above PD circuit utilizes the UP and DN signal directly for the reset operation, and hence eliminating the need for extra reset circuitry. The reset pulse generated is of sufficient width such that dead zone is almost completely eliminated.

The PD consists of minimum number (16) of transistors. Proper relative sizing of various transistors is required in order have rail to rail swings. The combined strength of m2, m3 (m8,

m9) should be more than m1 (m7). This is because, there exists a contention if Fout arrives when Fref is already low (in case of Fref leading Fout). Node A (B) must have a stronger pull down path than pull up, in order to get discharged. Similarly strengths of m4 and m10 should be weak in order to prevent UP and DN signal to go low until node A and node B are completely discharged to ground potential. The strengths of m5 (m11) and m6 (m12) should be high in order to generate instant response from the rising edge of Fref (Fout).

**Simulation Output and Results of Incorporated Phase Frequency Detector**

1. Figure 2.5 shows the simulation output for the case when Fref is leading Fout. The rising edge of $F_{ref}$ sets the UP signal, this UP signal is then reset by the rising edge of $F_{out}$. A short duration reset pulse is seen on DN signal when the reset operation takes place.

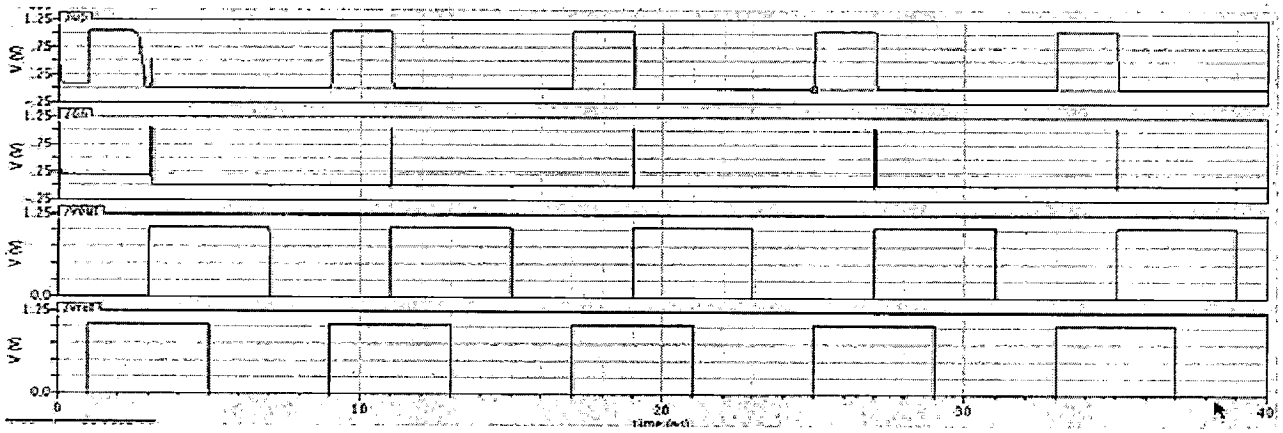


Figure 2.5 when Fref is leading Fout

2. Figure 2.6 shows the simulation output for the case when Fout is leading Fref. The rising edge of $F_{out}$ sets the DN signal, this DN signal is then reset by the rising edge of Fref. A short duration reset pulse is seen on UP signal when the reset operation takes place.

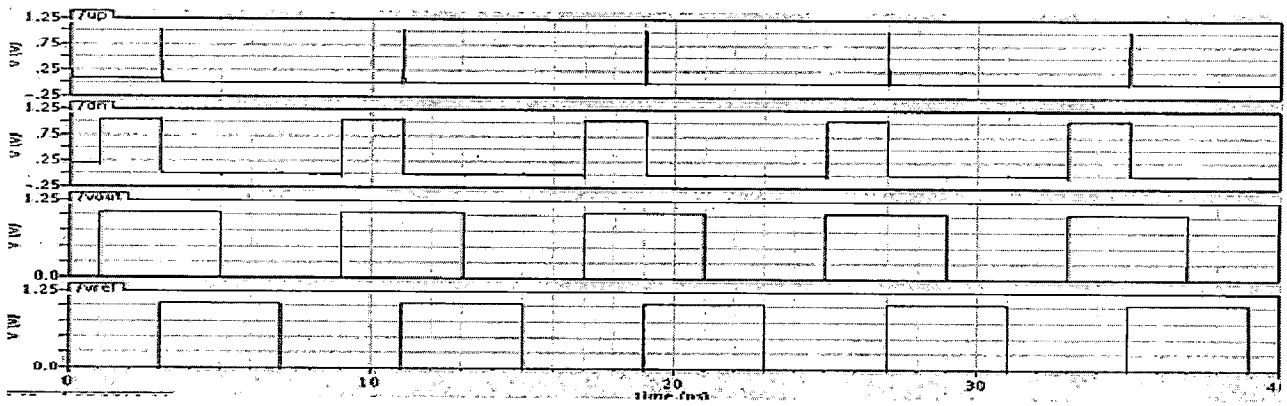


Figure 2.6 when Fref is lagging Fout

3. Fig. (2.7) shows the simulation output for the case when Fref and Fout is exactly in phase. As seen, only short duration reset pulse are obtained at UP and DN signal. These pulses are essential in order to eliminate dead zone. Also, the reset pulses are shown on a magnified scale.

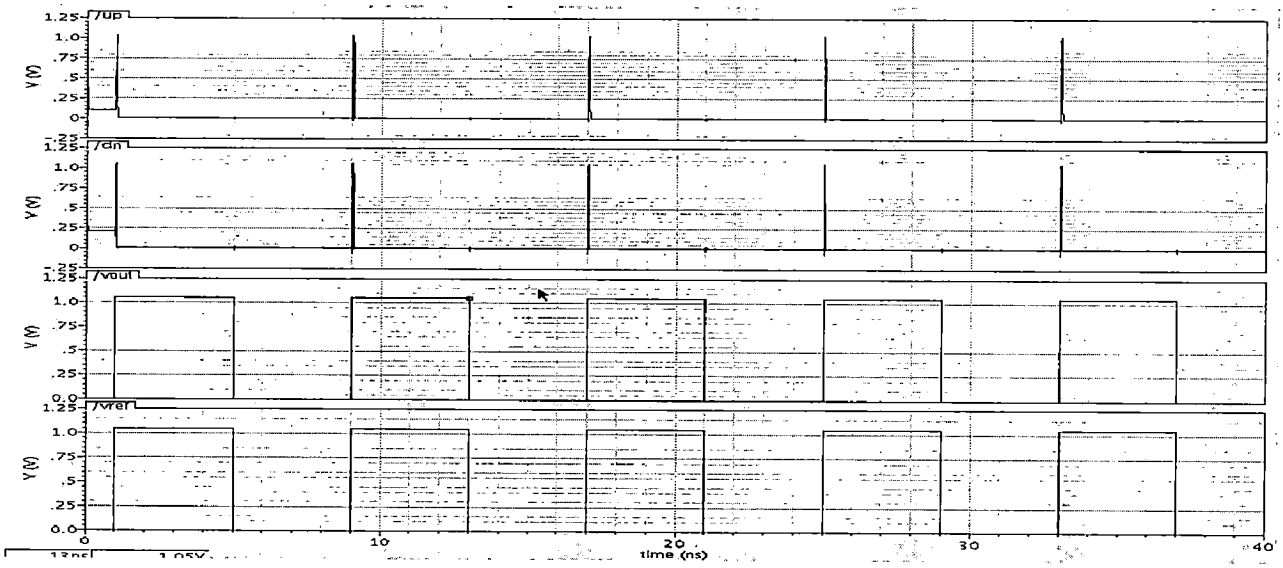



Figure 2.7 when Fref is exactly in phase with Fout

# 3 CHARGE PUMP AND LOOP FILTER

The charge pump is the second unit of PLL. It is responsible for generating necessary control voltage to the VCO unit. It utilizes the UP and DN signal provided by the phase detector, in order to pump in or pump out the charge from the loop filter capacitor. When PLL is in locked state, the control voltage is constant with some inherent ripples.

The important design considerations for an effective charge pump circuit are

- There should be minimum peak current mismatch
- The charge sharing phenomenon should be avoided
- The effect caused by channel charge injection and clock feed through should be minimized
- Output voltage range provided should be large

Minimum peak current mismatch ensures minimum static phase error between the two input signals ($F_{ref}$ and $F_{out}$) in locked state. The reason for this is as follows. In locked state the phase detector generates equal UP & DN pulses and the control voltage (Vctrl) is supposed to be constant. This means that quantity of charge $Q_{charge}$ and the one of discharge $Q_{discharge}$ must be equal and given by eqn.(3.1)

$$Q_{charge}=I_{UP}* T_{UP} = Q_{discharge}= I_{DN} * T_{DN} \quad (3.1)$$

where $T_{UP}$ and $T_{DN}$ are duration of UP and DN pulses in locked state, or charging and discharging time in one cycle. If $I_{UP}$ and $I_{DN}$ are different, then there has to be some difference between the duration of UP and DN pulse in order to satisfy eqn. (3.1) . The PLL, thus creates a static phase difference between its inputs in order to maintain the difference between the duration of UP and DN pulse in accordance with eqn. (3.1).

The charge sharing, charge injection and clock feed through phenomenon results in periodic ripples and sudden jumps on the control voltage line. This results in generation of spurious tones and jitters at the output. This becomes critical when PLL is used as a frequency multiplier in a local oscillator of a transceiver [7]. These non ideal effects can be reduced by suitable circuit level manipulations. The output voltage range provided by charge pump should be as large as possible. This helps to keep the VCO gain to a lower value (for a given operating frequency range), which further helps to decrease the sensitivity of VCO to sudden variations on control voltage line.

### 3.1 Conventional Charge Pump

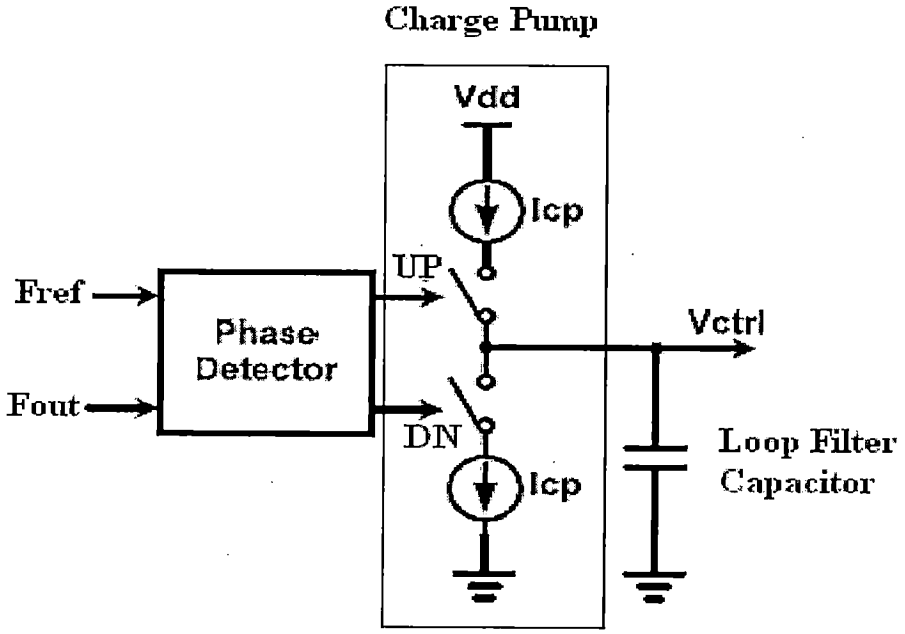



Figure 3.1 Conceptual circuit of charge pump

Figure 3.1 shows the conceptual circuit of the charge pump. It consists of two switched current sources. The current sources are switched by UP/DN pulses from the phase detector. When there is an UP pulse the charge pump pumps in charge to the loop filter capacitor. Similarly, when there is a DN pulse the charge pump pumps out the charge from the loop filter capacitor. This results in a staircase waveform during the transient period. When the PLL is locked, the output voltage remains constant.

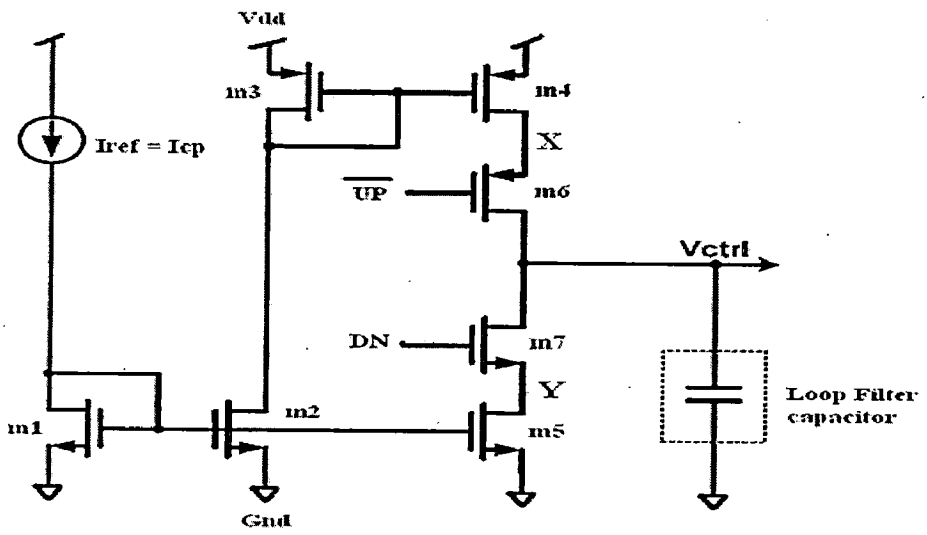



Figure 3.2 Conventional Charge pump

The conventional charge pump is based on the conceptual circuit of figure 3.1 and is shown in figure 3.2. The transistors m6 and m7 acts as switch and transistors m4 and m5 act as a constant current source. The desired value of current is mirrored from $I_{ref}$ via current mirror configuration formed by m1, m2, m5 and m3, m4.

However, the circuit of figure 3.2 shows many non ideal effects like charge sharing, clock feed through and channel charge injection. These phenomenons tend to produce ripples on control voltage line, which is transformed in phase noise and spurious tones in VCO output. The charge sharing is due to balancing of charge between node X, node Y and output voltage Vctrl, when the equal duration UP/DN pulse arrives (during locked state of PLL). Channel charge injection occurs due to flow of part of the channel charge from the channel to the output load capacitor (loop filter capacitor), at the drain terminal. This happens when the MOS switch, in on condition operating in triode region, is suddenly turned off. The magnitude of voltage error is given by



$$\Delta V = \frac{k\,Q_{ch}}{C} = \frac{k\,WL\,C_{ox}\,(Vgs - Vt)}{C} \tag{3.2}$$

Where k is the fraction of channel charge moving to drain, Qch is the channel charge, Cox is the oxide capacitance, Vgs is the gate to source voltage, Vt is the threshold voltage and C is the output capacitance (loop filter capacitance)

Clock feed through results due to non ideal behavior of MOS switches, which presents a parasitic gate to drain capacitance. These errors cause sudden jumps on the control voltage line. The magnitude of the error caused by clock feed through is given by

$$\Delta V = \frac{(V_{dd} - V_{ss})C_{par}}{C + C_{par}} \tag{3.3}$$

Where $V_{dd}$ and $V_{ss}$ are the high and low values of UP/DN signal, $C_{par}$ is the parasitic gate to drain capacitance. In order to minimize the error due to clock feed through, the circuit should be designed carefully enough such that the parasitic capacitance $C_{par}$ is made to be a small fraction of the loop filter capacitance C.

There are some circuit level techniques to suppress the effects due to above mentioned non-idealities. For example in order to suppress the effects due to charge sharing an OP AMP is connected in unity gain configuration and to suppress the effect due to channel charge

injection and clock feed through 'dummy switches' are connected, which creates opposite effect to the one created by UP/DN signal, hence minimize sudden jumps.

Chang and Kuo's model [9] provides one of the best solutions for charge pump design. The circuit eliminates all the non ideal effects completely by isolating the output node from the switching transistors and thus making the output is free from sudden jumps. As the technology node decreases this circuit shows significant mismatch in pump up and pumps down currents. This is due to Channel Length Modulation (CLM) effects which becomes prominent at short channel lengths. The current mismatch further results in static phase error between the inputs when PLL is in locked state.

### 3.2 Charge pump incorporated in the proposed PLL

In order to remove the channel length modulation effects, we have to use the bias generator to generate the bias voltages and then these bias voltages are used to produce the constant current sources. The circuit is as follows.

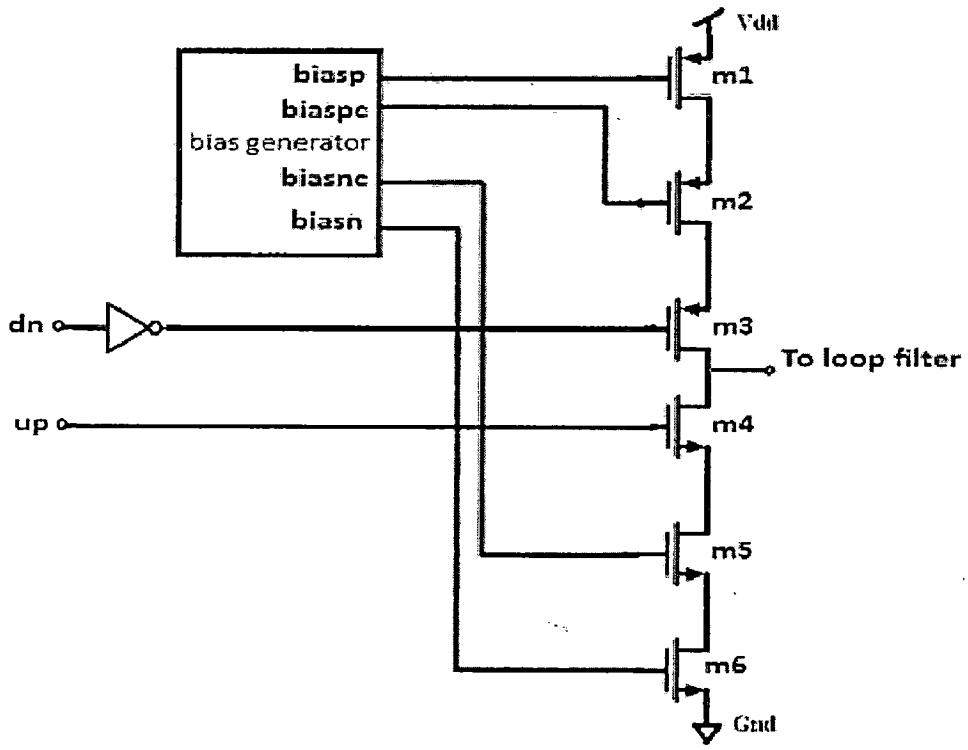



Figure 3.3 Proposed charge pump circuit

Here m1, m2 constitutes the current source and m5, m6 also constitutes the other current source. The bias voltages for these constant current sources come from the bias generator shown in the figure 3.3.

The internal circuit of the bias generator is shown in figure 3.4 and the working and design is also explained. At first for the drain of transistor m9 we have to give minimum voltage and calculate the width and length of the transistor for getting required current 150 μA. Similarly do the same procedure for m14 also.

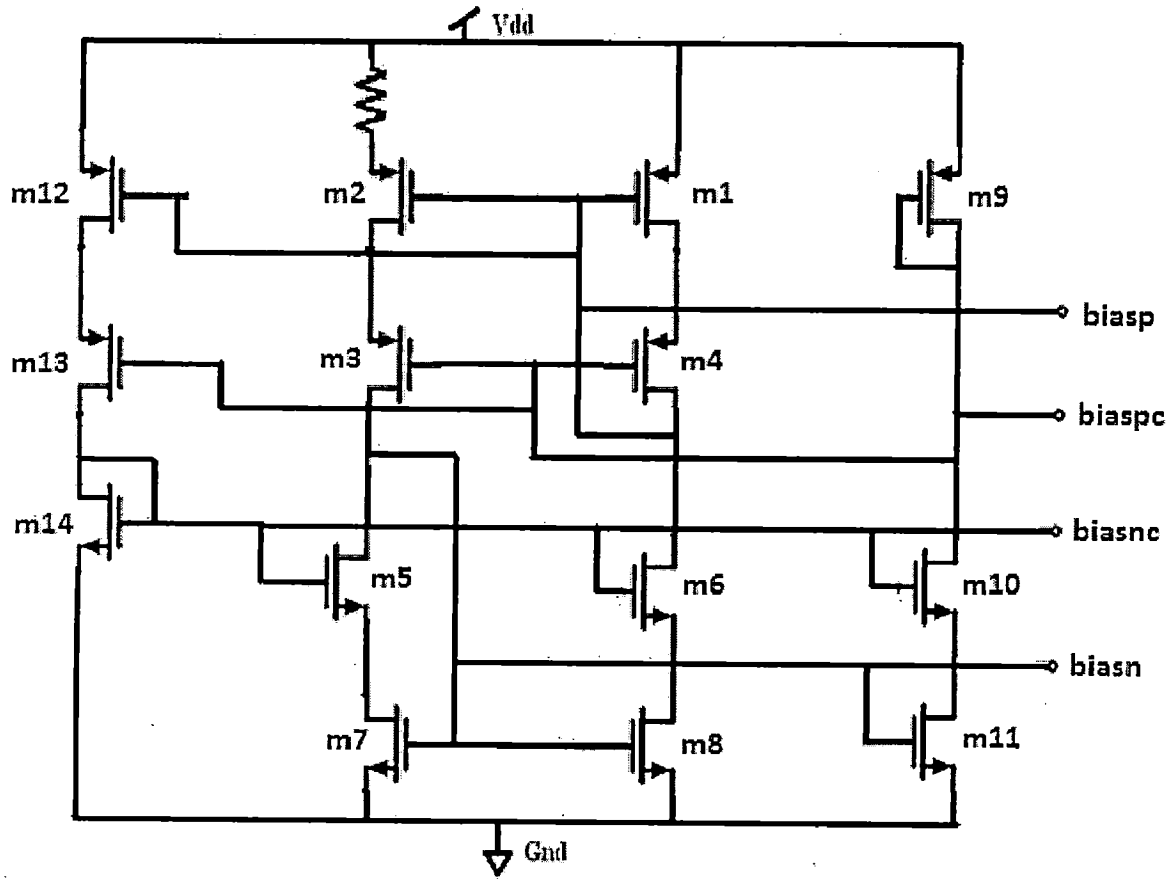



Figure 3.4 Bias generator used in the charge pump

when the simulation is started the m9 and m14 will produce 150 μA current and the gate voltage of m14 is given to m5, m6 and m10. Gate voltage of m9 is given to m3, m4 and m13. The widths of the transistors m5, m6, m7, m8, m10 and m11 should be 6 times that of the transistor m14. The width of the transistors m1, m2, m3, m4, m12 and m13 should be 6 times of the width of the transistor m9. The resistor value should be selected in such a way that the output current must be 150μA when simulated.

Bias voltages biasp and biaspc will come from the gate voltage of m12 and m13 respectively. And the bias voltages biasn and biasnc will come from the gate voltages of m7 and m14 respectively. By using these bias voltages we can make constant current sources.

The simulated output of the pump in current with respect to the output voltage is shown. From this plot we can observe that current is not varying with the output voltage that means the channel length modulation effect is neglected.

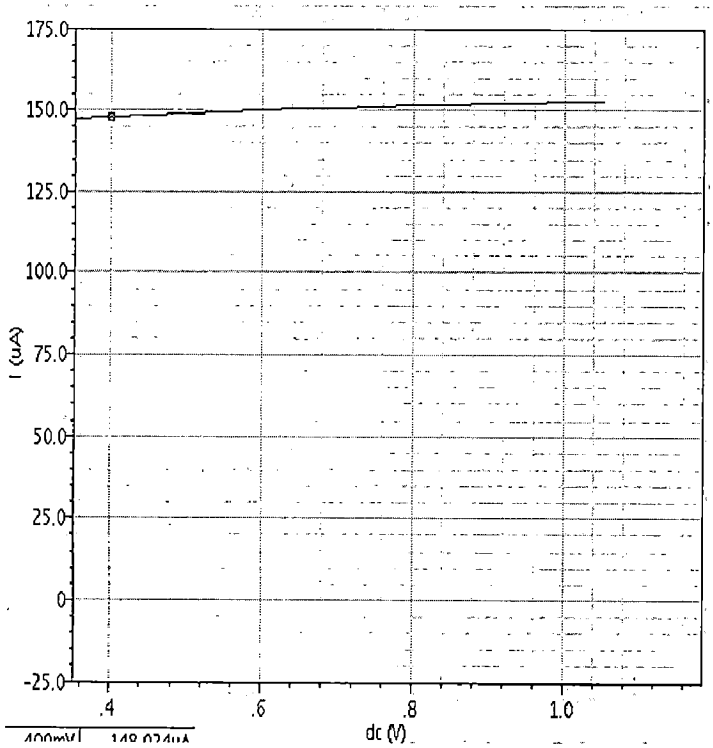
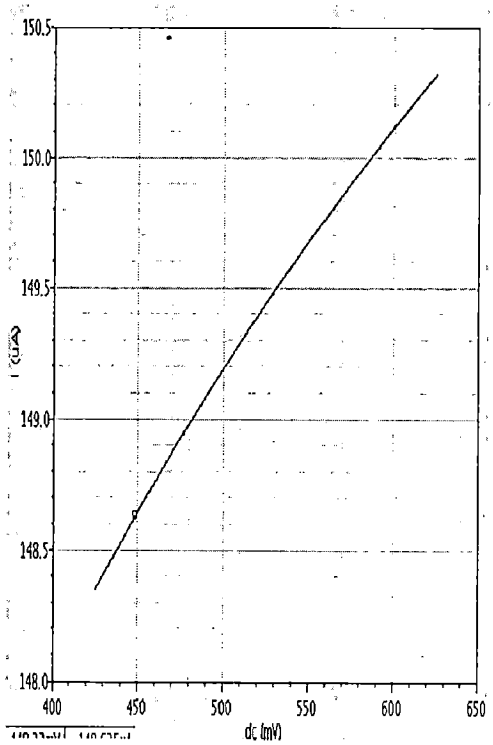



Figure 3.5 Pump out current when dn is high




Zoom in view of the plot

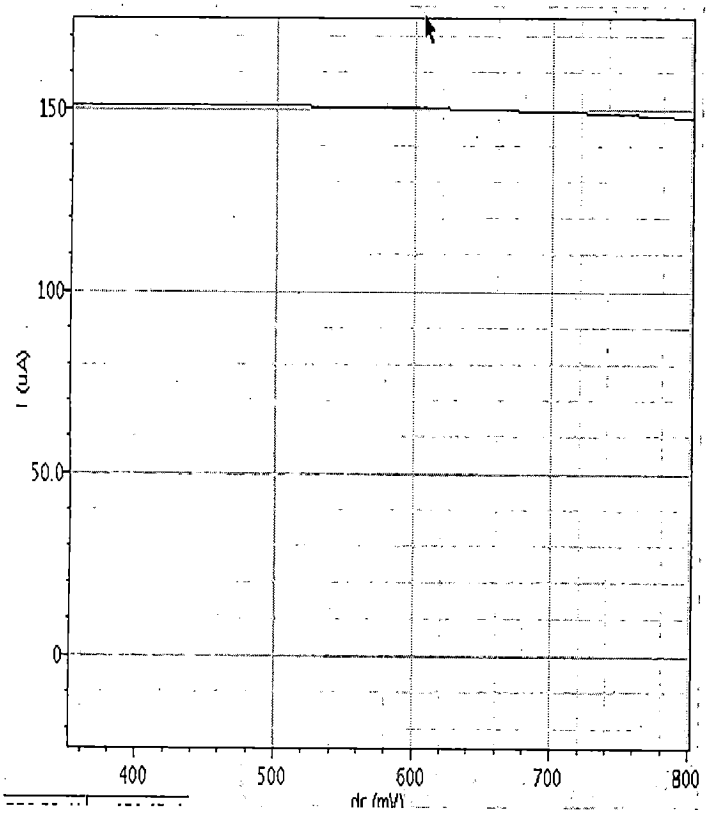
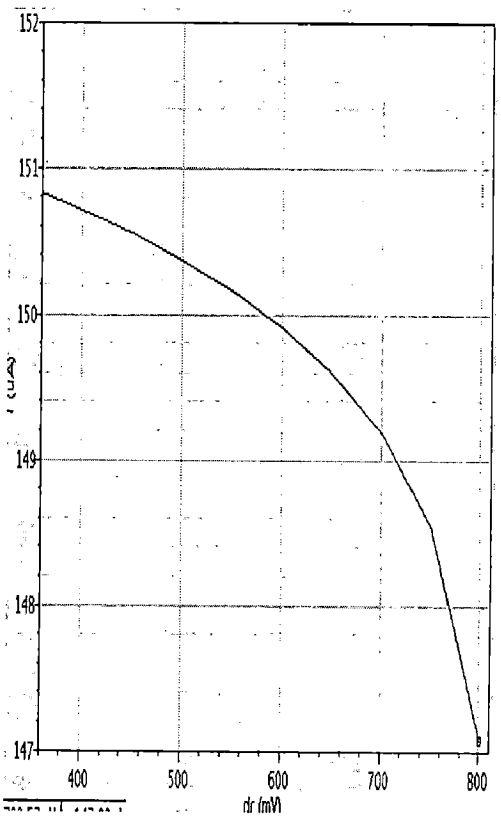



Figure 3.6 Pump in current when up is high




Zoom in view of the plot

The working of the charge pump circuit is explained with the help of the figure 3.3. Transistors m1 and m2 with bias voltages biasp and biaspc will constitute a current source so when the up signal goes high then the transistor m3 will get switched on so the charge will be pumped through m3 into the loop filter capacitor.

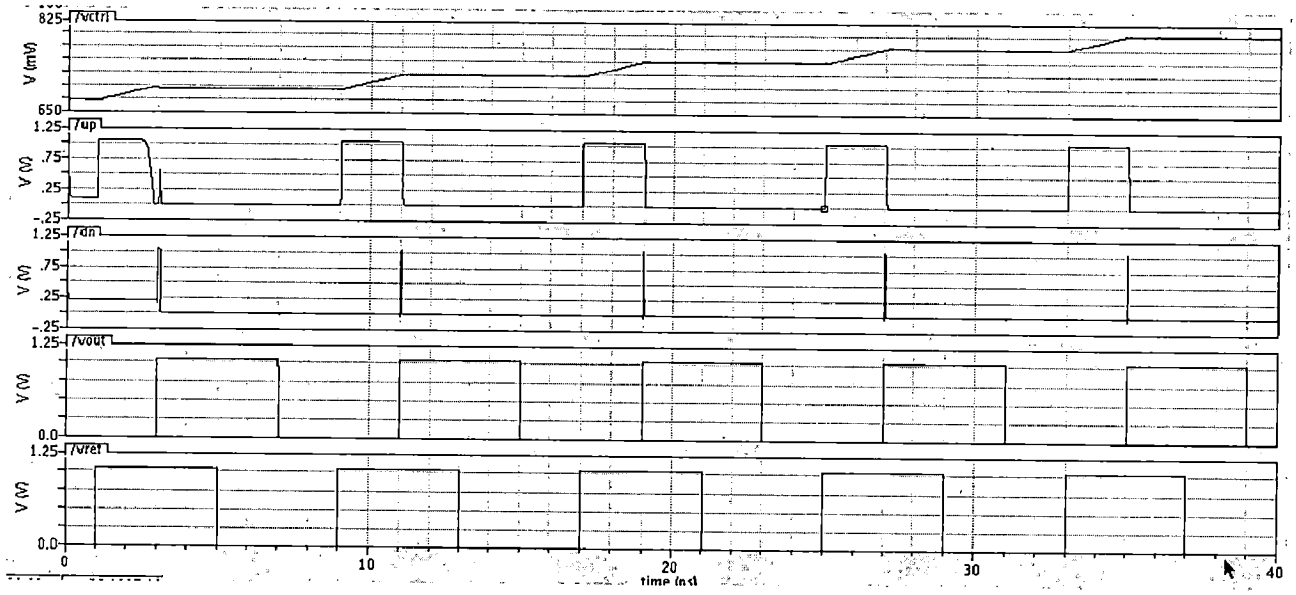



Figure 3.7 The output of control voltage when up signal got activated.

Similarly m5 and m6 with bias voltages biasn and biasnc will constitute a current source so when dn signal goes high then transistor m4 will get switched on then the charge will be pump out of the capacitor.

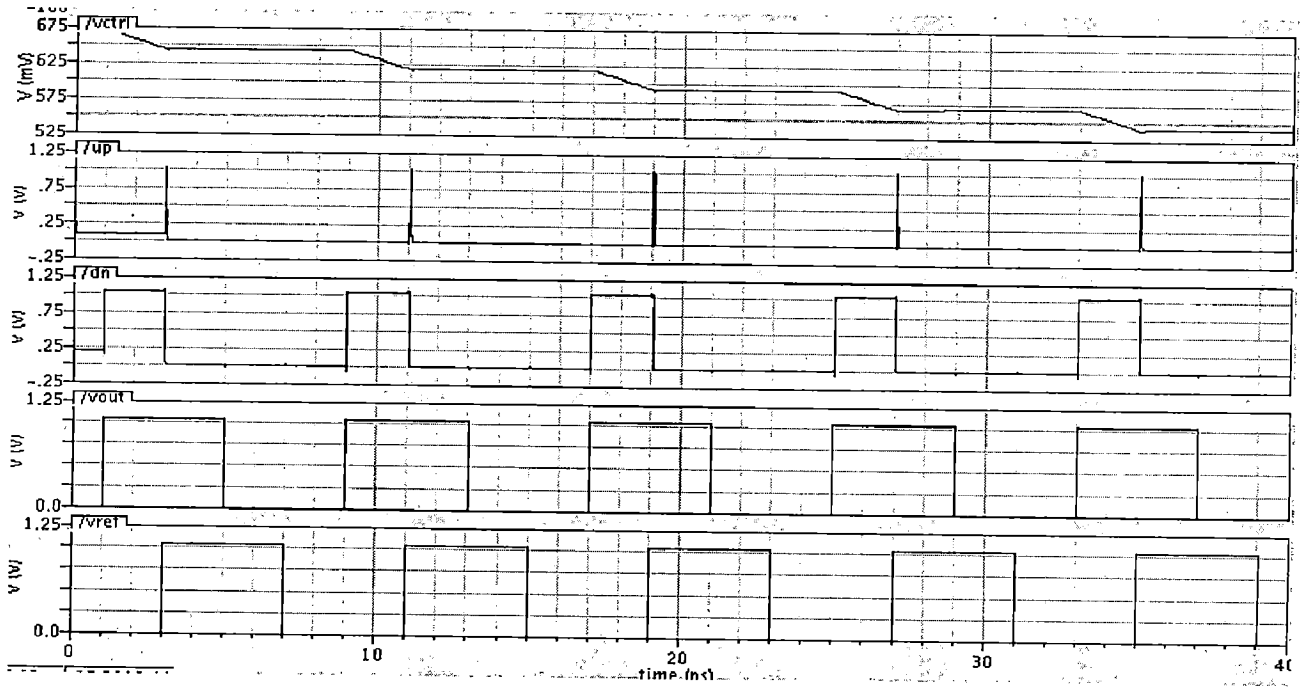



Figure 3.8 The output of control voltage when dn signal got activated.

### 3.3 Loop Filter Design

#### 3.3.1 Linear model of PLL

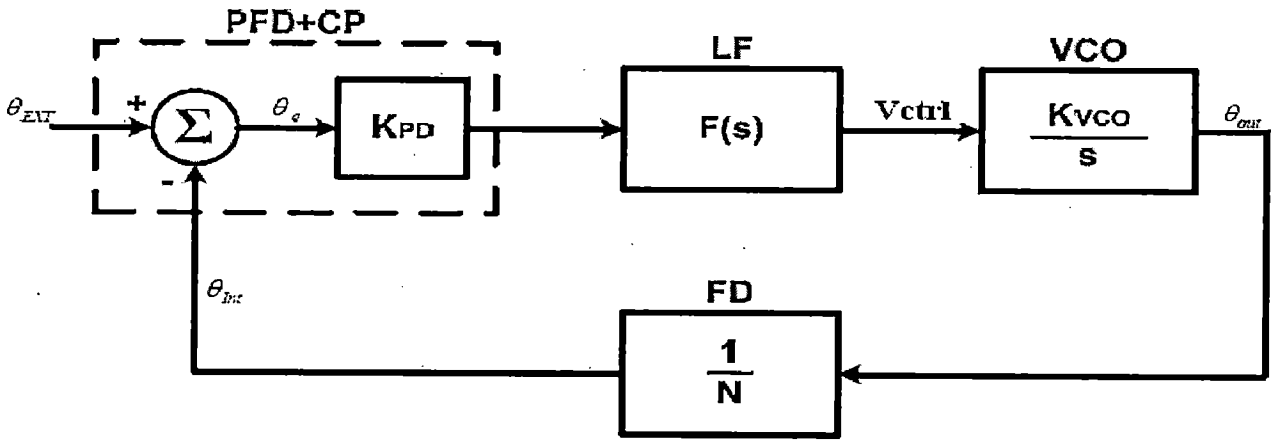



Figure 3.9 Linear model of PLL

The linear mathematical model of a PLL is shown in figure 3.9. Even though PLL is a highly non linear system, it can be approximated to a linear system using continuous time approximation, wherein the sampling nature of the PFD is ignored [11].

In the figure 3.9 $K_{PD}$ is the gain of PFD+CP combination. F(s) is the transfer function of the loop filter. $K_{VCO}/s$ is the transfer function of VCO.

When PLL is in locked state, the phase transfer function is given by:

$$H(s) = \frac{\theta_{out}(s)}{\theta_{Ext}(s)} = \frac{K_{PD}K_{VCO}\,F(s)}{s + K_{PD}K_{VCO}\,F(s)/N} \tag{3.3}$$

If a single capacitor (C) is used as a loop filter (like PLL) the transfer function becomes.

$$H(s) = \frac{\theta_{out}(s)}{\theta_{Ext}(s)} = \frac{K_{PD}K_{VCO}/C}{s^2 + K_{PD}K_{VCO}/CN} \tag{3.4}$$

As seen from eqn. 3.4 the transfer function of the closed loop system has two poles on imaginary axis and hence unstable. It would result in un-damped oscillations at the output and the output will never settle.

A zero added to the above system ( by adding a resistor (R1) in series to loop filter capacitor (C1)) makes the system stable, but cause sudden jumps on the voltage control line, which can further result in potential overload of VCO.

Therefore, to avoid it (sudden jumps), another capacitor (C2) is added in parallel to the series combination of resistor and loop filter capacitor, as shown in figure 3.10.

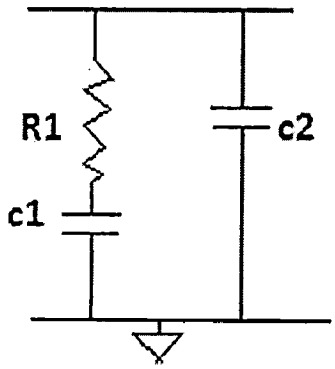



Figure 3.10 Loop filter of PLL

Thus, a PLL requires a minimum of second order loop filter to ensure its stability.

The loop filter is important to the performance of the PLL because

1) Removes high frequency noise of the detector

2) Influences the capture and tracking ranges

3) Influences the switching speed of the loop in lock.

4) Easy way to change the dynamics of the PLL

We will consider the filters that give us more flexibility in controlling the characteristics of the PLL. Filters are of two types: passive filters and active filters.

The advantages of the passive filters are they are linear, relatively low noise and unlimited frequency range. We have some disadvantages also in using the passive filters. If the filter components are larger in value(c>200pF and R>100kohm) then they are hard to integrate. Another disadvantage is it is difficult to get a pole at the origin (increase the order of the type of PLL). In order to remove the drawbacks of passive filters we will go for the active filters. Active filters can reduce the sizes of the passive elements but the disadvantages are they will produce more noise, consume more power and it has some frequency limitations.

The loop filter component values are R1 is 500 ohms, capacitor c1 is 100pF and c2 is 10pF. Generally the ratio of c1/c2 should be 10.

# 4 VOLTAGE CONTROLLED OSCILLATOR

Voltage controlled oscillators are one of the important blocks of data communication systems and have wide applications, from data modulating in transmitters to demodulation and clock recovery in receivers. A CMOS VCO can be built using ring structures, relaxation circuits, or an *LC* resonant circuit. Ring inverter based oscillators have some advantages among the other oscillators that have made them a good choice for designers.

Compared to other alternatives, especially the LC resonator-based oscillators, the ring oscillator are having the following advantages.

- The ring oscillator is compact, as it doesn't need on chip inductors [10].
- Its tuning range can span orders of magnitude as the ring oscillator is tuned by voltage.

Meanwhile, it is desirable to scale down the current consumption of the VCO proportional to frequency variations which can be reached using ring oscillators. However, ring oscillators suffer from low Q factor and consequently larger phase noise. Ring oscillators with differential delay stages exhibit greater immunity to supply disturbance and substrate induced noise than single delay stage ones.

## 4.1 The most important specifications of the VCO

**Electrical tuning range:** the tunable frequency range of the VCO must be able to cover the entire required frequency range of the interested application.

**Tuning linearity**: An ideal VCO has a constant VCO gain, $\mathbf{K_{vco}}$ at the entire frequency range. A constant VCO gain can simplifies the design procedure of a PLL.

**Supply voltage sensitivity**: Since there are many digital circuits in a modern transceiver circuit, the switching activities of the digital circuits will influence the supply voltage, $V_{dd}$, of the whole system [3]. Besides, the switching noise will also couple to $V_{dd}$ of the VCO and influence its output waveform. Therefore the dependency of the VCO oscillation frequency on the supply voltage must be as low as possible.

**Power consumption**: The VCO at high frequency has large dynamic power consumption and at low frequency, has large short-circuit power consumption. The main power consumption of the PLL comes from the VCO, so reducing the power of the VCO is very important.

According to above analyses, when we design the circuit of the VCO, we should pay attention to the main problems of the tuning range, noise, power consumption and linearity.

### 4.2 Ring oscillator architecture

The ring oscillators consist of delay cells connected in cascade as shown in figure 4.1. These are connected in a closed loop for providing enough gain and phase shift to satisfy the Bark hausen's oscillation criteria [17].

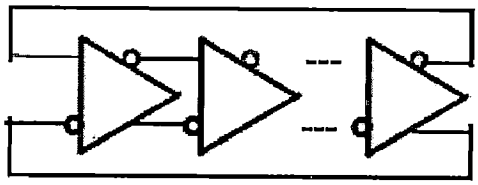


Figure 4.1 Basic structure of the ring oscillator

In these topologies the oscillation frequency is given as

$$f = \frac{1}{2N\tau_d} \tag{4.1}$$

Where $N$ is the number of delay cells in the ring and $\tau_d$ is the delay time in the cell. Eqn. 1 shows that the increase of the oscillators speed can be realized by two ways: through the reduction of the delay time in the cell or by decreasing the number of cells in the ring.

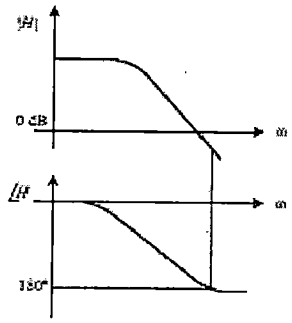


Figure 4.2 problem of insufficient gain

The reduction of the number of cells is very attractive not only for the operation speed increment but for the power consumption reduction and the saving in area for its implementation. However, as $N$ diminishes it is more difficult to satisfy the Barkhausen's oscillation criteria: *the steady oscillation in a ring oscillator requires a total phase shift of 360° around the loop at a frequency where the small signal gain is above 0 dB.*

In $N$ cells ring oscillator, each cell contributes with a frequency dependent phase shift of $180°/N$ and the *dc* phase shift provides the 180° remaining. For small $N$ the problem of insufficient gain (or insufficient phase shift) arises. Insufficient gain means that at the frequency where the frequency-dependent absolute phase shift reaches 180°, the loop gain is less than 0 dB, in other words, the crossover points of the phase (-180°) and the unity loop gain are different and the oscillation criteria cannot be met simultaneously, as is shown in figure 4.2.

In this project, a new differential ring oscillator with new composite load is proposed, resulting in relatively higher frequencies and wider tuning ranges. Figure 4.3 shows the schematic of delay stage.

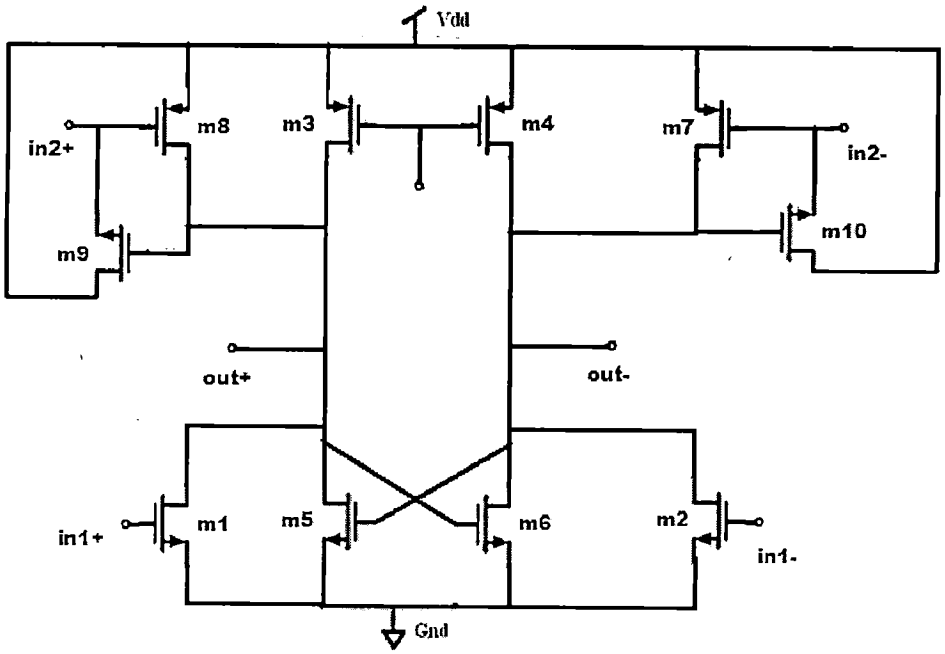



Figure 4.3 delay stage cell schematic in VCO

In this delay stage, the nmos transistors m1 and m2 create the input pair for primary loop, while the pmos transistors m7 and m8 form the input pair for secondary loop. The proposed differential ring oscillator uses composite load (m8 & m9- m7 & m10) and feed-forward technique to reduce the delay of each cell. The transistors m3 and m4 are utilized to control the frequency of operation by varying their gate voltage. Applying control voltage to pmos transistors helps avoiding tail current control mode and increasing output voltage swing and reducing 1/f noise. Furthermore, single control voltage relaxes the implementation of charge pumps and loop filters in the PLLs. The size of m3 and m4 determines the tuning range. The

single control voltage also eases the implementation of the charge pump and loop filter within the PLL.

The nmos transistors m9 and m10 are used as a load besides m8 and m7 to create a composite load, showing inductive impedance at the drain of m7 and m8. This new load helps the cell to oscillate at higher frequency and reaches wider tuning ranges. As shown in Figure 4.4, considering the gate source capacitance of m8 we have:

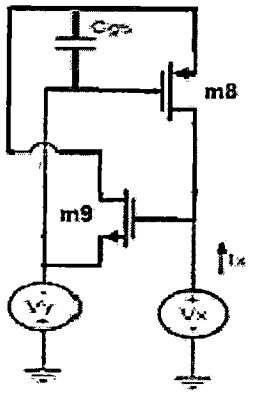



Figure 4.4 Load used in proposed ring oscillator showing inductive impedance

Therefore, the impedance at the drain of M3 is always inductive. Its magnitude can be changed by varying the widths of M7 and M8.

$$\frac{V_Y}{V_X} = \frac{\frac{1}{SC_{GS8}}}{\frac{1}{SC_{GS8}} + \frac{1}{g_{m9}}} = \frac{g_{m9}}{g_{m9} + SC_{GS8}} (\gamma = lambda = 0) \tag{4.2}$$

$$\frac{I_X}{V_X} = \frac{g_{m8}g_{m9}}{g_{m9} + SC_{GS8}} \tag{4.3}$$

$$\frac{V_X}{I_X} = \frac{1}{g_{m9}} + \frac{C_{GS8}}{g_{m8}g_{m9}}S \tag{4.4}$$

Therefore, the impedance at the drain of m8 is always inductive. Its magnitude can be changed by varying the widths of m9 and m10. Considering that the nmos switches faster than the pmos, a cross coupled nmos pair m5 and m6, is introduced at between the outputs to provide the essential self-balancing of the delay cell to prevent the differential ouputs from settling to the same voltage. In addition to that, the cross-coupled nmos pair can also help to

improve the phase noise performance of the oscillator by a significant amount since the positive feedback within the delay cell provided by this nmos pair helps to reduce the transition time of the output nodes.

### 4.3 High speed ring oscillator with dual delay paths

In a conventional ring oscillator, the oscillation frequency is determined as$1/2N\tau$, where N is the number of stages and $\tau$ is the unit delay time of a delay cell. Hence the frequency of the oscillator is decided by the delay time of one delay element. The delay time cannot be smaller than that of a single inverter; therefore, the maximum frequency of the VCO is limited by the delay time of the basic inverter delay cell.

To solve this frequency-limitation problem, a single-ended ring oscillator with a negative skewed delay scheme has been used [16]. If the delay cell is single ended, and the oscillator is sensitive to the power-supply noise and not controllable. In this work, by using a dual-delay scheme to implement the VCO, higher operation frequency and wider tuning range are achieved simultaneously. The dual-delay scheme means that both the negative skewed delay paths and the normal delay paths exist in the same ring oscillator. The negative skewed delay paths decrease the unit delay time of the ring oscillator below the single inverter delay time. As a result, higher operation frequency can be obtained. Since the normal delay paths also exist, the frequency range of the VCO can be wider than that of an oscillator with only skewed delay paths.

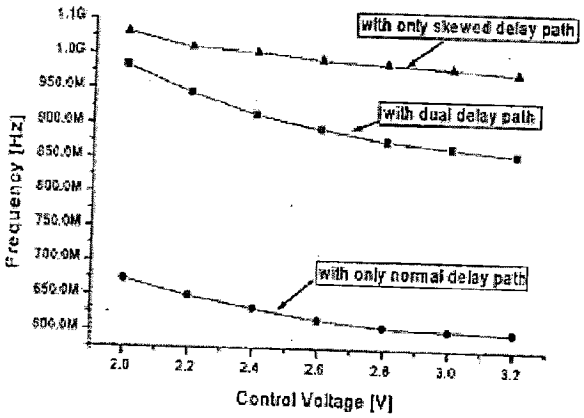



Figure 4.5 simulation results of three types of VCO's

Figure 4.5 shows the simulation results of the three types of VCO, with dual-delay path, only normal delay path, and only negative skewed delay path. The same types of delay cells are

used to implement the VCO's. The figure shows that the dual delay scheme achieves both a high oscillation frequency and a wide tuning range.

To utilize both the negative skewed and the normal delay paths, a pair of PMOS transistors, are added to the PMOS loads of the delay cell and are used to take the negative skewed signals, as shown in figure 4.3.

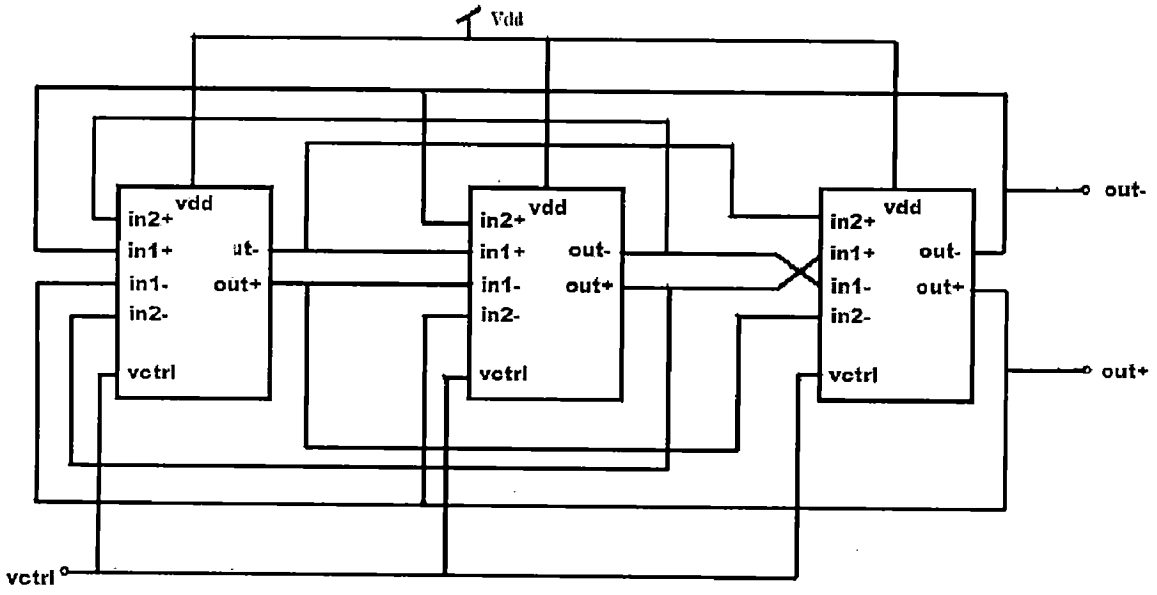



Figure 4.6 ring oscillator structure with dual delay paths

The negative skewed signal is connected to the PMOS input of the delay cell, and the normal signal is connected to the NMOS input of the delay cell. The negative skewed signal is taken from the two stages before the current delay stage. The signal prematurely turns on the PMOS during the output transition and compensates for the performance of the PMOS, which is usually slower than that of the NMOS. This operation enhances the rise time of the output and contributes to reducing the phase noise of the overall VCO. In figure 4.6, the negative skewed delay paths are the paths which are coming from the outputs to the inputs of in2+ and in2-, and the normal delay paths are the paths which are coming from outputs of previous stage to the inputs in1+ and in1-.

Figure 4.7 illustrates the tuning characteristics of proposed VCO. Changing the control voltage between 425mV-625mV, the frequency varies between 6.8GHz - 3.7 GHz in differential voltage controlled ring oscillator. It shows linear characteristics and wide tuning range of oscillator. The VCO gain is 18GHz/v.

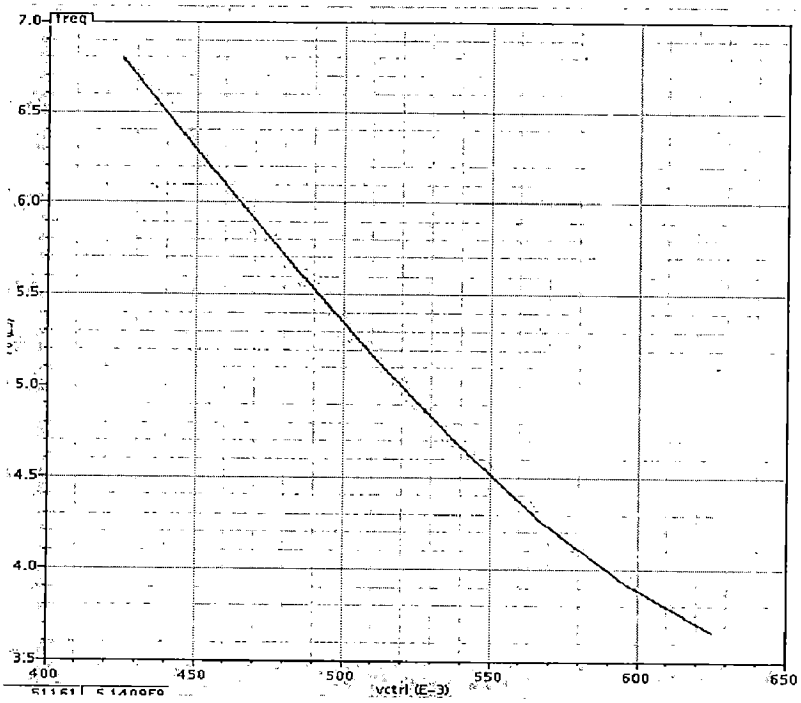



Figure 4.7 Frequency sweep with control voltage in differential oscillator

Figure 4.8 shows the duty cycle of the output waveforms as control voltage is varying.

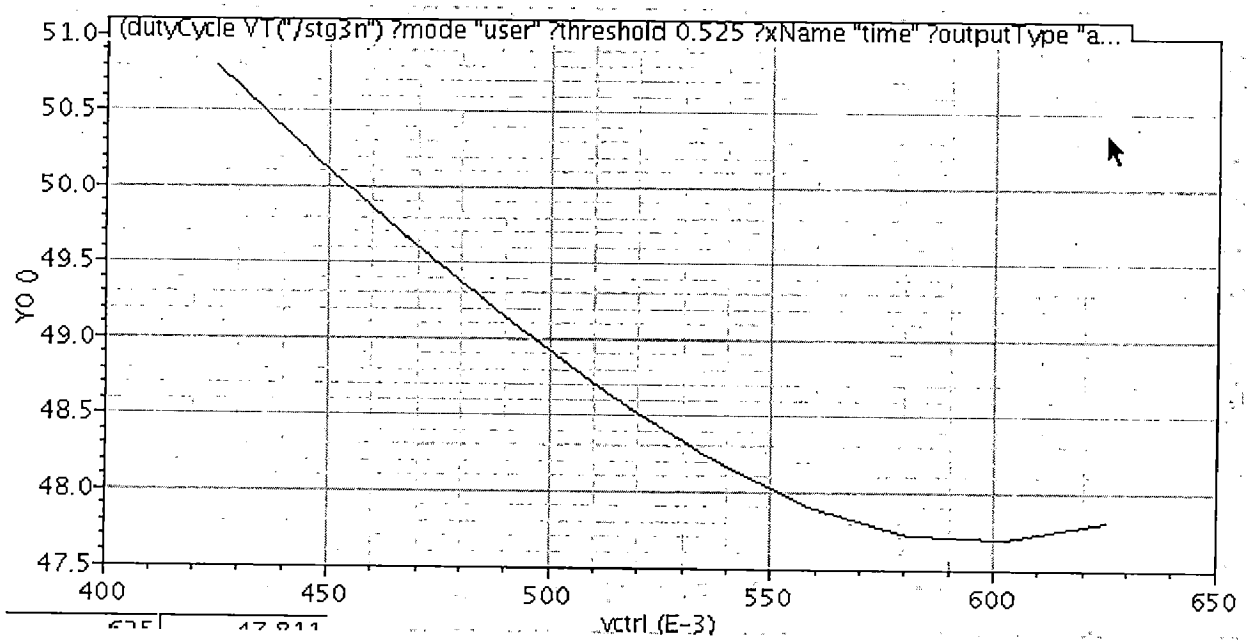



Figure 4.8 Duty cycle variation with control voltage

Figure 4.9 is the plot of output waveforms of the VCO for different control voltages. From this we can understand that as the control voltage is increasing the VCO is taking more time to change the states that means the frequency is decreasing.

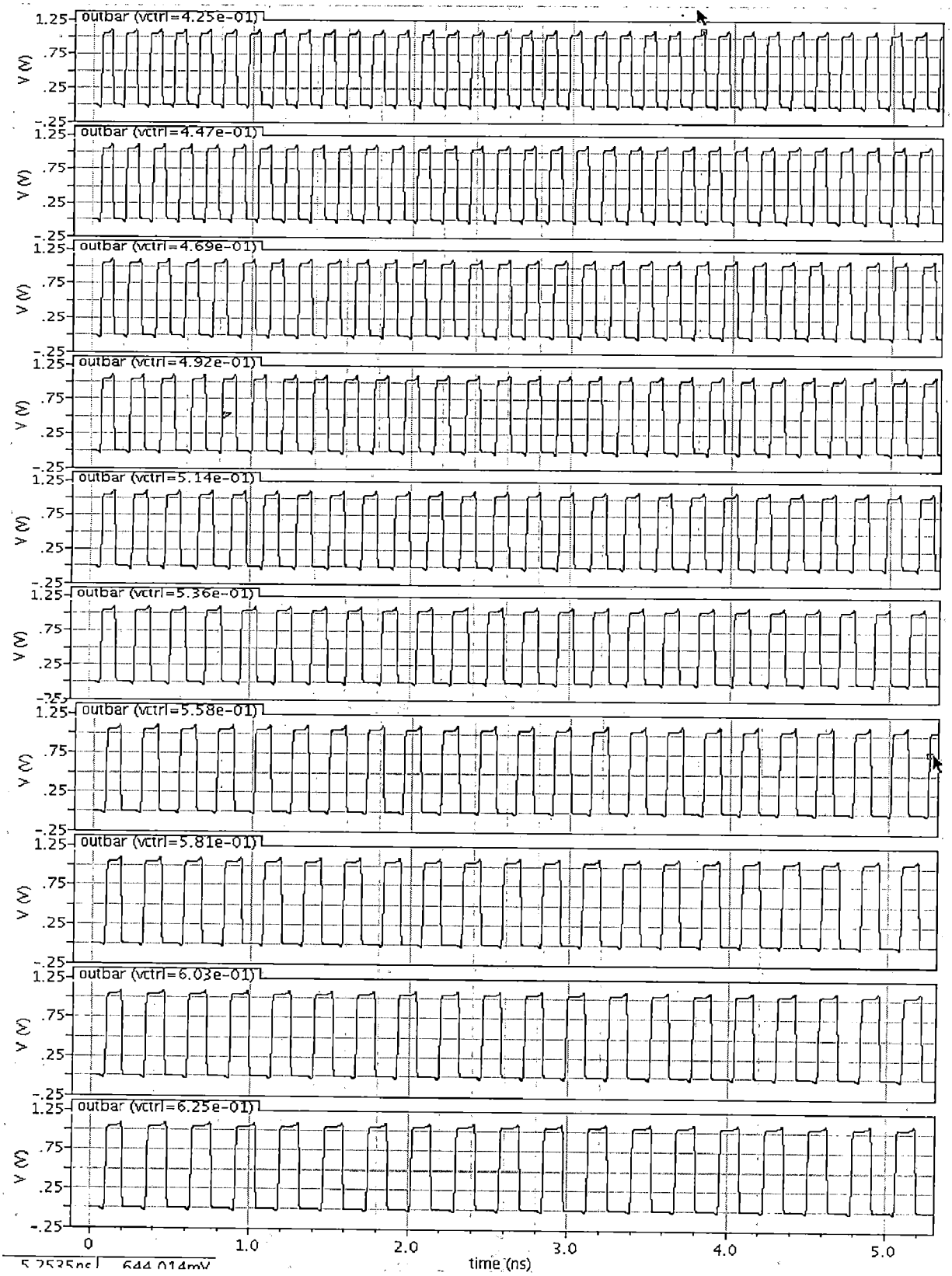



Figure 4.9 output waveforms of the VCO for different control voltage

## 4.4 FREQUENCY DIVIDER

The frequency divider is an important building block in today's RFIC and microwave circuits because it is an integral part of the phase-locked loop (PLL) circuit. In a typical PLL loop, the output of the voltage-controlled oscillator (VCO) is divided down by the frequency divider to a stable reference frequency signal produced by the crystal oscillator. The divided signal and reference frequency signal are fed into the phase detector for comparison. The output phase difference is used to adjust the VCO output frequency.

### 4.4.1 Digital dividers

To divide a digital signal by an integer multiple a Johnson counter is used. This is a type of shift register network that is clocked by the input signal. The last register's complemented output is fed back to the first register's input. The output signal is derived from the combination of the register outputs. For example, a divide-by-3 divider can be constructed with a 3-register Johnson counter. The three valid values for each register are 000, 100, 110, 111, 011, and 001. This pattern repeats each time the network is clocked by the input signal. The values 000 and 111 occur with three clock pulses apart and control the state change of the output signal. Additional registers can be added to provide additional integer divisors.

For power-of-2 integer division, a simple binary counter can be used, clocked by the input signal. The least-significant output bit alternates at the same rate as the input, the next bit is the 1/2 the rate, the third bit is 1/4 the rate, etc. An arrangement of flip-flops is a classic method for integer-n division. Such division is frequency and phase coherent to the source over environmental variations including temperature. The easiest configuration is a series where each flip-flop is a divide-by-2. For a series of three of these, such system would be a divide-by-8. By adding additional logic gates to the chain of flip flops, other division ratios can be obtained.

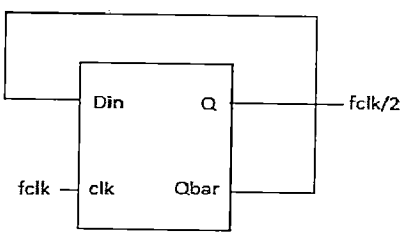



Figure 4.10 Divide by 2 frequency divider

In the figure 4.1 we give a frequency divider which divides the frequency by two. It is implemented using only one D flip-flop.

It is essentially an edge triggered master/slave D flip-flop (DFF). The inverted output is fed back to the input port D. As shown in Figure 4.2, each positive input clock cycle is loaded into the DFF. On the next cycle, inverted output again is fed back to the input, which causes the output to toggle. It is why toggle DFF is a more descriptive name for this circuit. The same event repeats for every two input clock cycle. Thus, output frequency is half of the input frequency.

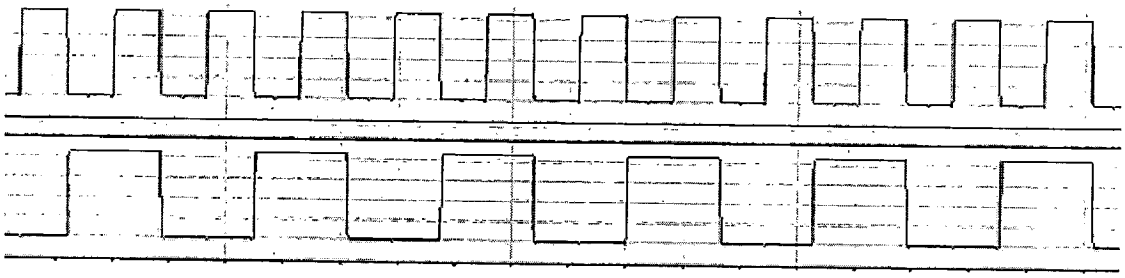


Figure 4.11 Divide by 2 frequency divider output

Now we will see the implementation of the D flip flop. The proposed DFF uses two sets of clocks. The clocks applied on transmission gates M1 and M3 are denoted clk and clkbar, and the clocks applied on gates *M2* and *M4* are denoted clk_d and clkbar_d clocks are generated by delaying clocks clk and clkbar, respectively, with two stages of inverters [13].

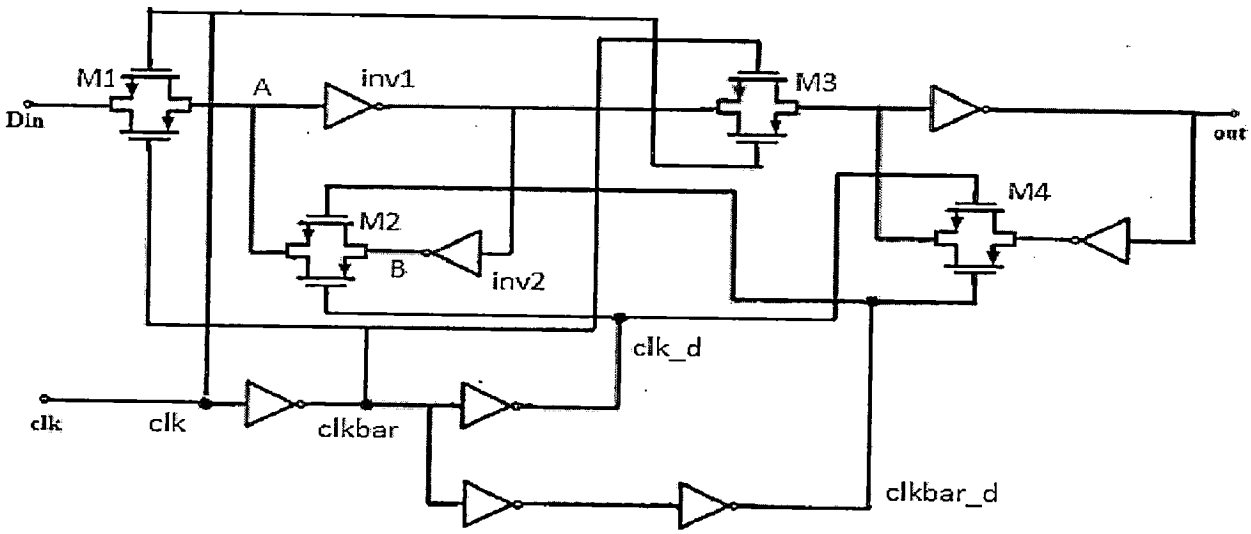



Figure 4.12 D Flip flop

Now we will see the implementation of the D flip flop. The proposed DFF uses two sets of clocks. The clocks applied on transmission gates M1 and M3 are denoted clk and clkbar, and the clocks applied on gates M2 and M4 are denoted clk_d and clkbar_d clocks are generated by delaying clocks clk and clkbar, respectively, with two stages of inverters.

The proposed static DFF has a reduced setup time compared to that of a conventional static DFF. In the conventional static DFF we will not have two clocks, but in our proposed D flip flop we have two clocks. Let us see what happens if we use same clock that is instead of clk_d we use clk signal only.

When the clock clk is high, the data *D* is loaded to node *A* and stored in the first memory unit composed of inverters inv and inv2. When the clock clk goes low, the data stored in the first memory unit is propagated to the output terminal. In order for the DFF to function correctly, a sufficiently large setup time is required to allow the new data to be propagated to node *B*, through the path of node *A*, inv1, and inv2.

If the clock is too fast, the DFF will not have sufficient setup time and the following scenario might cause the DFF to not function correctly. Assume that the clock is high and the input data changes from low to high, then the signal at node *A* will change from low to high. At this moment, due to the delay of inverters inv1, and inv2, node *B* is still in the previous state. If the clock goes high before node *B* changes to the present state, the transmission gate M2 will be closed, causing the data previously stored at node *B* to be propagated to node *A*. If the previous data is different from the new data, they will 'fight' with each other. Since the transmission gate M1 is now open, the final state of node *A* is uncertain and the DFF may function incorrectly.

The proposed design uses two sets of clocks on gates M1 and *M2.*When clock clk, is high, the new data is propagated to node *A* through M1. Then, as soon as the new data is propagated to the output of INV1, the clock can go low and the new data can be propagated to the output of the DFF. Since clock clk_d is the delayed version of clock clk, when clock clk goes high, clock clk_d is still low. Thus gate M2 is still open and the previous data stored at node *B* cannot be propagated to node *A* through M2. The 'fighting' condition between the new data and the previous data is then avoided. As a result, the setup time of the proposed DFF is reduced.

Simulation results of the proposed D flip flop:

Setup time of the flip flop = 50 ps

Hold time of the flip flop = 22 ps

In the proposed PLL we have used 6 bit frequency divider. Let us suppose the frequency of the clock given to the first D flip flop is " f " then the output of that flip flop is coming out to be the half of the frequency of the input clock i.e. f/2. This output is given to the next flip flop as clock then the frequency of output of the second flip flop will the half of the input clock i.e. f/4. This output is given to third flip flop then the frequency of the output of that flip flop will be f/8. Like this the output of the forth flip flop is f/16, output of fifth flip flop is f/32 and the output of the sixth flip flop is f/64. In this way our frequency divider will produce the output frequency which $1/64^{th}$ of the input frequency.

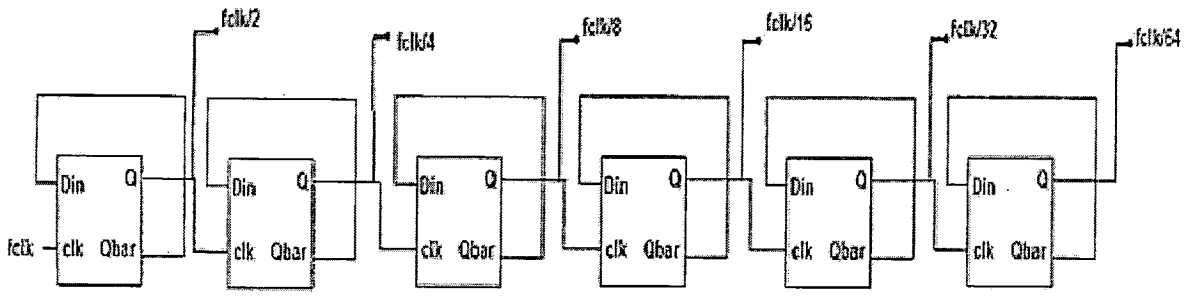



Figure 4.13 Proposed 6 bit frequency divider

The output waveforms of the frequency divider are shown below.

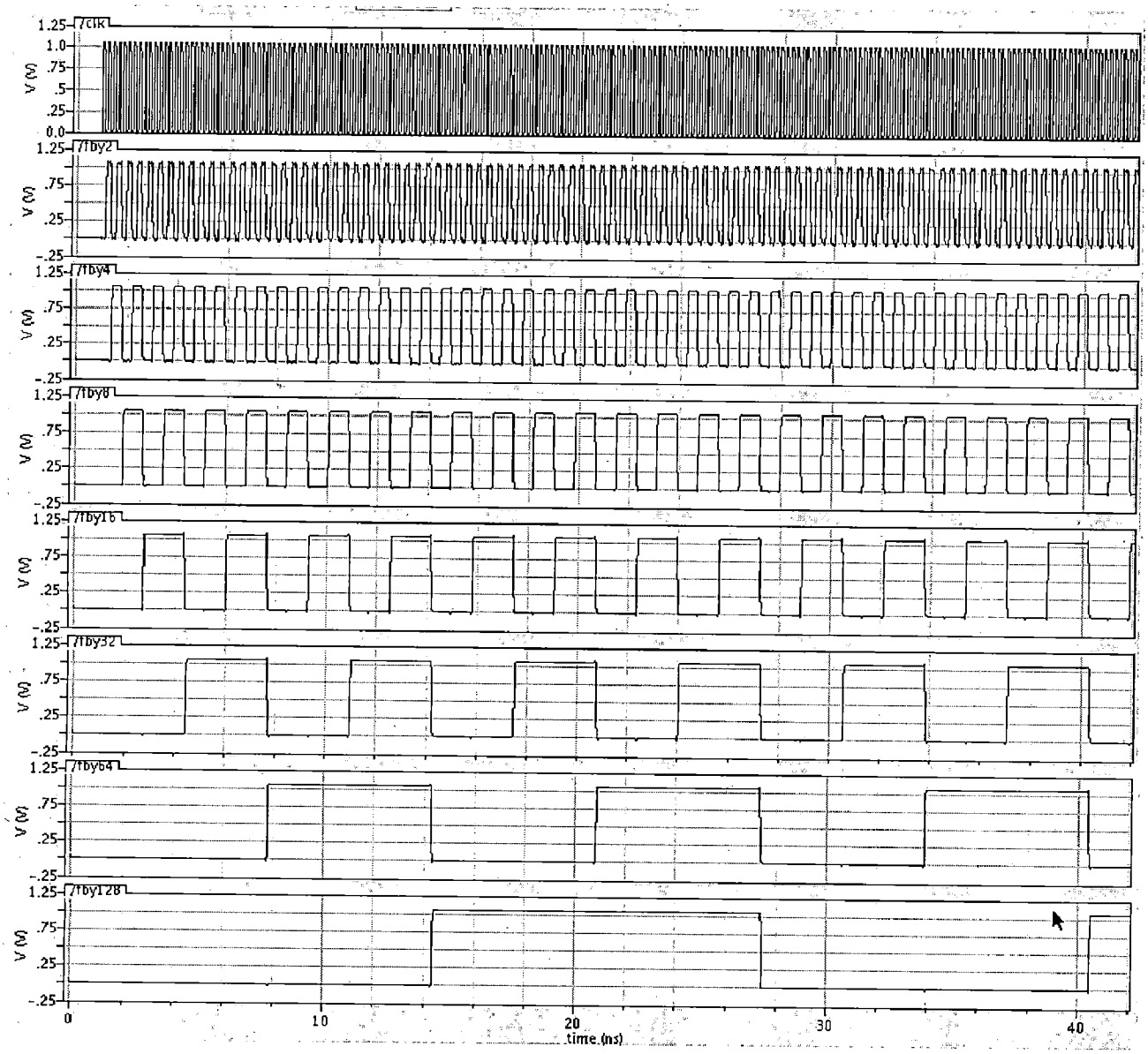



Figure 4.14 Output waveforms of the frequency divider

# 5 SIMULATIONS AND CONCLUSION

Full loop simulation of the proposed PLL is shown in the following figure 5.1. Initial control voltage given at the starting of the simulation is Vdd. So as the reference frequency is 100MHz and the frequency divider is 6 bit, the output frequency of the VCO should be 6.4GHz. So the control voltage should get settled to a specified value such that the output frequency of VCO is 6.4GHz.

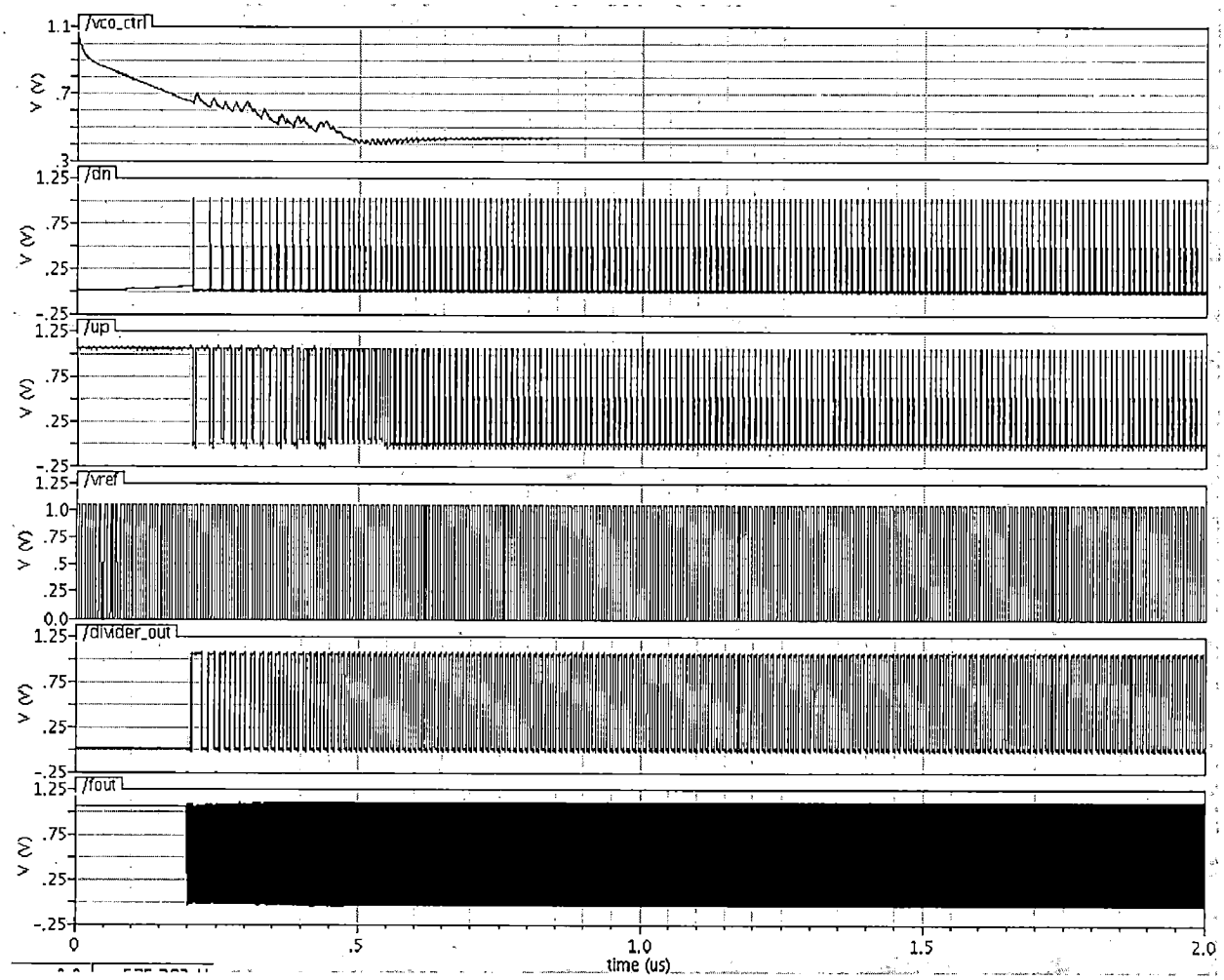



Figure 5.1 Full loop simulation of the PLL

When the PLL is in locked state the control voltage should be stabilized to a constant value which is clearly shown in the figure 5.2. The control voltage got stabilized to 435mV after time of 0.45µs. The time taken by the PLL to get lock to a new specified frequency is called lock time. So the lock time of the PLL is 0.45µs.

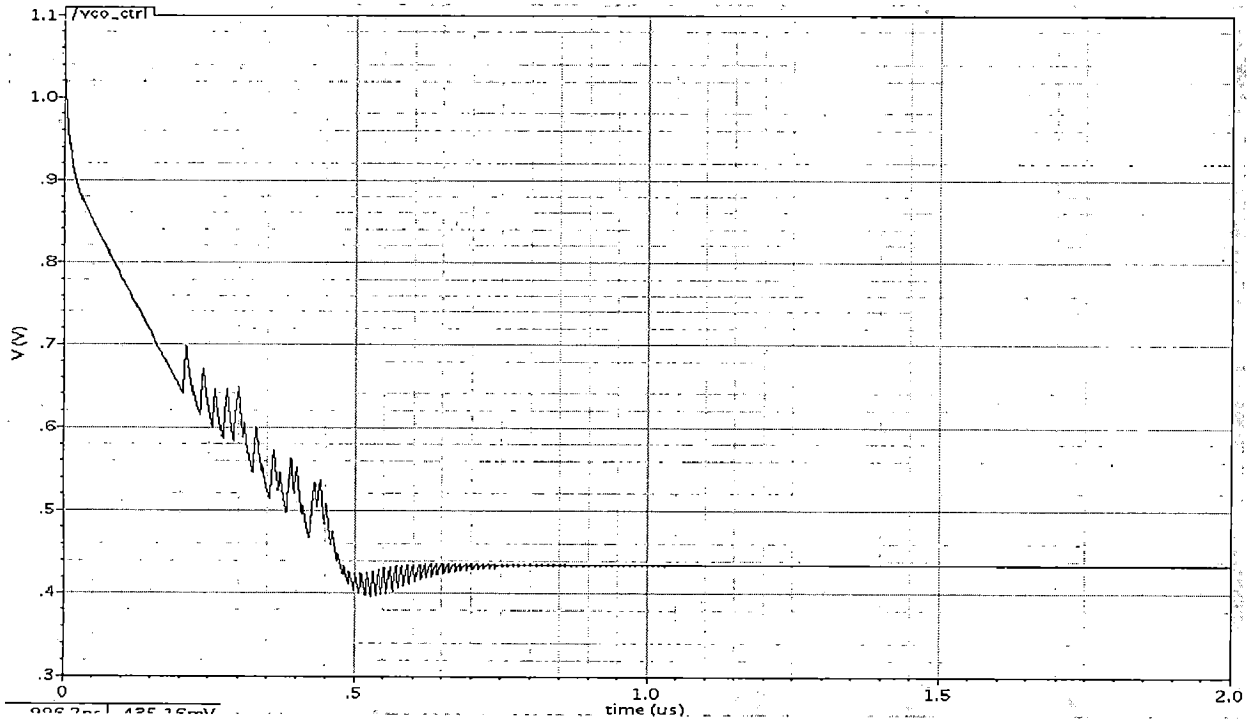



Figure 5.2 control voltage to VCO

The ripple on the control voltage is 1.17mV as shown in the figure 5.3.

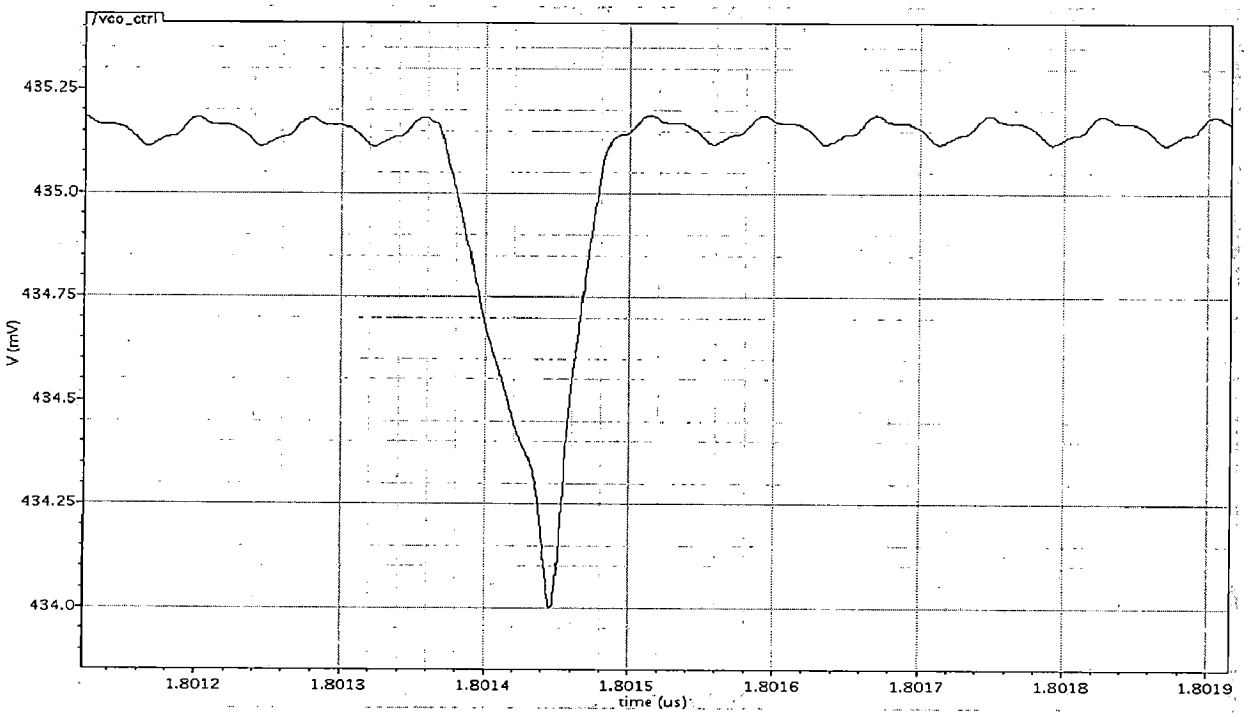



Figure 5.3 ripple on control voltage

When the PLL is in locked state the reference frequency and the feedback signal i.e. the output frequency of the frequency divider should be in phase. This is clearly shown in the figure 5.4.

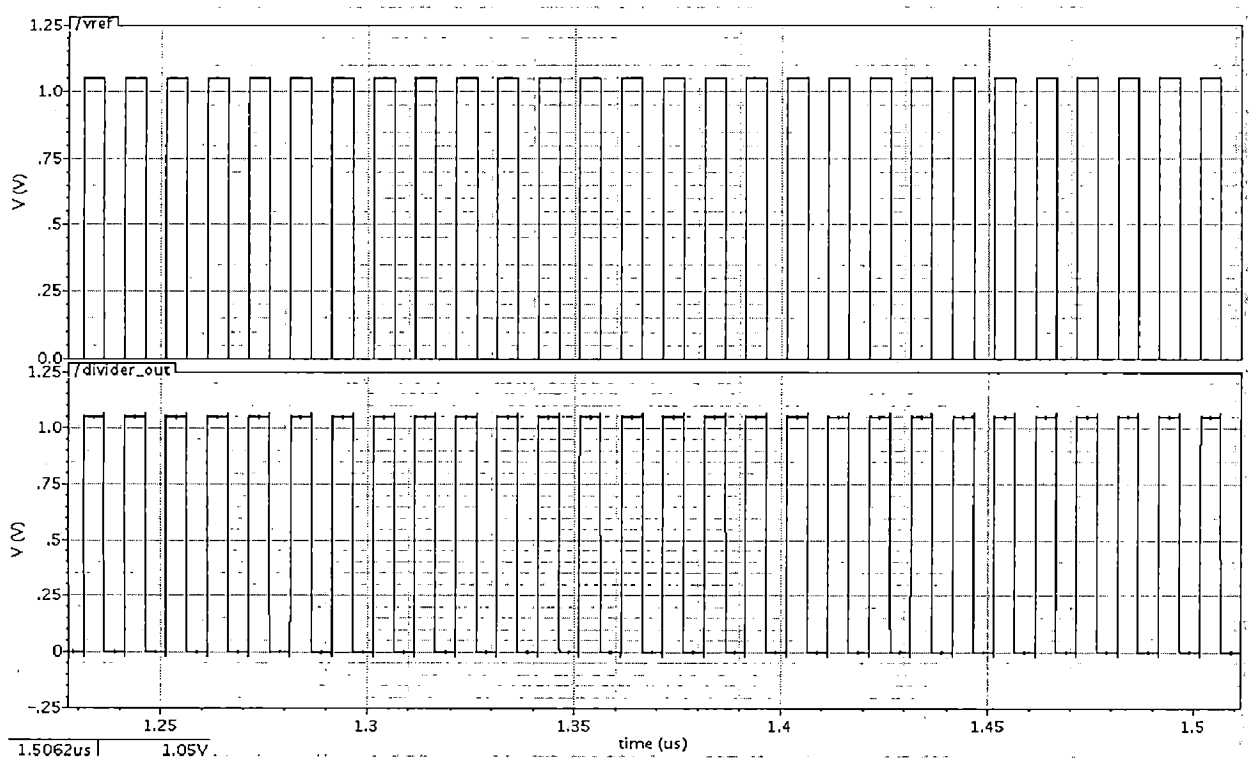



Figure 5.4 reference signal and divider output signal in locked state

The phase difference between the reference frequency and the feedback signal is 57 ps as shown in the figure 5.5.

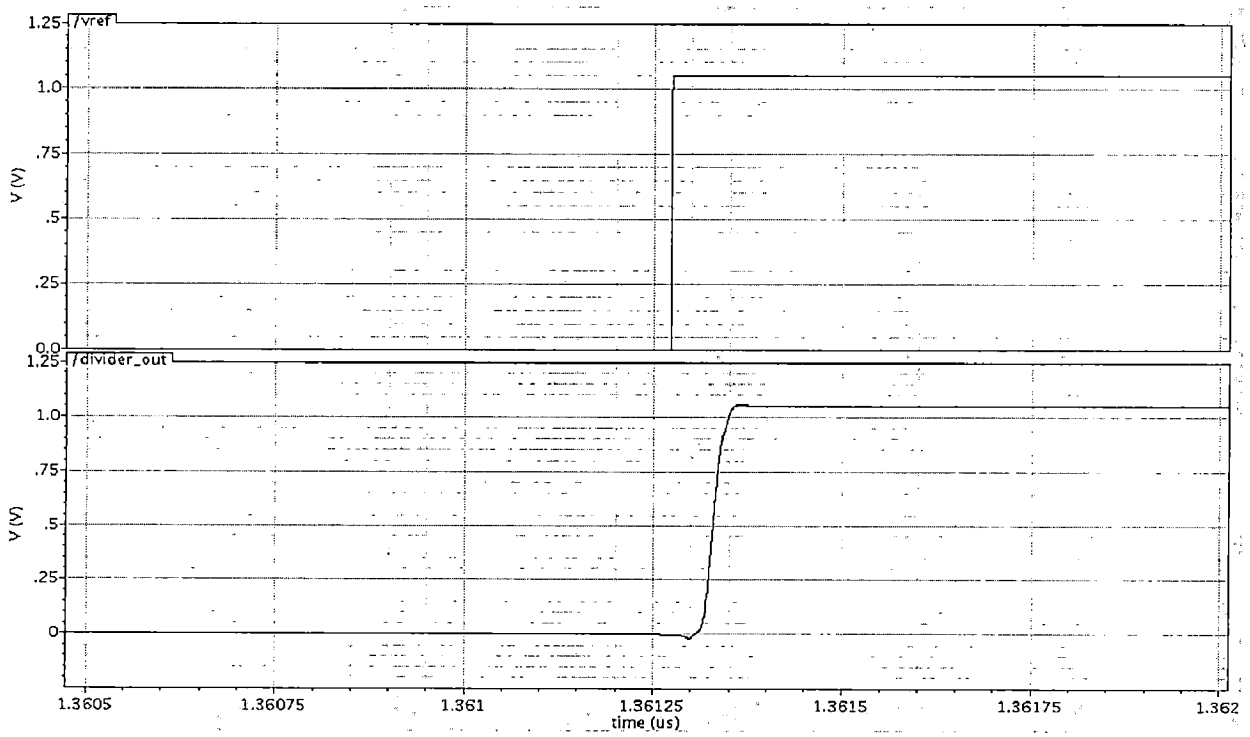



Figure 5.5 Plot showing the phase difference between reference and feedback signal

The outputs of the phase frequency detector, up and dn signals are producing pulses as shown in the figure 5.6 indicating that the reference frequency and the frequency divider output signals are in phase.

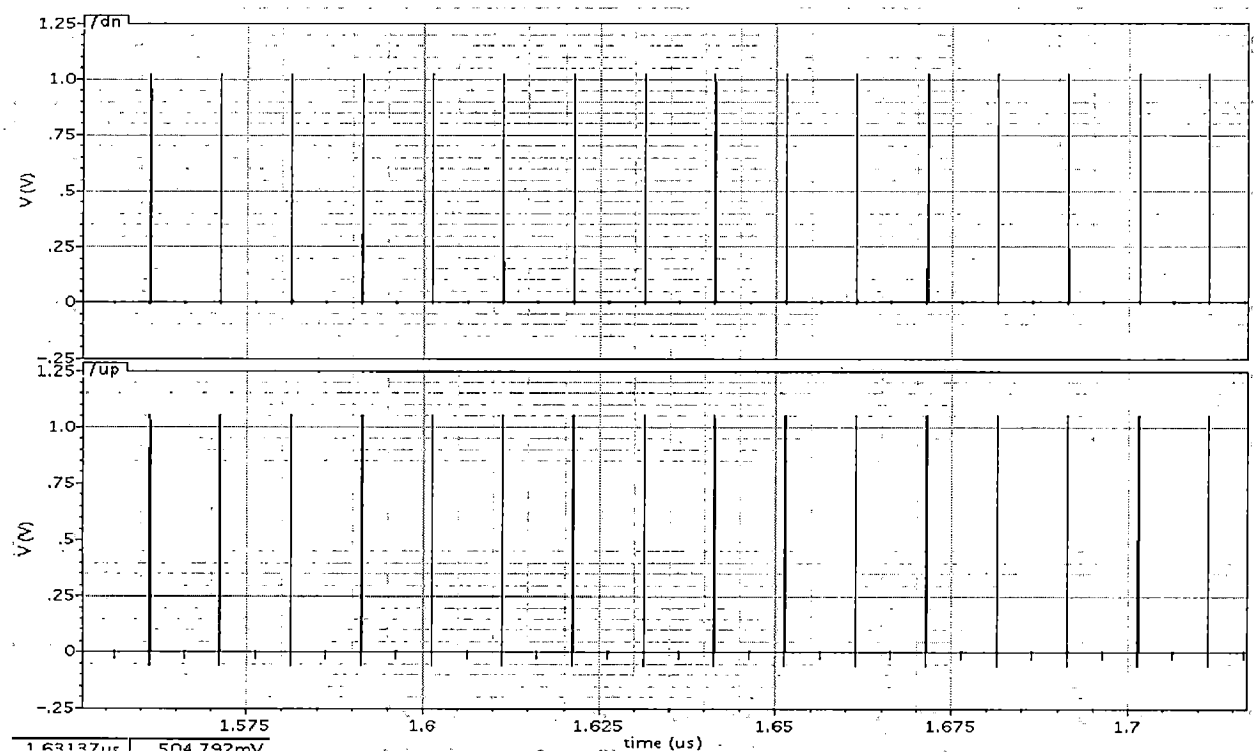



Figure 5.6 Outputs of phase frequency detector in locked state

The width of the dn signal pulse when PLL in locked state is 33ps, where as the width of the up signal is 95ps.

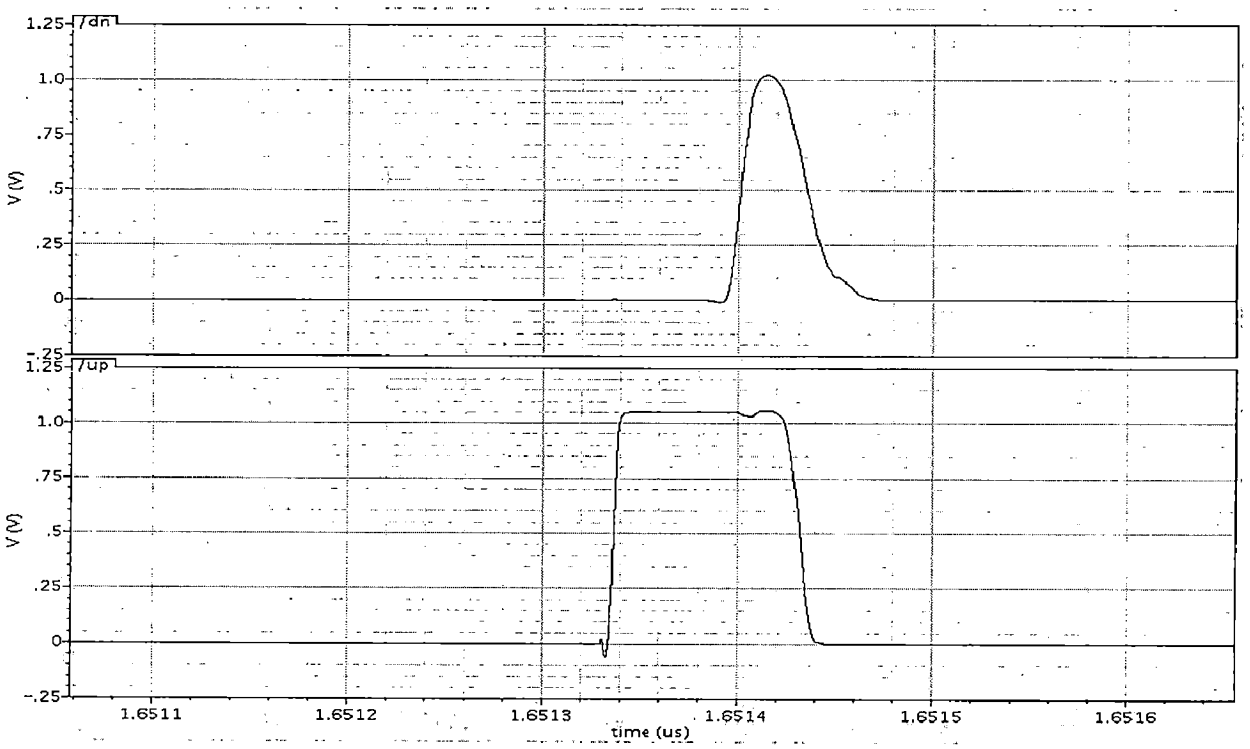



Figure 5.7 up and dn signal pulses

The Figure 5.8 shows the output waveform of the VCO when PLL is in locked state. The frequency of the VCO output signal is 6.410GHz.

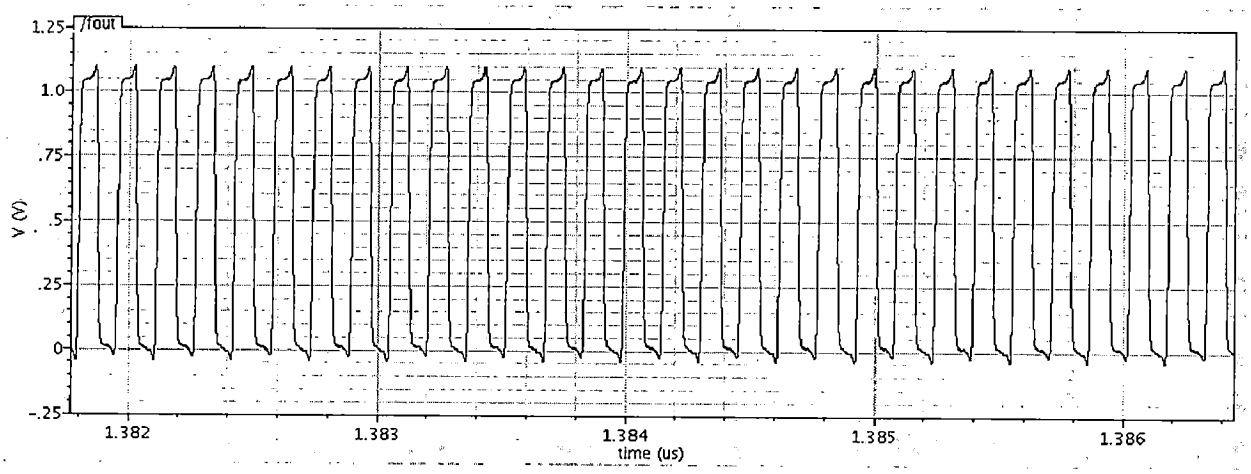



Figure 5.8 VCO output signal

Summary of overall PLL:

- Reference frequency is 100MHz
- Charge pump current is 150μA
- Loop filter is of second order
- VCO gain is 18GHz/v
- Linearity range of VCO is 200mV(425mV-625mV)
- Frequency divider is 6 bit
- Lock time of PLL is less than 0.45μs
- Power consumption of PLL in locked state is 3.2mW
- PLL output is 6.410 GHz
    - Error is 10MHz (0.15%)

# CONCLUSION

In this thesis we presented the design of CMOS based Digital Phase Locked Loop for generating high frequency clocks. In the proposed digital PLL, the previously proposed circuits for various units of DPLL were modified for better performance.

It incorporates a high performance phase frequency detector that requires minimum number of transistors and consumes as low as 0.4 μW of power. It provides a linearity range of $-2\pi$ to $+2\pi$ and eliminates dead zone almost completely.

The charge pump unit incorporated in the proposed PLL gave satisfactory simulation results. Various non idealities (channel charge injection, clock feed through and charge sharing) that were present in conventional charge pump were eliminated. Therefore no sudden jump phenomenon was observed in output during pump up or pump down operation. The problem of current mismatch that was present before (due to channel length modulation (CLM) effect) was suppressed by using stable bias voltages which are generated by the bias generator. The charge pump is designed to produce an output current of 150μA. The average power consumption is 0.625 μW.

The VCO unit incorporated will have dual delay paths in order to reduce delay of the single delay stage so that the frequency of operation will get maximized. The transfer characteristic of VCO was satisfactory in the operating range provided by charge pump (425mV- 625 mV). The average power consumption of the VCO circuit is 0.5 μW at 5GHz frequency and the frequency divider used is 6 bit.

The proposed PLL obtained by integrating all the units gave good simulation results. The lock time of PLL is less than 0.45μs and the average power consumption in locked state is 3.2 mw. The static phase error of proposed PLL is as low as 57 ps. The proposed circuit (DPLL) is suitable for various applications in high speed systems due to advantages of low power, fast locking and low static phase error.

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