PERFORMANCE INVESTIGATION OF SINGLE PHASE MULTILEVEL RECTIFIER

A DISSERTATION

Submitted in partial fulfillment of the
requirements for the award of the degree
of
INTEGRATED DUAL DEGREE
in
ELECTRICAL ENGINEERING
(With Specialization in Power Electronics)

By

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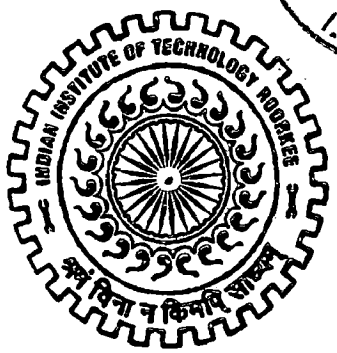

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Candidate's Declaration

I hereby inform that the dissertation titled, "**Performance investigation of single phase multilevel rectifiers**" being submitted by me in partial fulfillment of the requirements for the award of integrated dual degree in Electrical engineering with the specialization in power electronics at I.I.T Roorkee is a bonafide work carried by me under the guidance and supervision of **Prof. Pramod Agrawal** in the department of Electrical engineering, I.I.T Roorkee.

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Certificate

This is to certify that the above declaration made by candidate is correct to the best of my knowledge.

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Abstract

Researchers have always been improving the technology when it comes to the power quality improvement. Many converter topologies have been discovered in last 25 years and the research is still on in this area. Years back in around 1975, multilevel converters came into existence which completely changed the whole scenario of converter fed induction motors and many other power electronic applications.

This work starts with the comparison of multilevel rectifiers with other traditional converter topologies showing their edge over others. Different control strategies are discussed. In this dissertation work, basically different rectifier topologies are compared on the basis of their simulation results. The control strategy used here is mainly PWM scheme with hysteresis current control.

MATLAB simulations are carried out for R and RL loads for different topologies with PWM scheme. The hardware has been implemented for just one topology in the laboratory. SPARTAN 3 FPGA kit has been used for the digital control and the VHDL code for the control strategy is been generated by using Xilinx System Generator tool kit.

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Chapter 1: Introduction

1.1 Background:

Since the birth, power electronics has been in use widely in various applications. Its main objective has always been to maximize the efficiency and minimize the losses. To achieve this objective even researchers have been striving hard when they come to think of improving power quality at the receiving end.

Traditional diode and thyristor based rectifiers used in power converter applications draw pulsed current from the input main which deteriorates the line voltage, produce radiated and electromagnetic interference leading to the poor efficiency. For single phase power applications, passive power filters, active one and two stage PFC rectifiers are typical approaches used to achieve high power factor and low THD but they are bulky and heavy due to which there was a trade-off between their high efficiency, low cost and compactness. Active power factor corrector and active filters have been successfully researched and developed for power factor correction and current harmonics elimination, respectively. Power factor correction based on active current-shaping techniques has been presented in [1, 2] to improve the power quality of power converter systems. Several active power conversion topologies were used for power factor correction. These include the step up or boost converter, flyback converter and active input current shaper (AICS). Among the high power factor converters, the boost type is the most popular [3, 4]for drawing a sinusoidal current from the AC mains with nearly unity power factor. The DC side voltage of the boost converter is always higher than the peak voltage of the AC mains. The buck type AC-DC converters provide a DC bus voltage smaller than the peak voltage of the AC mains. The buck converters can limit the input inrush current and DC short circuit current. However, the high voltage stresses of the power devices are the main drawbacks if the circuits are used in medium voltage or high power applications. It has been shown in the literature that a single staged fly back converter can be operated as a single phase AC/DC converter with active power factor correction [5]. But the disadvantages of this conversion technique attributed mainly to the constant switching frequency and discontinuous nature of the current. In 1999 Active Input Current Shaper (AICS) was proposed [6] to turn a conventional Buck converter into a single

stage AC/DC converter with high efficiency, fast transient response and low cost. Here, the disadvantages mainly attributed to the increased cost compared to the conventional topology due to the extra winding coupled to the buck's output inductor and the voltage magnitude higher than peak value, across the bulk capacitor. Even conventional boost converters posed certain problems despite proving themselves good as power factor correctors. For high power or high voltage applications, the major concerns of conventional boost converters are inductor volume and weight, and losses on the power devices, which will affect converter cost, efficiency and power density. Some other methods were also experimented to improve the power quality like transformer coupling in multipulse converters so as to improve the power factors due to cancellation of certain low order harmonics of high amplitudes. But again the disadvantages here attributed mainly to the bulkiness, heavy and lossy nature of the converters.

Next came the two level converter topology which was popular in low voltage power conversion market but for applications with high switching frequencies such as high speed drives, traction converters, grid converters, wind power applications, etc. its technological progress has been slow. This two level converter also attributes some disadvantages [7, 8] which are discussed as follows:

1. For high switching frequencies the conduction losses increase with high or medium voltage rating devices for same rated currents. For example, 600-V IGBTs feature on-state voltages that are roughly 10% lower than that of a 1200-V IGBT at the same rated current and technology. Similarly, the switching loss energies of a 600-V IGBT with the same device technology and current are smaller by a factor of 3–5.
2. Common-mode currents are considered to be the main reasons for bearing currents/failures and electromagnetic interference (EMI) problems. These currents are caused by the common mode voltages which are significantly large in two level voltages.
3. Large size of inductors used to filter out the harmonics in AC currents and voltages at the terminal end which contains the high frequency content, thus increasing the effective cost.
4. It also uses a DC-link filter to reduce the ripples in DC output voltage which again increases the cost.

5. The major disadvantage is in the applications for medium and high voltage converters because to increase the operating voltage of these converters, many semiconductor devices are to be connected in series but this approach introduces high dv/dt which necessitates the use of interfacing transformers with high insulation requirements to withstand the switching of large voltage steps at high frequency (1-2Khz).

To overcome the aforementioned difficulties faced by conventional conversion techniques, multilevel technology came into existence years back in 1975. The very inception of the idea of concept of multilevel converters brought a ray of hope to the world of power electronics by proving themselves IPQCs. The multilevel converters have drawn tremendous interest in the power industry [9]. The general structure of a multilevel converter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The so-called "multilevel" starts from three-level. A three-level converter is usually called as "neutral clamped" converter. A large volume of research has been documented in the areas of circuit configuration, control and applications. These converters provide high power factor and reduced THD of current at the input ac mains and ripple-free regulated dc output voltage. It has been reported in the literature that using multilevel converters the THD can be reduced below 1% [10]. Multilevel converters have outperformed the conventional AC/DC converters known as rectifiers by achieving an improved power quality in terms of power factor correction, reduced harmonic distortions in AC input mains, higher efficiency, ripple free regulated DC output voltage and reduced stresses on the switching devices.

NOTE: Number of levels as denoted in further chapters of this report is only for half cycle.

1.2 Factors driving the research interest in this area:

Multilevel converters have an edge over conventional aforementioned converters due to the following multitude of factors:

- One of the major reasons is the self commutating devices unlike thyristor based converters, hence, complex commutation circuits can be escaped. MOSFETS are used mainly for small power ratings, IGBTs for medium, and GTOs for large power

applications. These have unsurpassed performances especially for high power applications.

- ❖ Yesteryears' trend shows a trade-off between the voltage rating and the switching frequency but the voltage stresses across the switching devices are just a fraction of overall voltage rating of the converter, thus allowing the use of high performance devices available at low voltage rating.
- ❖ Common mode voltages and electromagnetic interferences (EMI) caused by the changes in voltage levels at high frequency are reduced in these converters as the voltage is obtained in small steps (stair-case) with low dv/dt.
- ❖ Since there is no problem of high voltage stresses on the devices, voltage handling capacity of MLCs is not restricted by the voltage rating of the switches.
- ❖ Voltage and current harmonics are significantly reduced in MLCs. As mentioned earlier, the MLCs produce a regulated ripple-free dc output due to which the size of the inductor is reduced and hence, the core losses of the same. Thus, the efficiency and the performance are considerably enhanced. This has the advantage over conventional boost converters where the inductor size is four times the size used in here to ripple out the current [11].
- ❖ High voltage handling capability and improved spectral performance reduce the need for step-down and multi-pulse/poly-phase transformers which are used in two level and multi-pulse converters in high voltage applications. Substantial reduction in cost, size, weight and losses are possible by reduction of transformers.

1.3 Advantages over two level converters:

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

• Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced. The voltage stress across the switches in case of multilevel converters is reduced considerably as voltage is synthesized in small steps.

• Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage, therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies. Figure 1.1 shows the comparison of common mode voltage at switching frequency of 10Khz and common mode base voltage of output DC voltage in case of MLCs and two level converters.

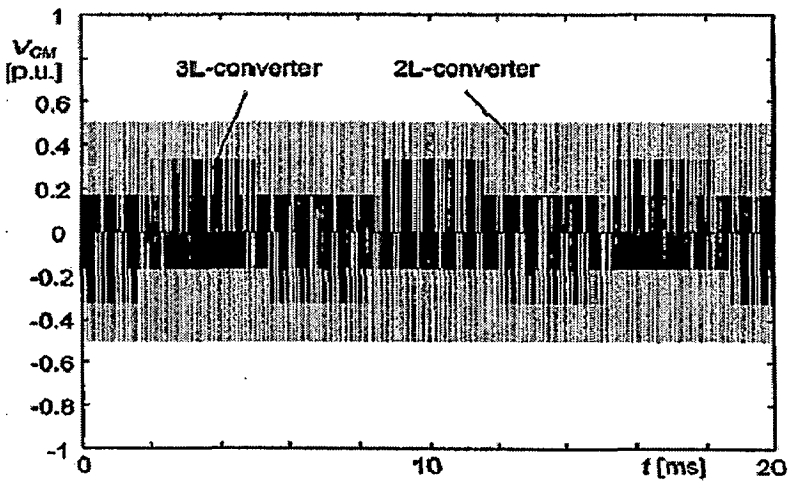
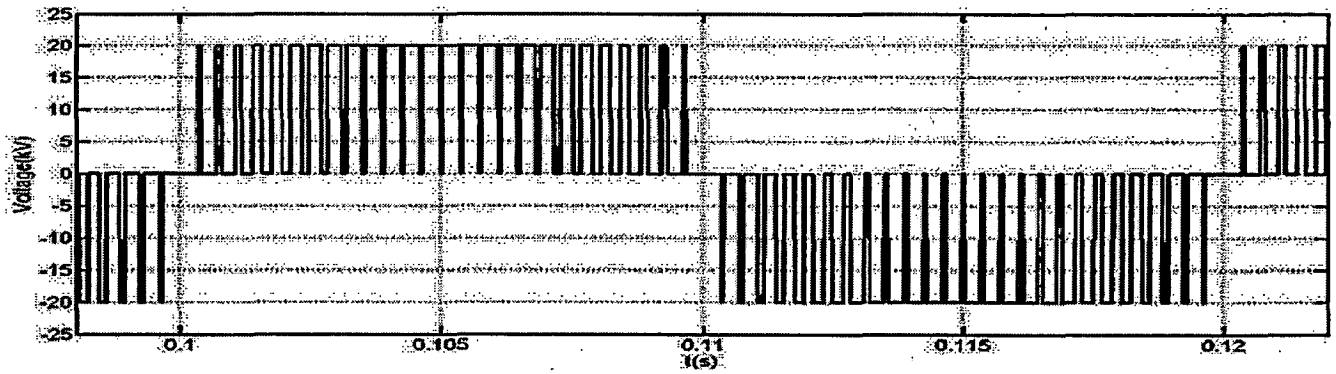


Fig. 1.1 Common mode voltages at Fs = 10Khz and Vcm,base = Vdc. [7]

• Multilevel converters can draw input current with low distortion. Line to line voltage waveforms shown in figure 1.2(a) and 1.2(b) along with their spectra show that multilevel converters produce lower harmonic distortion and lower voltage stress on the switches than those in two level converters.



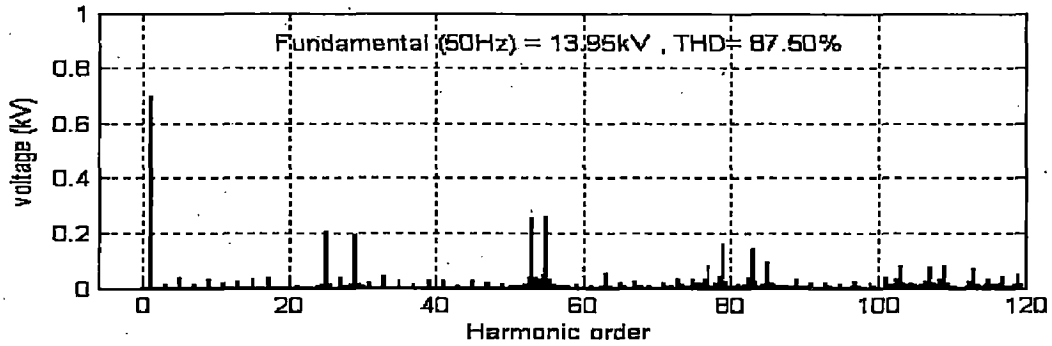


Fig. 1.2(a) Line to line voltage waveform and its spectrum in case of two level converter. [8]

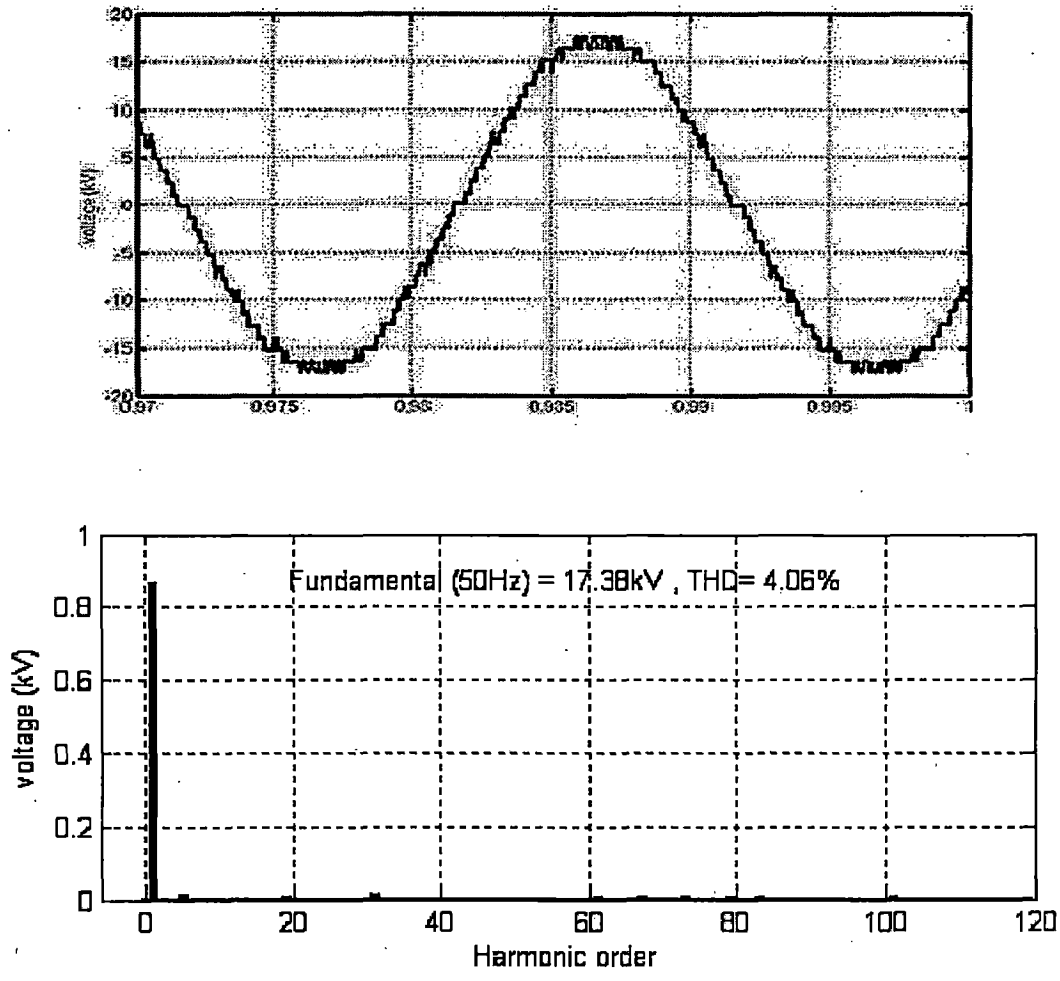


Fig. 1.2(b) Line to line voltage and its spectrum in case of a 17-level converter. [8]

• Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM with lower semiconductor losses than two level converters. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

1.4 Applications of MLCs:

Multilevel converters have been used widely in various applications since the birth. Multilevel ac–dc conversion of electric power is widely used in adjustable-speed drives (ASDs), switch-mode power supplies (SMPSs), uninterrupted power supplies (UPSs), and utility interface with non-conventional energy sources such as solar PV, etc., battery energy storage systems (BESSs), in process technology such as electroplating, welding units, etc., battery charging for electric vehicles, and power supplies for telecommunication systems, measurement and test equipments. Use of multilevel converters in DC-DC applications especially in automotives is commendable. Figure 1.3 shows a four level DC-DC converter used in 42 automotive systems.

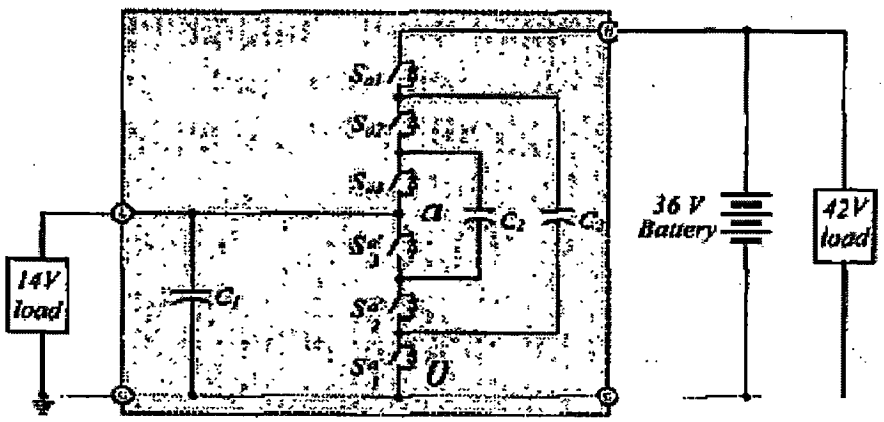


Fig. 1.3 Four level DC-DC converter used in 42 automotive systems.

Application of MLC with bi-directional power flow in electric drives forms an important area of research in MLC. MLCs were initially proposed in ac motor drives applications due to their ability to generate low harmonics, multi-tier waveforms. These converters have been extensively applied in ac motor drives in medium and high voltage ratings. Permanent magnet brushless motor (PMSM) drives are used in high power three-phase industrial drives and as well as in

single phase traction drives. These MLCs have various other applications in many fields shown in figures 1.4-1.5. Multilevel power converters have an important application in back to back inter-tie connections where one of the converter acts as rectifier and other acts as inverter thus making the bidirectional power flow possible between them. The result is a well-balanced voltage across each capacitor while maintaining the staircase voltage wave, because the unbalanced capacitor voltages on both sides tend to compensate each other. Such a dc capacitor link is categorized as the "back-to-back intertie." The purpose of the back-to-back intertie is to connect two asynchronous systems. It can be treated as 1) a frequency changer, 2) a phase shifter, or 3) a power flow controller. This back to back intertie configuration is used for driving three phase induction motor drives where front end of the converter set is used as rectifier and back end is used as inverter fed by the DC output of front end rectifier as shown in figure 1.6.

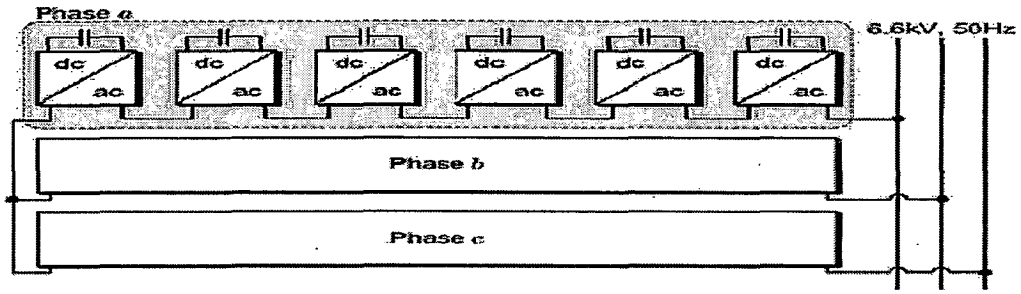
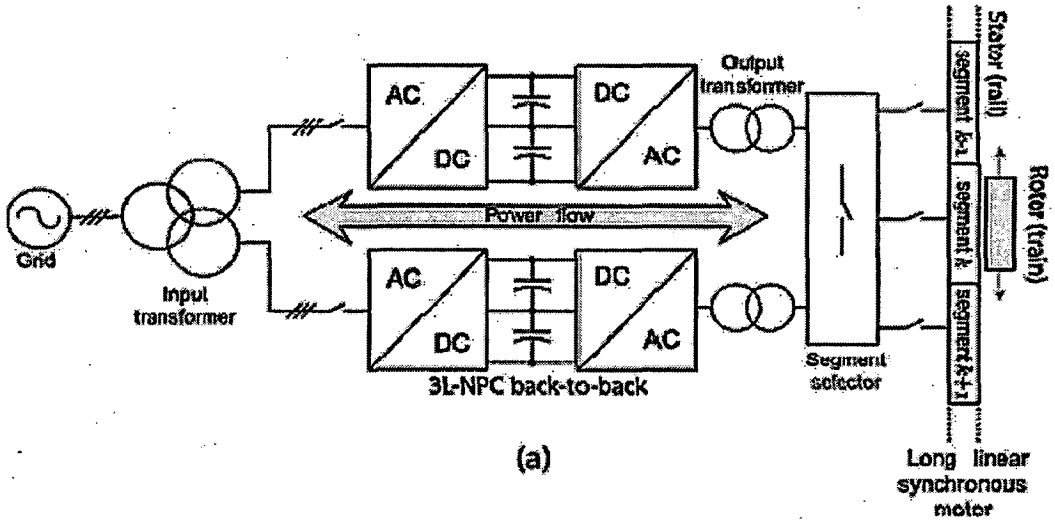


Fig. 1.4 Thirteen level CHB based transformerless STATCOM.



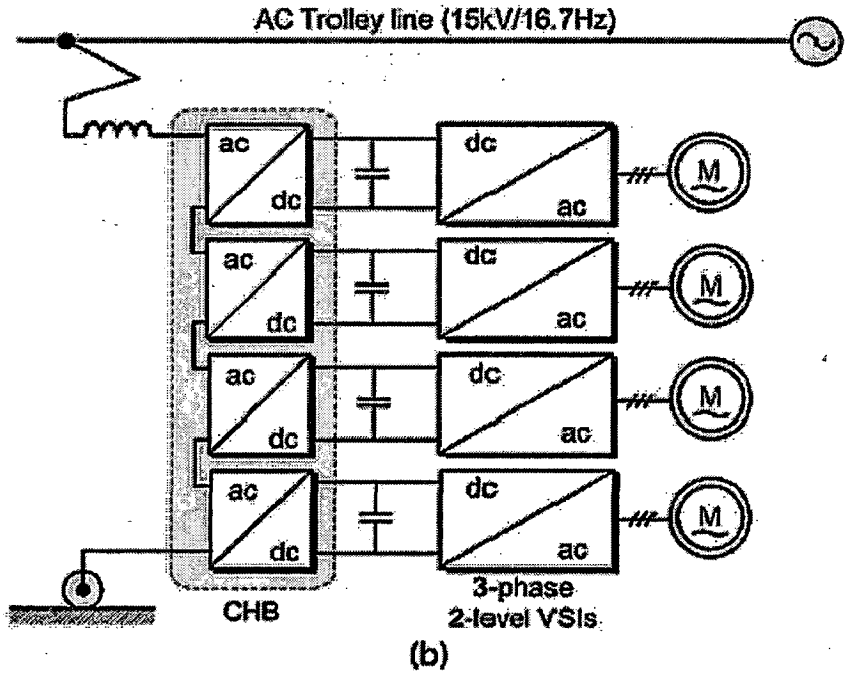


Fig. 1.5(a) Transrapid maglev train long linear synchronous motor with back to back 3L-NPC drive system. (b) CHB transformerless front end for the power interface of a locomotive traction drive

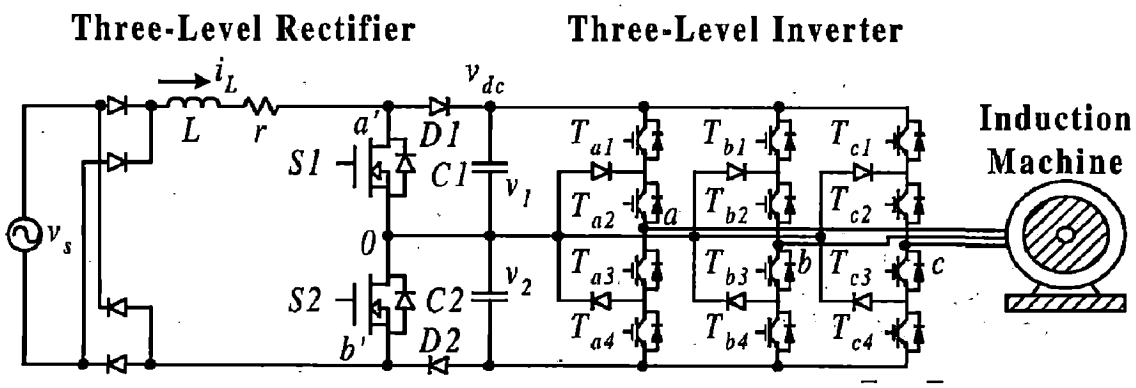


Fig. 1.6 Three level PWM rectifier/inverter.

1.5 Classification of MLCs:

MLCs are generally classified as diode clamped, flying capacitor and cascaded multilevel converters [12]. Circuit configurations of MLCs are classified [13] on the basis of power flow capability as shown in Figure 1.7. Since this work is mainly on single phase, it is better to

present the classification of single phase topologies. Many single phase circuit configurations are reported in the literature [14],[15],[16],[17] and few are shown in Fig. 1.8(a)–(e) using unidirectional and bidirectional switches with single, dual, and three capacitors at the dc link.

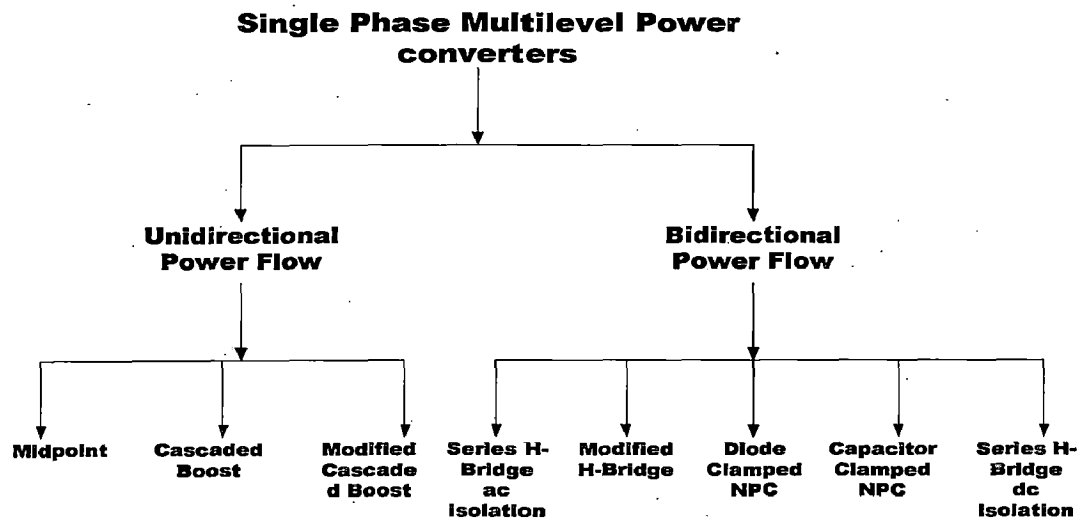


Fig. 1.7 Classification of single phase MLCs.

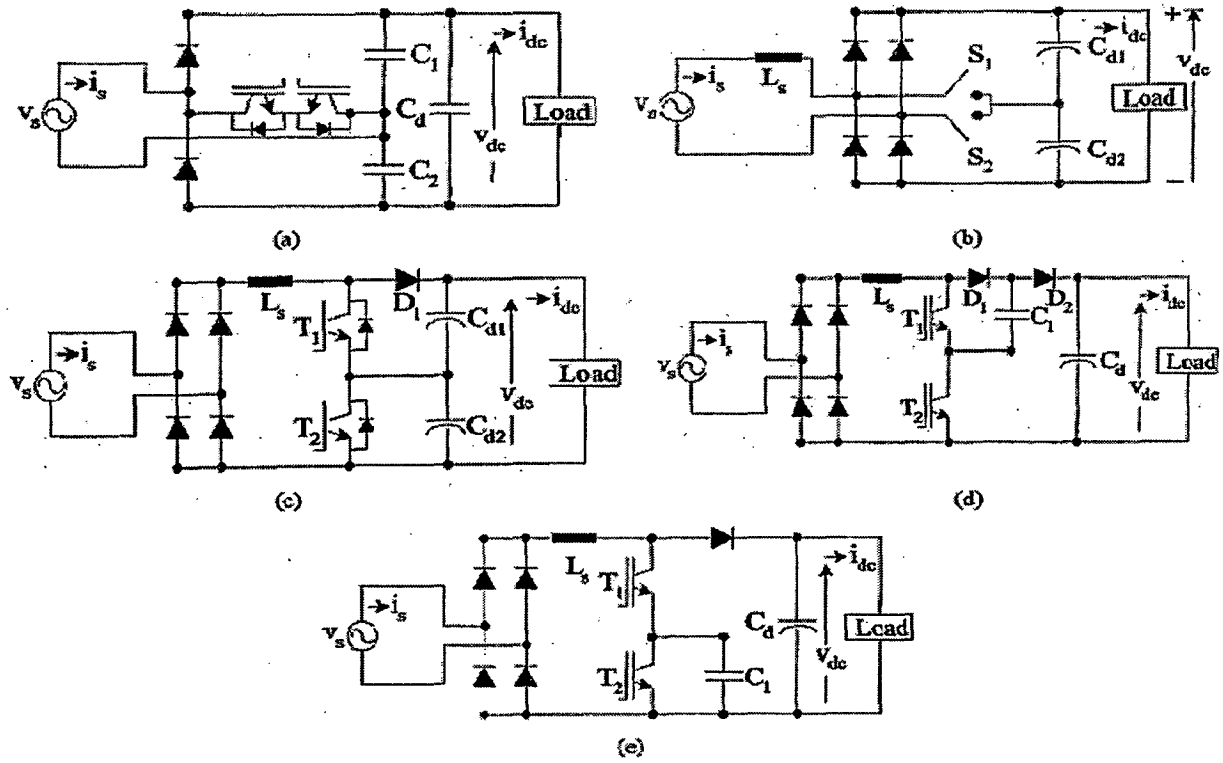


Fig. 1.8 (a)Half-bridge unidirectional multilevel converter. (b) Two-bidirectional-switch unidirectional multilevel converter. (c) Two-switch midpoint unidirectional multilevel converter. (d) Adapted unidirectional multilevel converter. (e) Modified adapted unidirectional multilevel converter.

1.6 Basic structure of MLCs:

1.6.1 Diode clamped topology:

An m-level diode-clamp converter typically and basically consists of $(m-1)$ capacitors on the dc bus and produce m levels of the phase voltage. Fig. 1.4 shows a single-phase full bridge five level diode-clamp converter in which the dc bus consists of four capacitors, C_1, C_2, C_3 and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. Table 1.1 lists the voltage levels and their corresponding switch states. State condition 1 means the switch is on, and 0 means the switch is off.

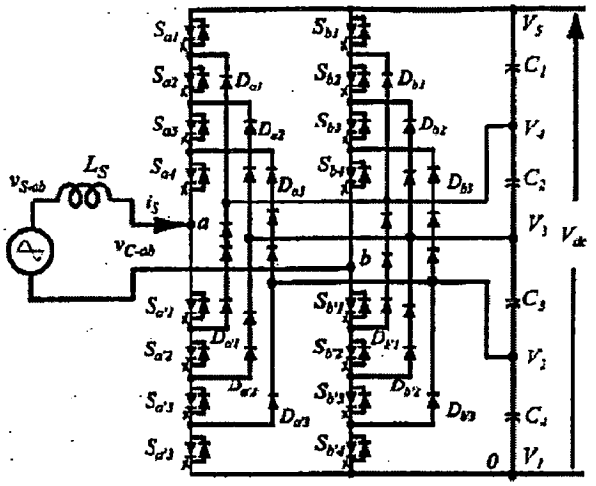


Fig. 1.9 A diode clamped five level configuration.

Output V_{a0}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

Table 1.1 Diode clamped five level rectifier with switching states and voltage levels.

There are certain advantages and disadvantages of this diode clamped topology as follows:

Advantages:

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Efficiency is high because all devices are switched at the fundamental frequency.
- Reactive power flow can be controlled.
- The control method is simple for a back-to-back intertie system.

Disadvantages:

Some of the inherent features of this topology mainly attribute to the disadvantages as described:

- Although each switching device blocks $V_{dc}/4$ only but the each diode blocks a different voltage depending upon its position in the topology. For example, in figure 1.4, diode $D_{a'1}$ blocks all three capacitor voltages, when switches $S_{a'1} - S_{a'4}$ are turned ON, equating to $3V_{dc}/4$. Due to this the diodes are of different voltage ratings. If we employ diodes of equal ratings then the no. of diodes would be increased to (m-1)(m-2) in each leg for m-level converter thus, making the system impractical to implement.
- From Table 1.1, it can be seen that switch S_{a1} conducts only during $V_o = V_{dc}$, while switch S_{a4} conducts over the entire cycle except during $V_{ao} = 0$. Such an unequal conduction duty requires different current ratings for switching devices. When the

inverter design is to use the average duty for all devices, the outer switches may be oversized, and the inner switches may be undersized.

- In most applications, a power converter needs to transfer real power from ac to dc (rectifier operation) or dc to ac (inverter operation). When operating at unity power factor, the charging time for rectifier operation (or discharging time for inverter operation) for each capacitor is different. Such a capacitor charging profile repeats every half cycle, and the result is unbalanced capacitor voltages between different levels.
- Adapted diode clamped topology addresses an important issue of unequal sharing of voltages in clamping diodes and hence neutral point voltage balance problem arises in diode clamped converters with higher number of levels. The topologies with the inherent neutral point voltage balance have been discovered in the literature [18]. These topologies are being extensively used in ac motor drives and other utility applications.
- It is difficult to do real power flow control for the individual converter.

1.6.2 Flying capacitor topology:

Then came the capacitor clamped topology which was an important modification to the diode clamped topology. This topology was proposed to simplify the neutral point voltage balancing and to eliminate clamping diodes. However, this also further faced a couple of difficulties in control which are mentioned in further section of this section. Some basic flying capacitor topology [19] is described as follows:

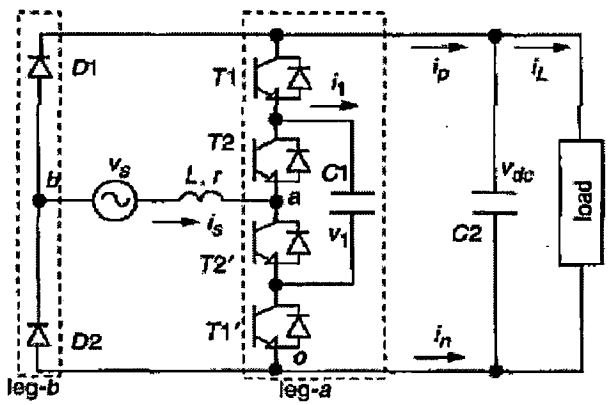


Fig. 1.10 Single phase unidirectional flying capacitor topology.

To perform the power factor correction in the proposed rectifier, the operating principle must be considered. There are four power switches, two diodes and one clamped capacitor in the proposed rectifier. To prevent damage to the power switches in the rectifier leg *a*, the constraints on the power switches are $T_i+T_i'= 1$, $i = 1,2$ where *Ti* (or *Ti'*)= 1 or 0, if power switch *Ti* (or *Ti'*) is turned on or off, respectively. Therefore, there are two independent power switches and four valid switching states in leg *a*, and two operating states in leg *b*. Table 1.2 gives eight valid switching states in the proposed rectifier. Depending on the voltage level, there is one operating state to generate the voltage levels $V_{ab} = V_{dc}$ and $-V_{dc}$, respectively, and two operating states to perform voltages $V_{ab} = V_{dc}/2$, 0 and $-V_{dc}/2$, respectively.

Valid switching states	i_s	T1	T2	V_{ab}	$V_{ab}(V_1=Vdc/2)$	Mode
1	+	0	0	0	0	3
2	+	0	1	V_1	$V_{dc}/2$	2
3	+	1	0	$V_{dc} - V_1$	$V_{dc}/2$	2
4	+	1	1	V_{dc}	V_{dc}	1
5	-	0	0	$-V_{dc}$	$-V_{dc}$	5
6	-	0	1	$V_1 - V_{dc}$	$-V_{dc}/2$	4
7	-	1	0	$-V_1$	$-V_{dc}/2$	4
8	-	1	1	0	0	3

Table 1.2 Valid switching states of above mentioned topology.

This configuration is also generally known as capacitor clamped. Now there are certain advantages and disadvantages of this topology as well.

Advantages:

- Large number of storage capacitors enables the converter to ride through short duration outages and deep voltage sags.
- Provides switch combination redundancy for balancing different voltage levels.

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Both real and reactive power flow can be controlled, making a possible voltage source converter candidate for high voltage dc transmission.

Disadvantages:

- An excessive number of storage capacitors is required when the number of converter levels is high. High-level systems are more difficult to package and more expensive with the required bulky capacitors.
- The control will be very complicated to track the voltage levels of all the capacitors and also their precharging to the same level and start-up are complex.
- Switching utilization and efficiency are poor for real power transmission.

1.6.3 H-Bridge topology:

These converters are generally bidirectional in nature. These are used for even high-power applications such as BESS, metros, traction, etc. These have major applications in STATCOM [20], facts devices as static var compensator for exchanging the reactive power along the power transmission lines. These can be developed for a higher number of levels for high-voltage and high-power applications. A bidirectional H-bridge converter topology is shown in figure 1.6. This topology has used isolation transformer which is application specific.

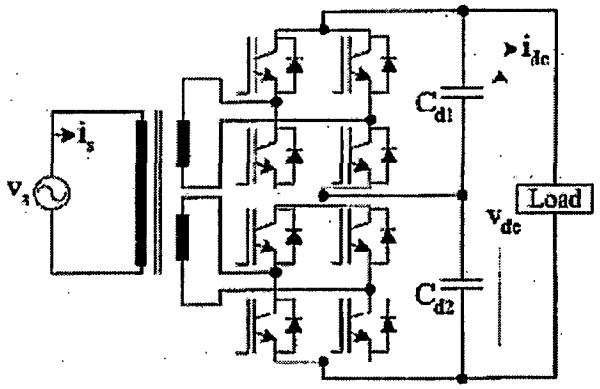


Fig. 1.11 Bidirectional cascaded five level converter.

Every cell of the H-bridge converter has equal or different input supply depending upon the type of converter which can be further classified [21] as follows.

There are 4 types of H-bridge converters.

1. Cascaded H-bridge.
2. Hybrid H-bridge.
3. Quasilinear.
4. New hybrid (ternary).

The summary of $V_{in}(max)$, no. of levels and maximum output voltage $V_{out}(max)$ is described in table 1.3.

Type	$V_{in\,(max)}$	$V_{out\,(max)}$	No. of levels
Cascade	V_{dc}	SV_{dc}	2S+1
Hybrid	$2^{s-1}V_{dc}$	$(2^s-1)V_{dc}$	$2^{S+1}-1$
Quasilinear	$2*3^{s-2}V_{dc}$	$(3^{s-1})V_{dc}$	$2*3^{s-1}+1$
Ternary	$3^{s-1}V_{dc}$	$((3^s-1)/2)V_{dc}$	3^s

Table 1.3 Summary of different types of H-Bridge converters.

This configuration also possesses some advantages and disadvantages as well.

Advantages:

- Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
- Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors.
- Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.
- The number of possible output voltage levels is more than twice the number of dc sources as shown in table 1.3.
- Stage with higher DC link voltage has
  - Lower number of commutations.
  - Lower associated switching loss.

- Higher DC link voltage consists of lower switching frequency components.
- Lower DC link voltage consists of higher switching frequency components.

Disadvantages:

- Needs separate dc sources for real power conversions, and thus its applications are somewhat limited.
- Connecting separated dc sources between two converters in a back-to-back fashion is not possible because a short circuit will be introduced when two back-to-back converters are not switching synchronously.

1.7 Control Schemes:

The control strategy is the heart of any converter system to get the desired output results. It is mainly implemented in three sections as described further.

1. First section involves the sensing of variables being used in the scheme according to the applications. The sensed variables can be the input ac mains voltage, dc output voltage, input current and in some cases some additional variables are also sensed such as the capacitor voltage in the flying capacitor topology. For example in the control scheme of topology shown in figure 1.5 the sensed variables are input voltage, input current, output dc voltage and voltage Vc1 across the capacitor C1. The sensing of these variables involves different sensors.

2. Second section is the most important part of the whole scheme as it comprises the control algorithm which is responsible for the transient and steady state performance. The control algorithm is implemented through several controllers like PID or PI controller, sliding mode control high speed digital controllers, microcontrollers, DSP, application specific integrated circuits(ASIC) depending upon the rating, cost, customer requirements and types of converters. In some of the cases fuzzy logic controllers and neural network based controllers are employed to provide the fast dynamic response. Moreover, high-speed and high-accuracy microcontrollers and digital signal processors (DSPs) are available at reasonably low cost. Many processors are developed to give direct PWM outputs with fast software normally used in some of these converters, which reduces hardware drastically.

3. Third section involves the generating of the firing pulses for the switching devices which actually make any converter work. The output of the controllers used in the second section is obtained by the processing of the error difference between reference parameter and the sensed variable in the controller itself. This output generates the switching signals for the devices. Nowadays, processors are available which are developed only for power electronics applications and have dedicated PWM controllers as an inbuilt feature to implement concurrently all three stages of the control strategy for improving the transient and steady-state performance of these converters. For hardware, the firing pulses are being generated using FPGA tools and DSPs.

The control strategies for the multilevel power converters can be classified as shown in figure 1.7:

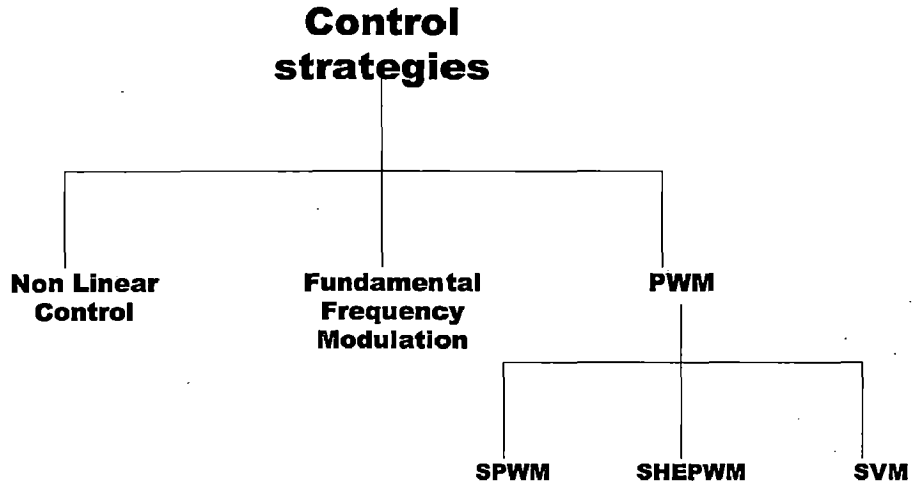


Fig. 1.12 Control strategies of MLCs.

(a) *Non linear control:* This scheme is mainly applied to the single phase unidirectional converters due to the inherent non-linearity. The control decision is based on several factors such as magnitude of input voltage, voltage level in individual capacitors and current tracking requirement.

(b) *Fundamental frequency modulation:* This modulation technique involves approximation of the required voltage waveform with the discrete voltage levels. Implementation of this scheme is computationally simple and several problems associated with high frequency

switching like EMI/RFI, losses etc are reduced. The main drawback is requirement of controllable dc bus to vary the magnitude of output voltage in inverters.

(c) *Pulse width modulation (PWM):* Conventional two-level PWM techniques have been extended to MLCs with consistent results. These include space vector modulation (SVM), multilevel sinusoidal PWM (which has been mainly used in the topologies described in this work), selective harmonics elimination PWM (SHEPWM) and random PWM techniques. In most of the above topologies, PWM scheme is used.

1. *Sinusoidal PWM (SPWM):* In multilevel SPWM, multiple bands of carrier signals of high frequency (to achieve the spectral performance comparable to two level converters) are compared to sinusoidal command signal to achieve linear amplification. This sinusoidal command signal is synchronized with high frequency carrier wave. MLCs can operate in low modulation index region in several applications losing one or several levels to provide the required voltage magnitude.
2. *Space Vector Modulation (SVM):* This technique involves synthesis of required voltage vector from a number of voltage vectors corresponding to switching states. Nearest three vectors (NTV) algorithm synthesizes voltage vector from nearest three vectors and is found to be the optimal solution in synthesis of required voltage vector and excellent spectral quality. This control scheme is most common in three phase converters. Large redundancy in three level converters is utilized to maintain neutral point voltage balance and is an inherent part of SVM of multilevel converters. Use of SVM beyond three-level converters is computationally intensive and becomes impractical as number of levels increase. However, some generalized algorithms for SVM in MLCs with higher number of levels provide a less computationally intensive method for MLCs.

1.8 Literature Review:

Ralph Teichmann and Steffen Bernet presented a paper [7] giving the comparisons between two level and multilevel converters for low voltage applications, traction drives and utility applications. Another paper was presented showing the comparison between two level and multilevel converters for medium voltage applications [8].

S. Norrga presented the paper [22] on a bidirectional AC/DC converter for AC fed railway propulsion applications. This topology includes the soft switching of the devices. Many other industrial applications have been shown in the paper [23].

B.R. Lin, S.J. Huang and T.L. Hung presented the paper [24], on a novel single phase AC/DC converter with two PWM schemes including a hysteresis current control scheme. This paper showed that using a new topology with just three switches how a three level converter can be achieved with reduced THD. They have used a flying capacitor topology. ***B.R. Lin, T.L. Hung and C.H. Huang*** proposed a single phase half bridge rectifier [25] with capacitor clamp topology. The control scheme proposed here can also perform a shunt active power filter operation to eliminate the harmonic distortions in input source current and compensate the reactive power generated from the non-linear load. ***B.R. Lin, T.Y. Yang and K.T. Yang*** presented a paper [26] on a novel single phase half bridge rectifier. Topology comprises two power switches and two diodes. A carrier based current controller is used. ***B.R. Lin, Y.A. Ou and T.Y. Yang*** presented a paper [27] on a novel single phase unidirectional power flow rectifier to generate a three level PWM voltage waveform. No flying capacitor or clamping diode is used in this topology. ***B.R. Lin and C.H. Huang*** proposed a novel single phase AC/DC/AC converter [28] with capacitor clamped topology with a three leg configuration which has a common leg between AC/DC and DC/AC converters to reduce the number of switching devices compared with the conventional three level AC/DC/AC system.

Bhim Singh, Brij N. Singh, A. Chandra, Kamal Al-Haddad, Ashish Pandey, and Dwarka P. Kothari presented a review paper [12] on improved power quality AC/DC converters including boost, buck and buck-boost converters. In this paper advantages of multilevel converters are also

presented. Bhim Singh along with others also presented a review paper on multilevel AC/DC converters describing types of topologies, control strategies, applications and future scope as well in [13].

1.9 Objective of Dissertation work:

After presenting the literature review of multilevel converters over a period of years, we can give the objective of this dissertation work as follows:

- Studying features of multilevel rectifiers and its advantages over conventional two level and other topology rectifiers.
- Simulations of different topologies with sinusoidal PWM control scheme.
- Analysis of THDs for various loads and input power supply.
- FPGA based implementation of sinusoidal PWM scheme.
- Hardware development of one specific topology in the laboratory.

1.10 Organization of dissertation:

Chapter 1

This chapter gives the introduction to the multilevel rectifiers, its advantages over traditional rectifiers, its control schemes and literature review is also discussed.

Chapter 2

In this chapter, simulations of different multilevel rectifier topologies are carried out on MATLAB SIMULINK and study of THDs is analyzed with varying loads and input voltage supply.

Chapter 3

This chapter gives an overview of FPGA. Its origin, architecture, applications, design implementation and problems are discussed.

Chapter 4

In this chapter, the digital control and software implementation is carried out on SPARTAN 3 FPGA kit using Xilinx System Generator tool kit

Chapter 5

In this chapter, hardware implementation of a single topology is detailed and other hardware circuits are described.

Chapter 6

In this chapter, conclusions and future scope on multilevel rectifier are placed in this chapter.

Chapter 2: Simulations study of Multilevel Converters

2.1Introduction:

In this chapter the simulations of different multilevel rectifier topologies implemented in MATLAB SIMULINK are presented. Topologies are presented one by one with their power circuit, control scheme, simulation results with R load and then RL load, steady state analysis, dynamic analysis and THD analysis.

2.2 Simulations of Multilevel Rectifier:

Multilevel rectifier topologies are simulated with R and RL loads by simple PWM control scheme.

One of the topologies is already been discussed in chapter 3, so we will start with the simulations of other topologies and previous topology will be presented at last. There are number of different topologies presented.

2.3 Topology 1:

For following topologies the control scheme implements the hysteresis current control in the inner control loop. The first topology [19] is as shown below in figure 2.1.

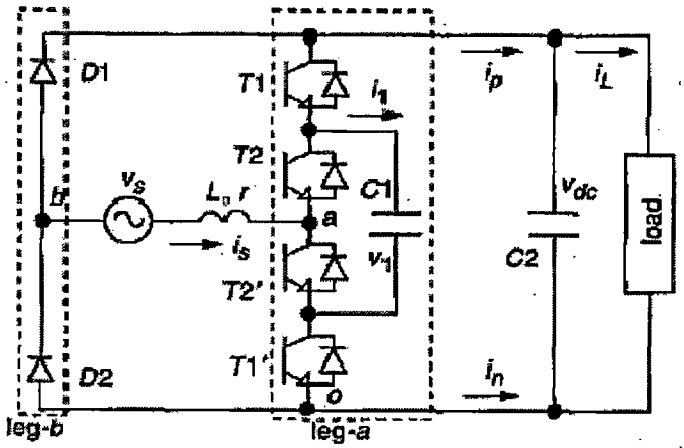


Fig. 2.1 Unidirectional three level rectifier with capacitor clamped scheme.

The control scheme block is shown in figure 2.2 below:

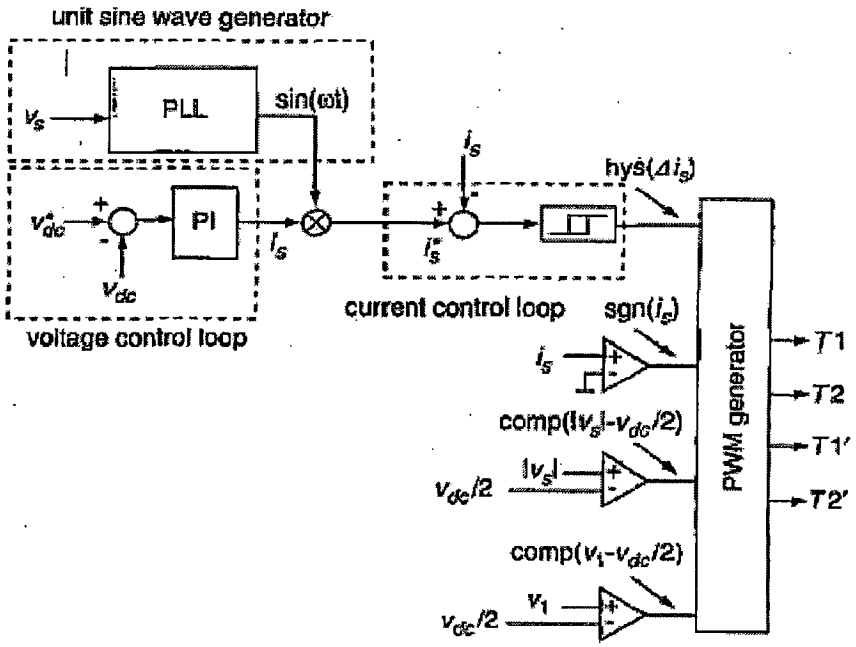


Fig. 2.2 Control block of above rectifier.

The control scheme uses a PI controller for the balancing of output DC voltage. The unit template is multiplied with the output of PI controller to give the reference input current which compares the actual input source current with itself and the error goes to the hysteresis current controller. This current tries to track the reference current due to the controller. PWM generator generates the firing pulses for the switching devices of the converter by the different combination of comparator outputs depending upon the direction and sign of input voltage and current.

2.3.1 Simulation with R load:

The simulation parameters are varied with varying loads. Initially the parameters are as follows:

Input AC voltage = 110V rms.

Output DC voltage = 200V.

Hysteresis Band = 0.5A.

R load = 1A.

The simulation results for the steady state are shown in figure 2.3.

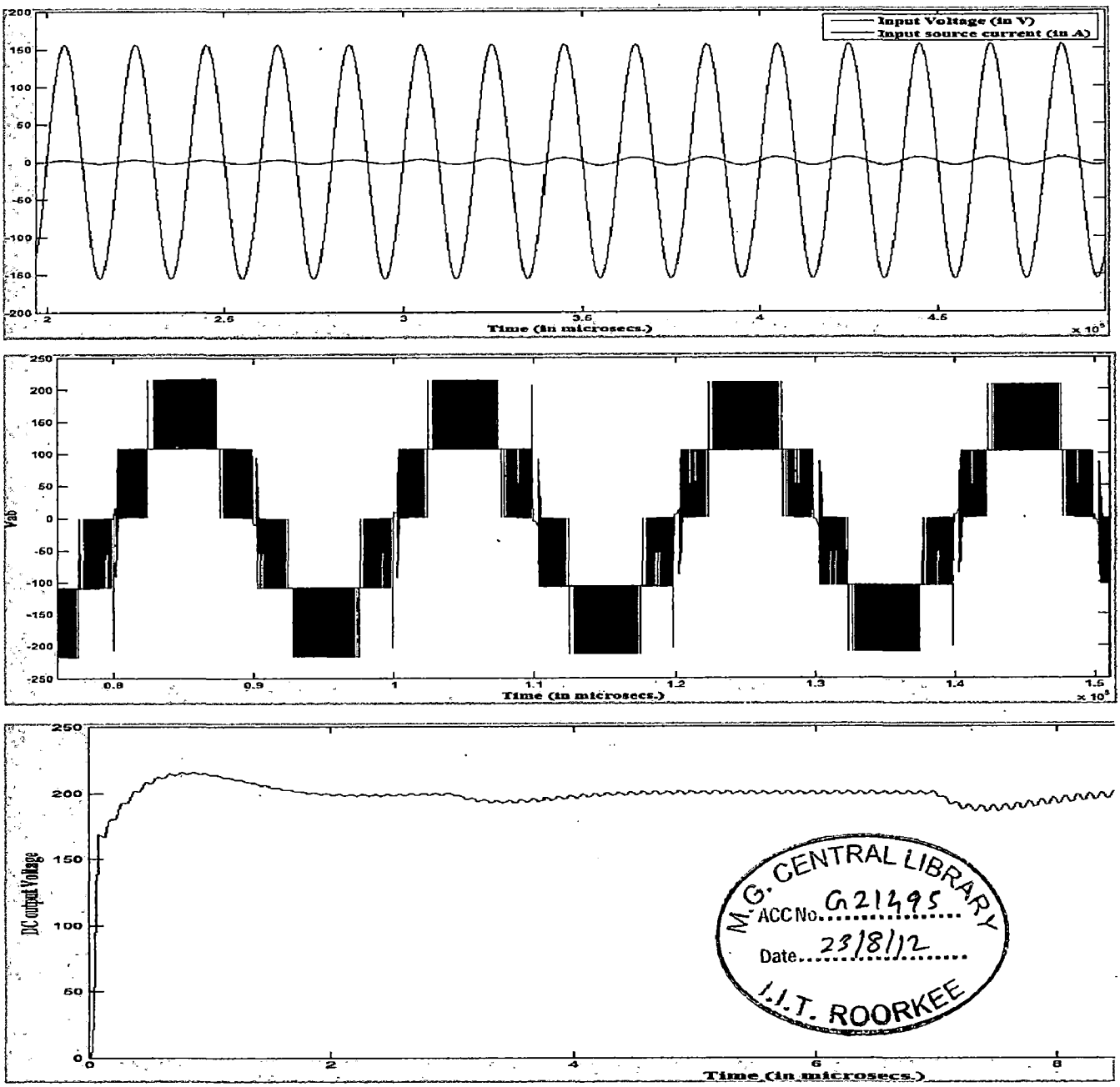


Fig. 2.3 Scope results for input voltage, input source current, three level voltages and DC output voltage.

The first scope window shows input voltage and input source current which are in phase with each other showing the power factor is nearly unity.

The FFT analysis shows the THD as 3.30% like shown in below figure 2.4.

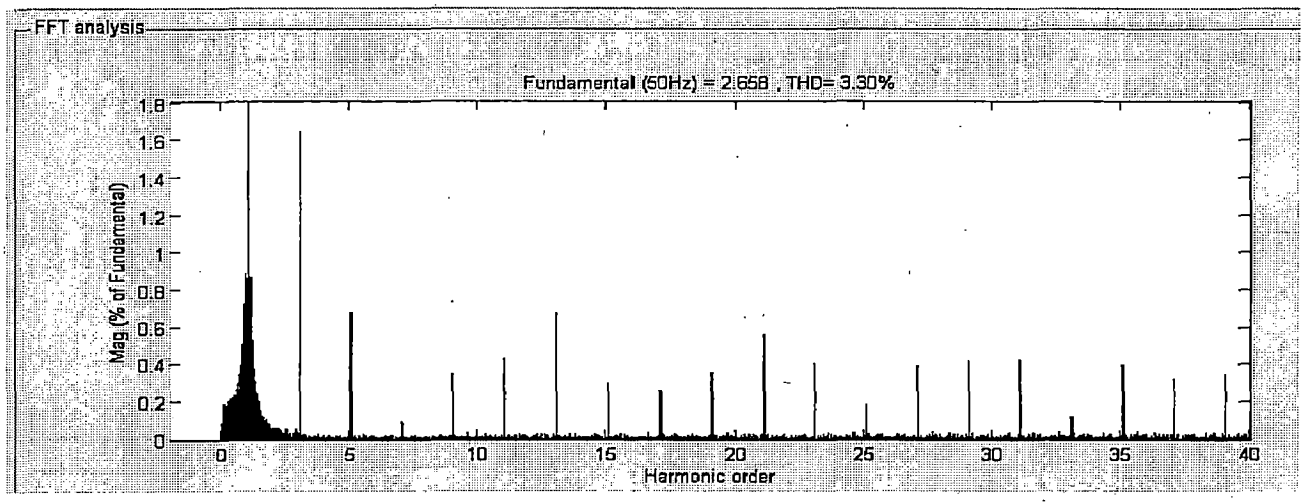


Fig. 2.4 FFT analysis showing THD.

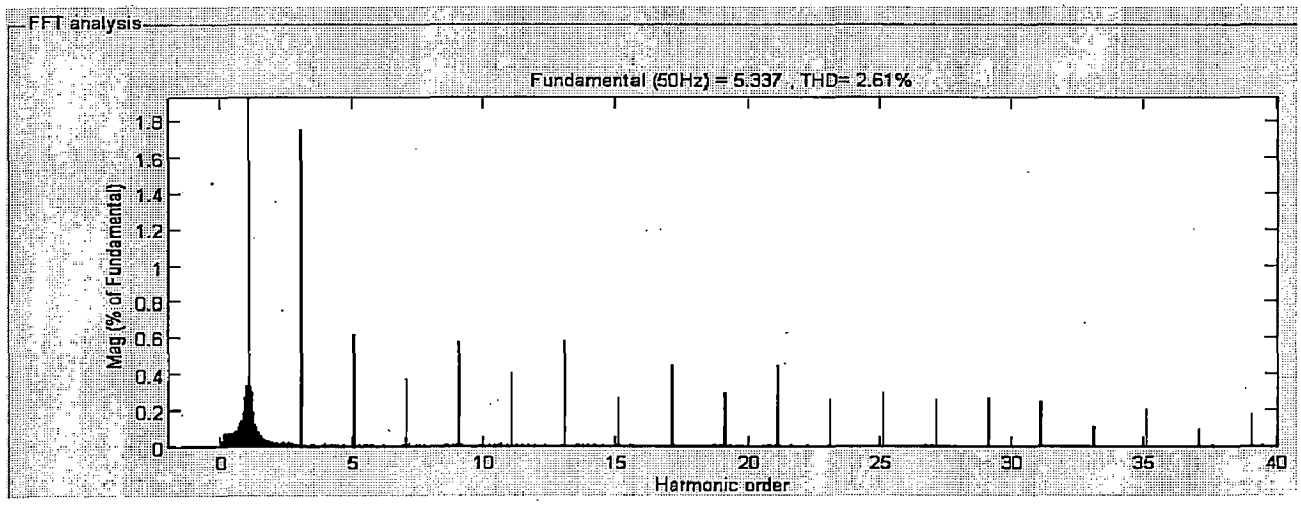


Fig. 2.5 FFT analysis with load of 2A.

Now the simulation results with R load of 2A are nearly similar to those shown previously except that the input source current is increased and the DC output voltage is not much regulated (reason is explained further in conclusion). FFT analysis is shown in figure 2.5. Similarly the simulation results for 4A load current are shown but the FFT analysis is shown in figure 2.6.

Note: THD of input source current only is talked about in this dissertation work.

Now we will vary the input power supply and watch the results. Input power supply is 70V rms. The results are as shown in figure 2.7. This is called as dynamic state study of a converter.

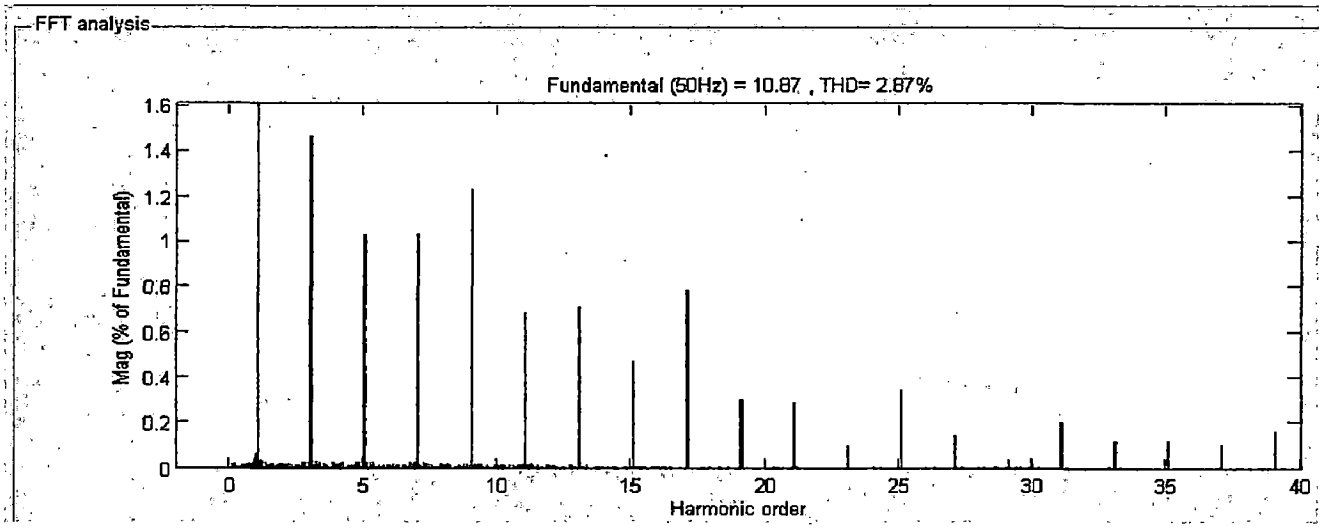
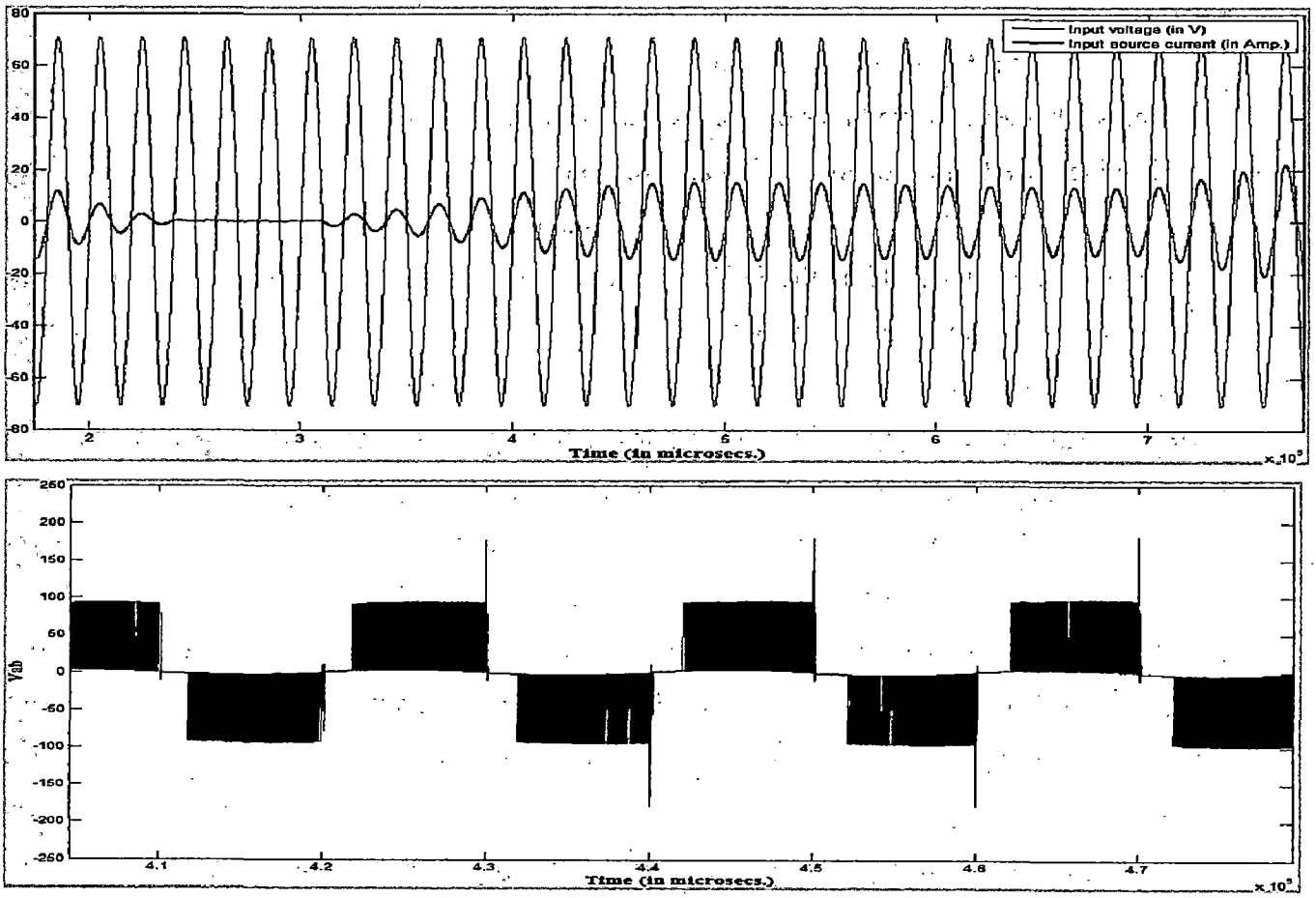


Fig.2.6 FFT analysis with load of 4A.



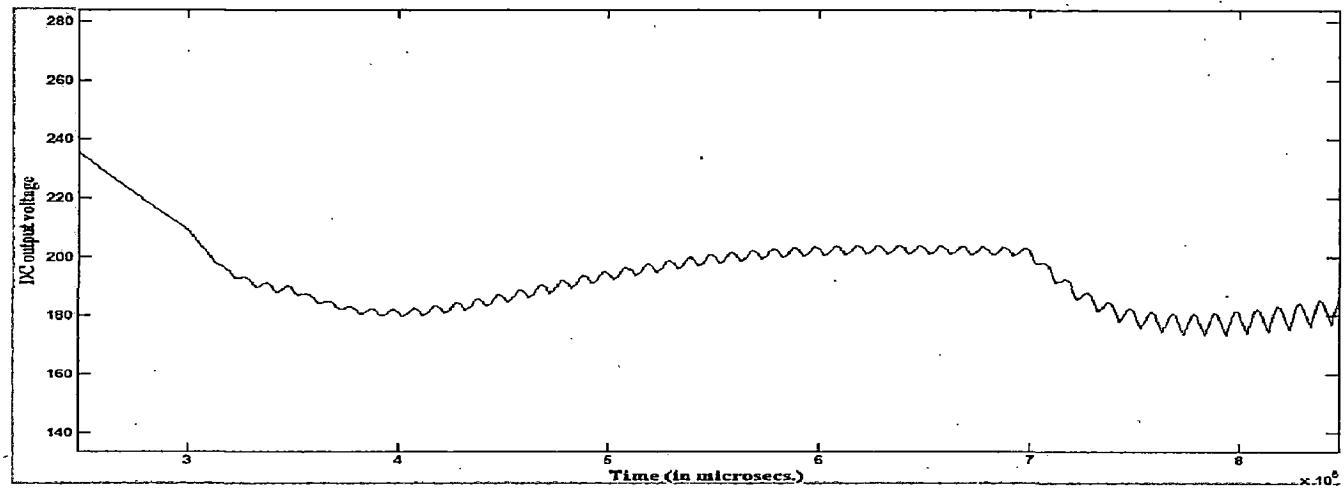


Fig. 2.7 Scope showing simulation results with input voltage, input source current, multilevel voltages and Dc output voltage.

As we can see that after reducing the supply voltage the level has decreased to two. The results of Vab shows that level of voltages on the AC side has decreased to two levels only. Input source current has increased significantly. This has a reason behind it. To generate a three-level voltage waveform on the AC side of the converter, the mains voltage must be less than the DC bus voltage and greater than half of the DC bus voltage. Two operating regions of mains voltage during one cycle of mains frequency are defined and shown in figure 2.8. In the first region, the instantaneous mains voltage is greater than –Vdc/2 and less than Vdc/2. Voltage levels 0 (low voltage level) and Vdc/2 (high voltage level) are generated on voltage Vab in the positive mains voltage to control the line current. During the negative mains voltage, voltage levels -Vdc/2 (low voltage level) and 0 (high voltage level) are selected to control the line current. In the second region, the absolute value of the mains voltage is less than the DC bus voltage Vdc but greater than half of the DC bus voltage Vdc/2. Voltage levels Vdc and Vdc/2 (or -Vdc and -Vdc/2) are generated during the positive (or negative) half-cycle of the mains voltage to control the line current. So, when input mains supply is reduced below the Vdc/2 value (keeping reference Vdc value constant) only region 1 is left for the operation of converter and hence the number of levels on AC side gets reduced. Thus, two such values are chosen for showing the difference. If the magnitude of Vs is reduced even below 70V, the results would be distorted more.

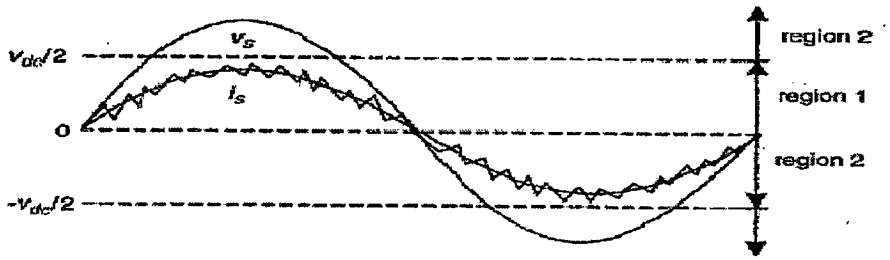


Fig. 2.8 Operating regions of a three level converter.

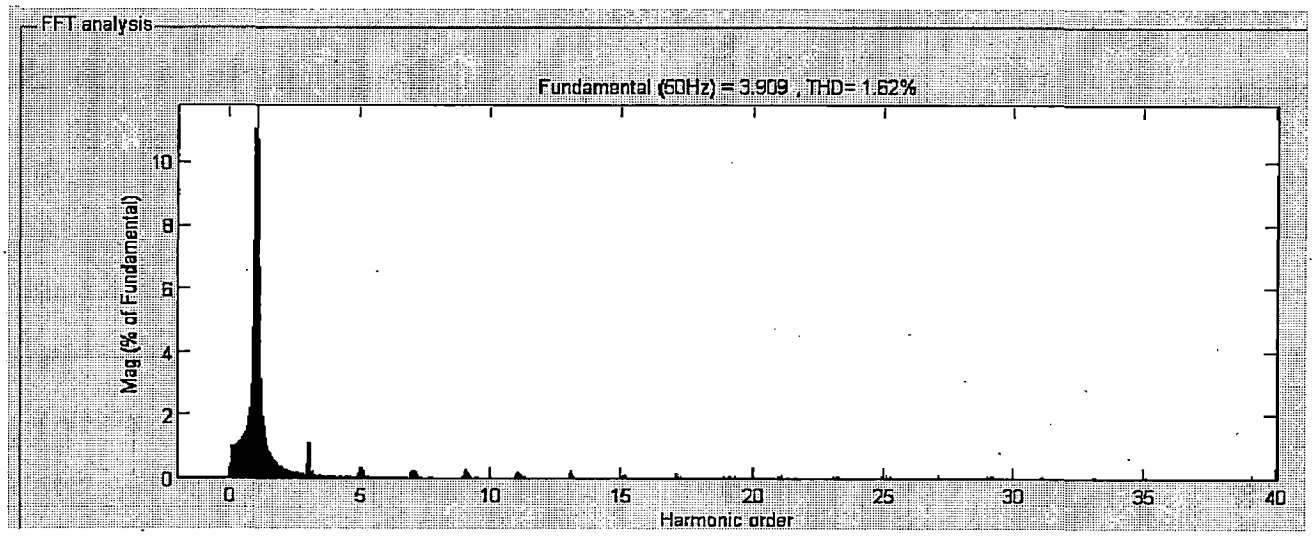


Fig. 2.9 FFT analysis with voltage 70V rms and load 1A.

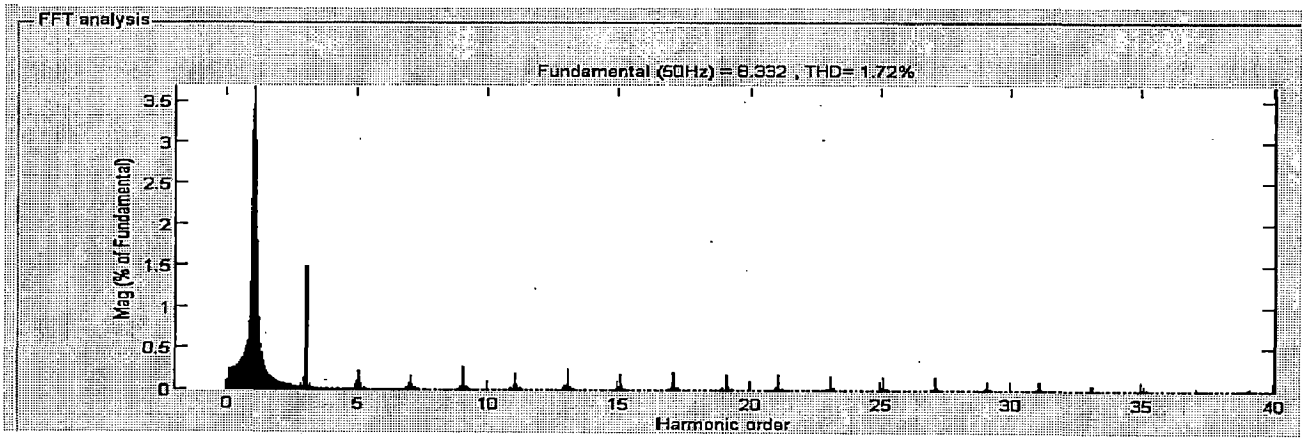


Fig. 2.10 FFT analysis for 70V rms supply and load of 2A.

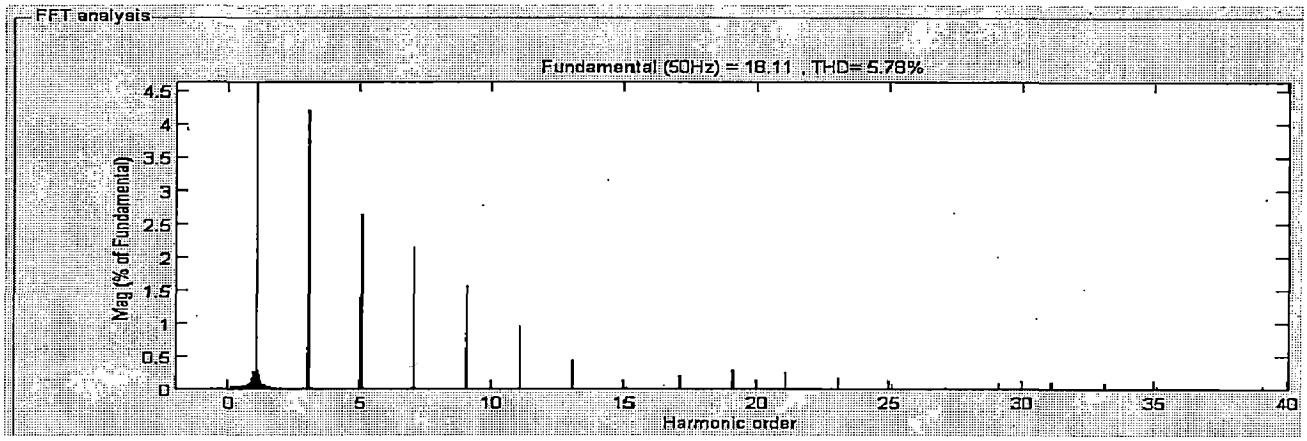


Fig. 2.11 FFT analysis for 70V rms supply and load of 4A.

Now we can summarize the above study of THDs with varying loads and input power supply as shown in table 2.1.

Input Voltage (rms)	Load current (A)	THD (%)
110	1	3.30
110	2	2.61
110	4	2.87
70	1	1.62
70	2	1.72
70	4	5.78

Table 2.1 Summary of THDs with varying load and supply voltage.

2.3.2 Simulations with RL load:

The topology shown in figure 2.1 is analyzed here with RL load in place of R load. Now the parameters are as given below. Load would be varied for different span of time.

Input voltage = 110V

DC output voltage = 200V

R load = 1A, 2A and 4A.

L load = 5mH, 3mH and 10mH.

Simulation results are shown in figure 2.12.

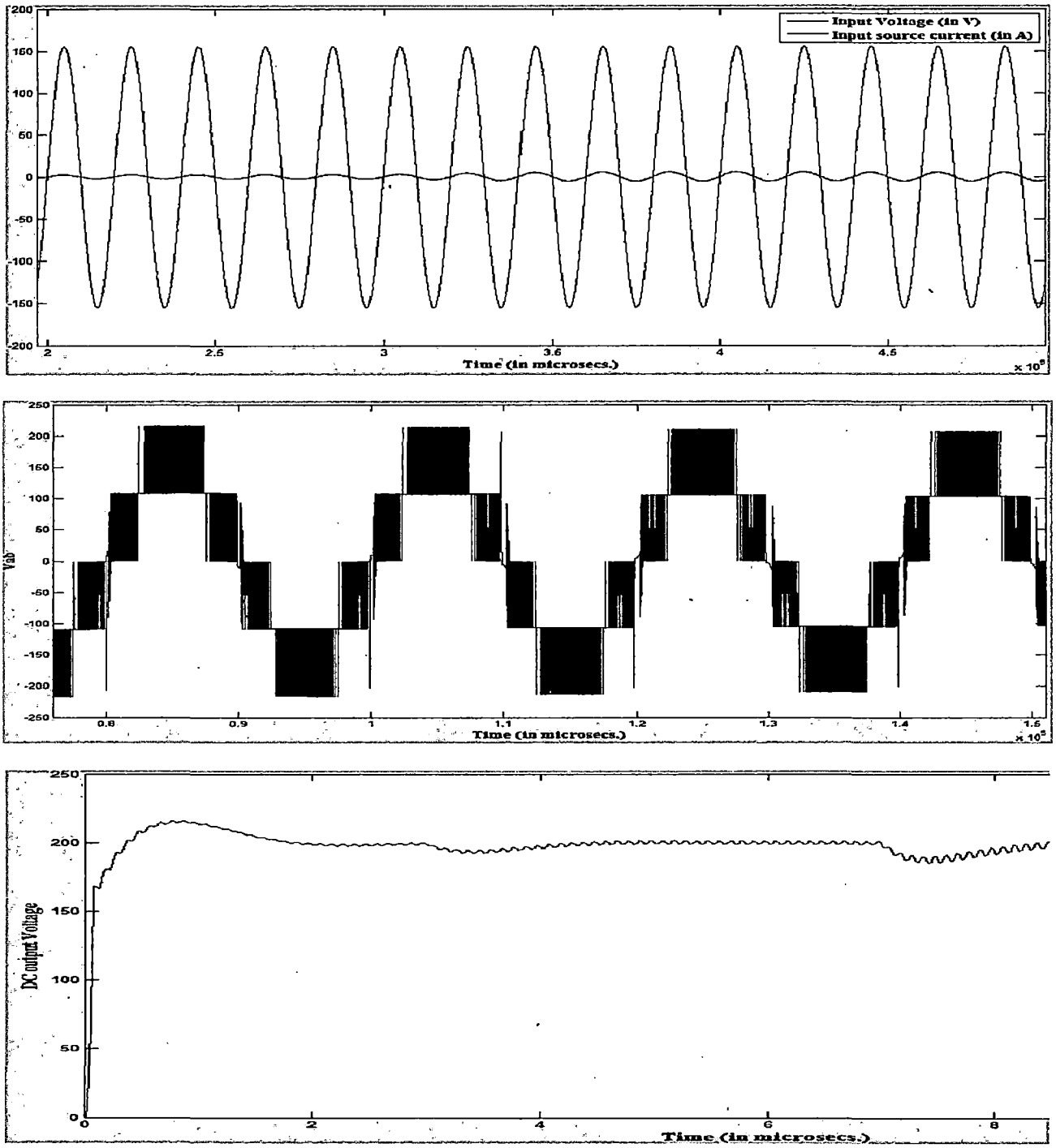


Fig. 2.12 Simulation results.

Input voltage (V)	Load current (A)	THD (%)
110	1	2.87
110	2	2.52
110	4	2.82
50	1	10.52
50	2	5.19
50	4	13.25

Table 2.2 Summary of THDs with RL load.

2.3.3 Conclusions:

From the table 2.2 we can analyze that after adding an inductive load in series with a resistive load there is not much change in the THD of input source current because of following reason:
This is an AC/DC converter and at the output end there are capacitors which get charged completely to a fixed voltage so there is hardly any change in the load current when we add inductor to the resistor already added previously. Hence, we can say that there is no need for the simulation results of other topologies.

2.4 Topology 2:

The second topology is the unidirectional diode clamped rectifier [29] which is as shown in figure 2.13. From now on only the resistive load is considered for all topologies. First the simulation results are shown for two level voltages where the control scheme produces the firing pulses for T1 and T2 exactly same and those for T1' and T2' exactly same.
The control scheme is similar to that shown in figure 2.2 except for the PWM generator which generates firing pulses for the rectifier since every topology has different sets of firing pulses. The simulation results for the following parameters are shown in figure 2.14.
Input power supply = 110V rms.
DC output voltage = 200V
R load = 1A, 2A, 4A respectively on same scope window so as to distinguish properly.

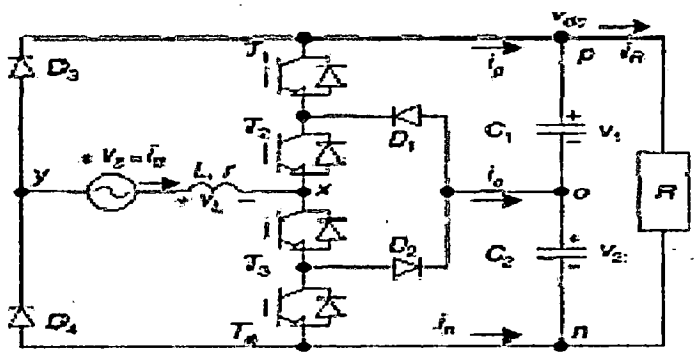
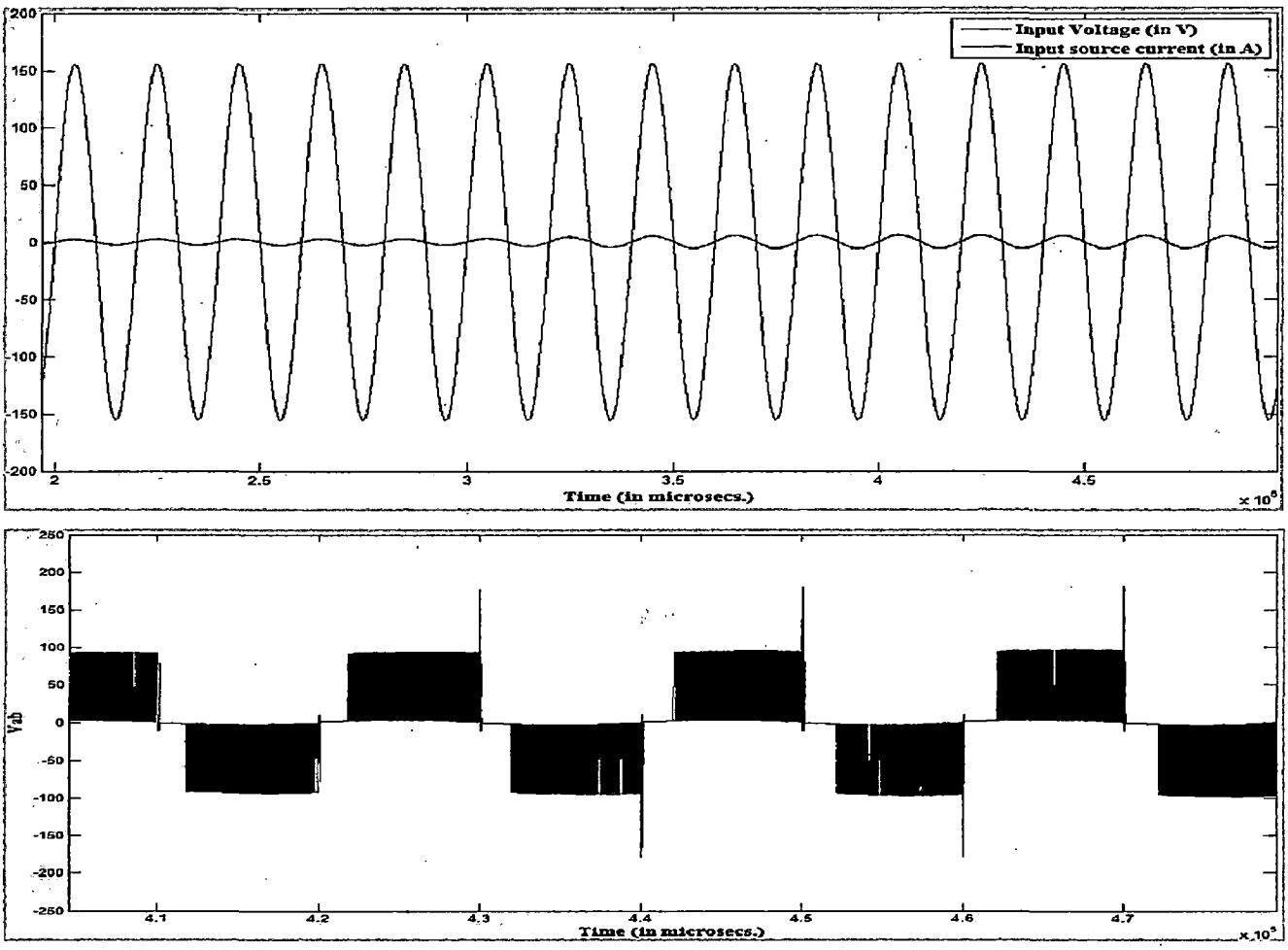


Fig. 2.13 Diode clamped rectifier.



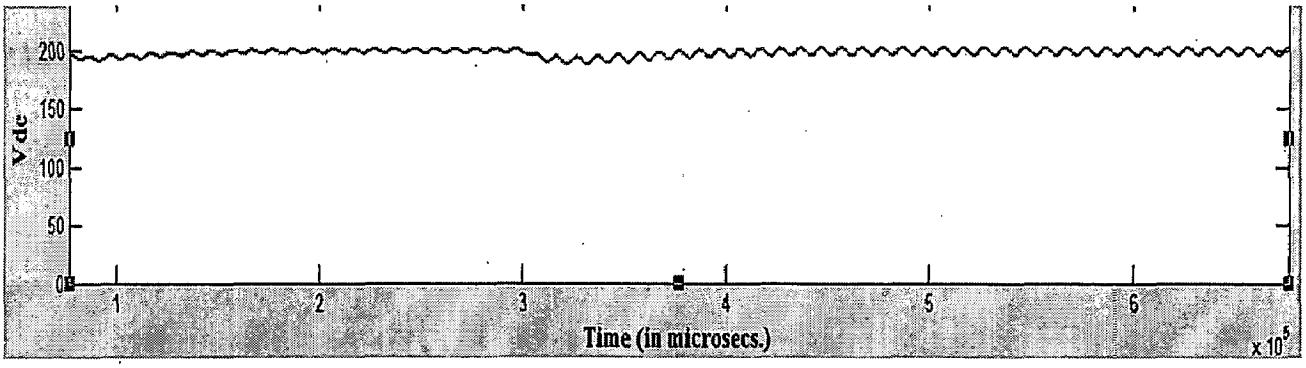
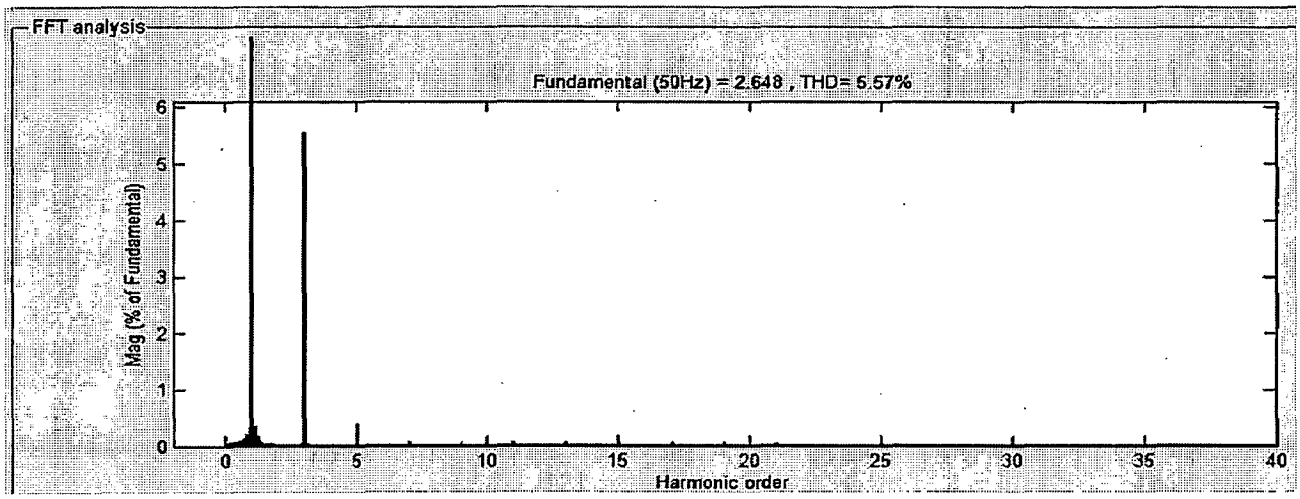
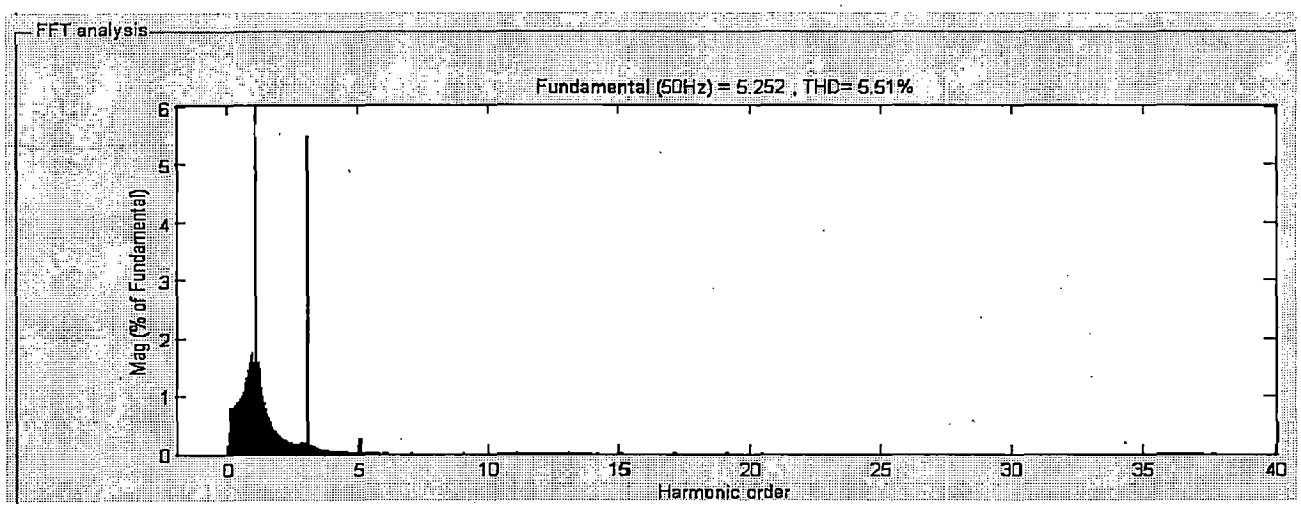


Fig. 2.14 Simulation results.

The simulation result for the input source current shows that it is increasing with increasing load current and DC output voltage is more rippled with increasing load current. Figure 2.15 shows the FFT analysis with varying loads of 1A, 2A and 4A respectively for 110V supply.





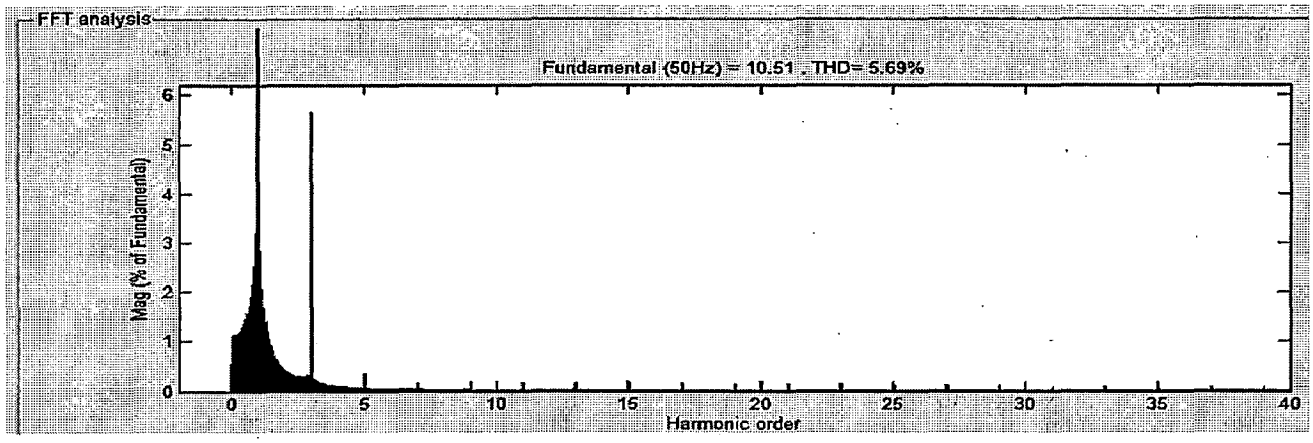
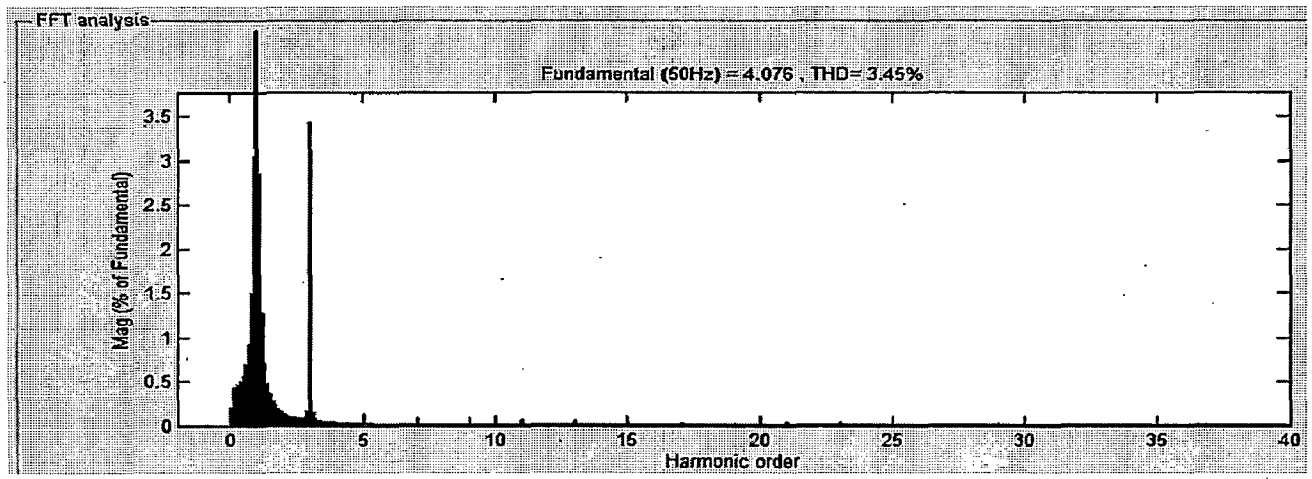
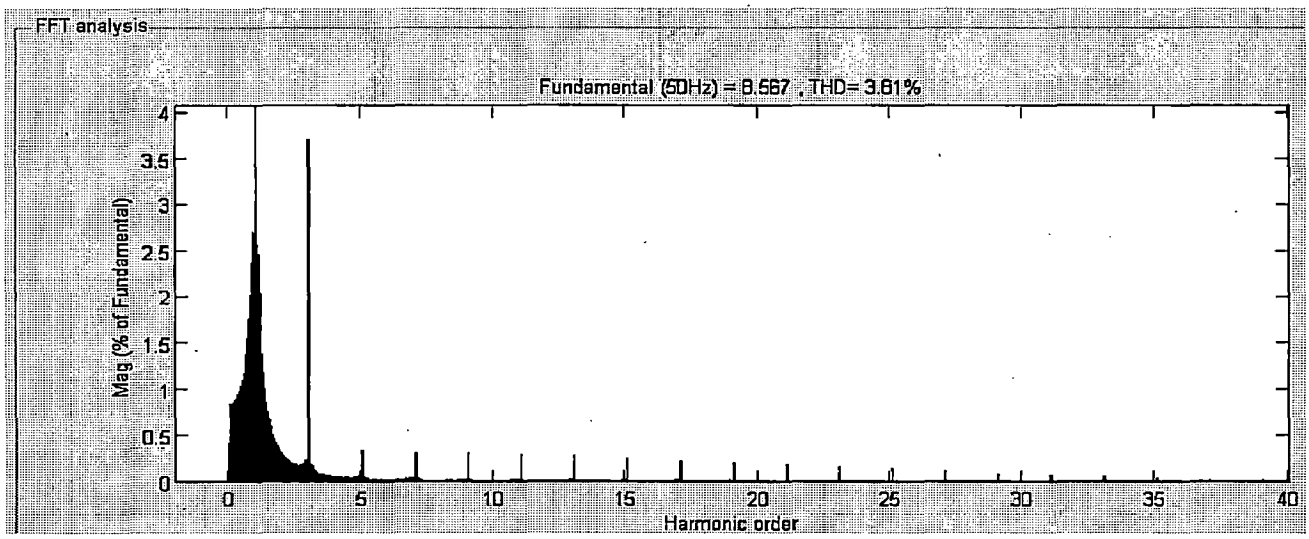


Fig. 2.15 FFT analysis for loads of 1A, 2A and 4A respectively.

The figure 2.16 shows the FFT analysis for loads of 1A, 2A and 4A respectively for 70V input voltage.





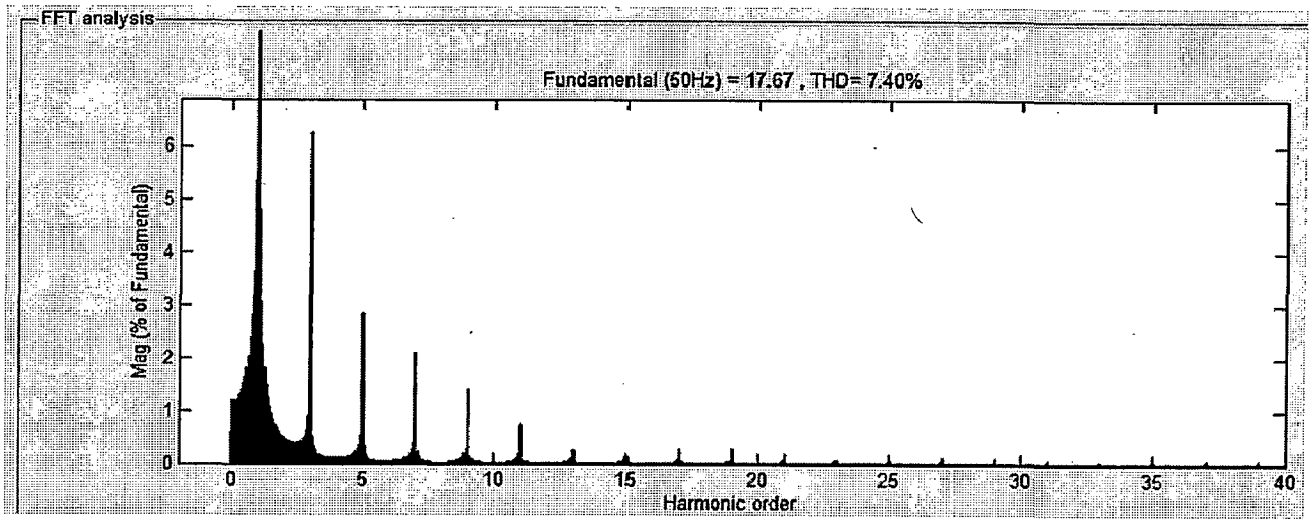


Fig. 2.16 FFT analysis for loads of 1A, 2A and 4A respectively with 70V rms.

Input Voltage (V rms)	Load Current (A)	THD(%)
110	1	5.57
110	2	5.51
110	4	5.69
70	1	3.45
70	2	3.81
70	4	7.40

Table 2.3 Summary of THDs with varying load and power supply.

Now we will see the simulation results for three level voltages for same topology with same control scheme but different firing pulses resulting in more number of voltage levels. We will follow the same sequence of supply and load for the convenience and simplicity. Again the parameters such as output voltage are same as earlier.

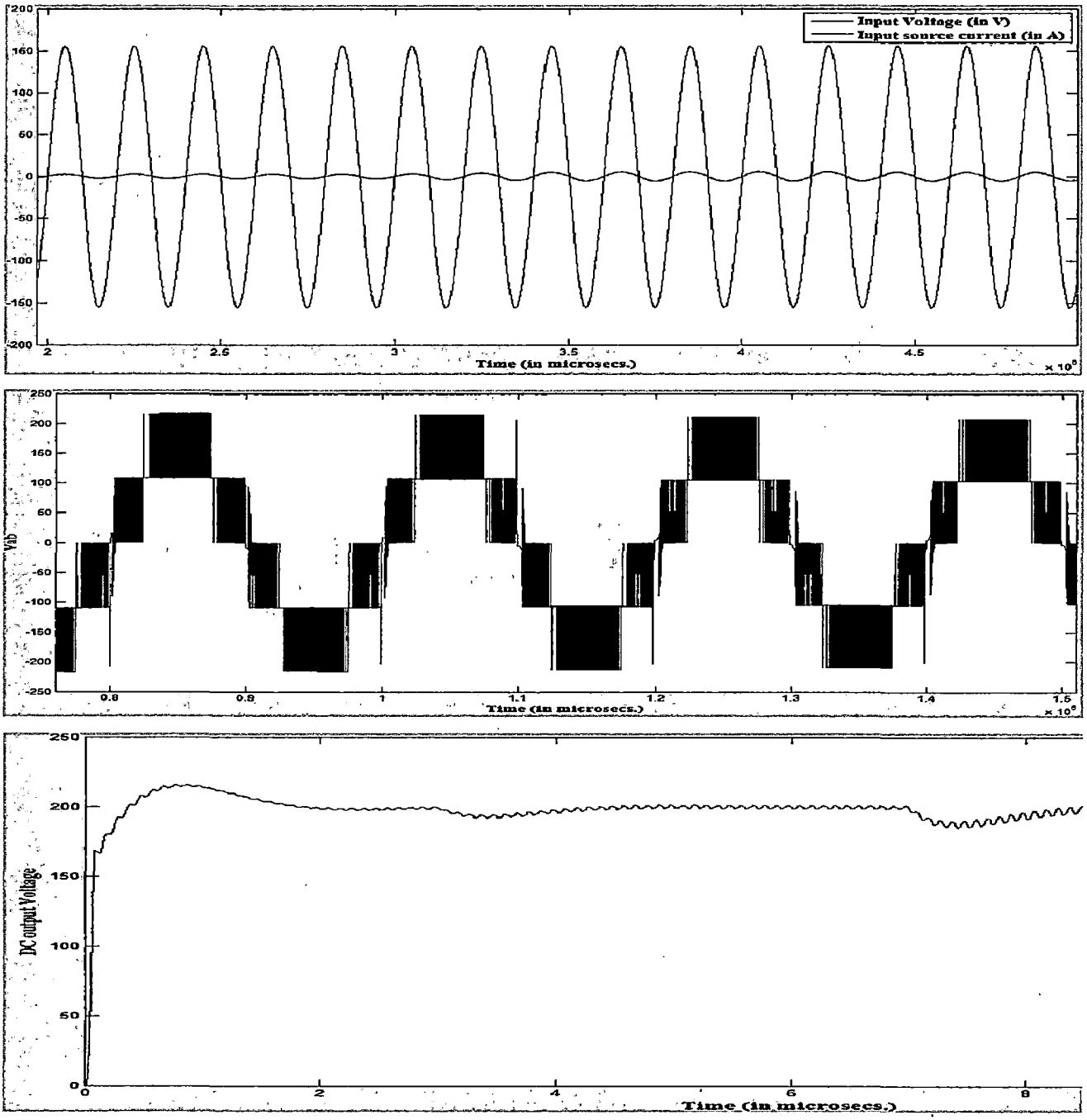


Fig. 2.17 Simulation results for three level voltages.

Now the simulation results for 50V rms supply is as shown in figure 2.18.

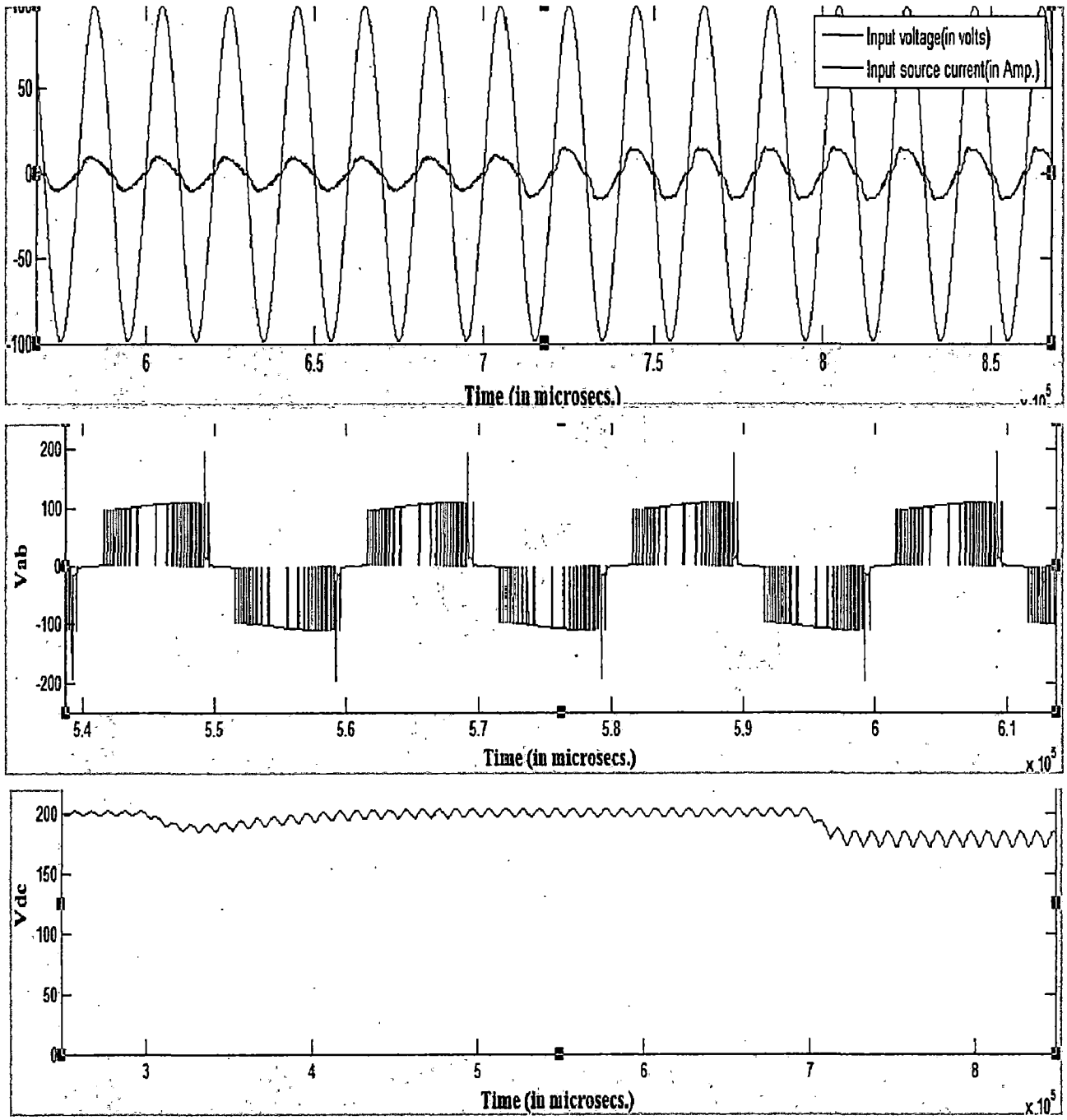


Fig. 2.18 Simulation results for supply of 50V.

In this case we can see that as we decreased the input supply keeping other parameters same as earlier, the output DC voltage is more rippled with decreased stiffness with increasing load. Level of voltages has also almost decreased to two with a kind of distortion in current waveform. Now we will summarize the THDs in table 2.4.

Input Voltage (V)	Load current (A)	THD (%)
110	1	7.73
110	2	9.37
110	4	11.52
50	1	9.06
50	2	15.02
50	4	20.88

Table 2.4 THDs with varying load and input supply.

2.5 Topology 3:

Next is bidirectional converter topology with neutral point clamped [30] as shown in figure 2.19. The control scheme used for this topology is shown in figure 2.20. In next figure (2.21) simulation results for steady state are also shown with following parameters: Input voltage supply = 110V, DC output voltage = 200, Load R = 1A, 2A and 4A.

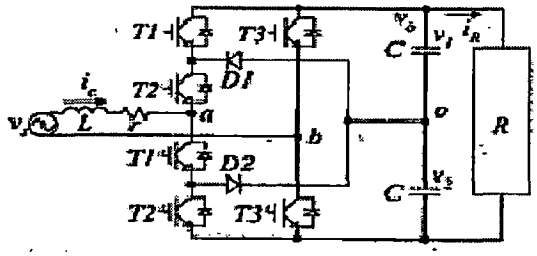


Fig. 2.19 Converter topology with neutral point clamped.

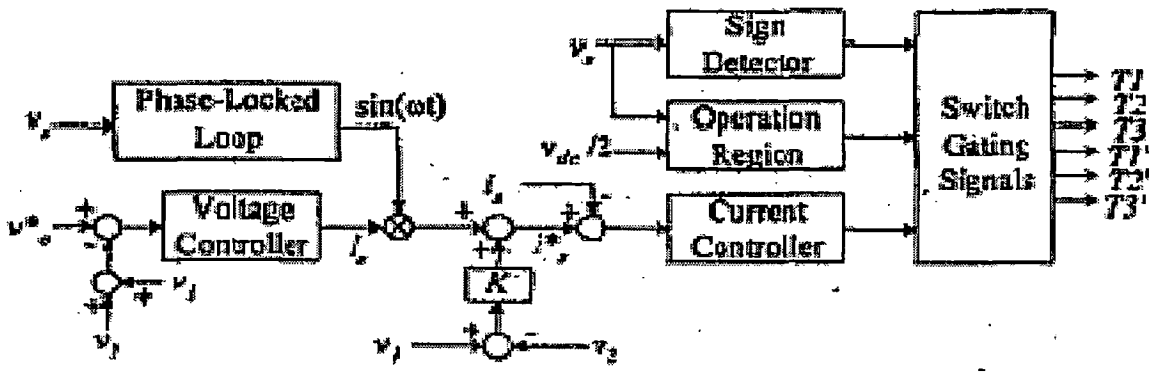


Fig. 2.20 Control block of above rectifier.

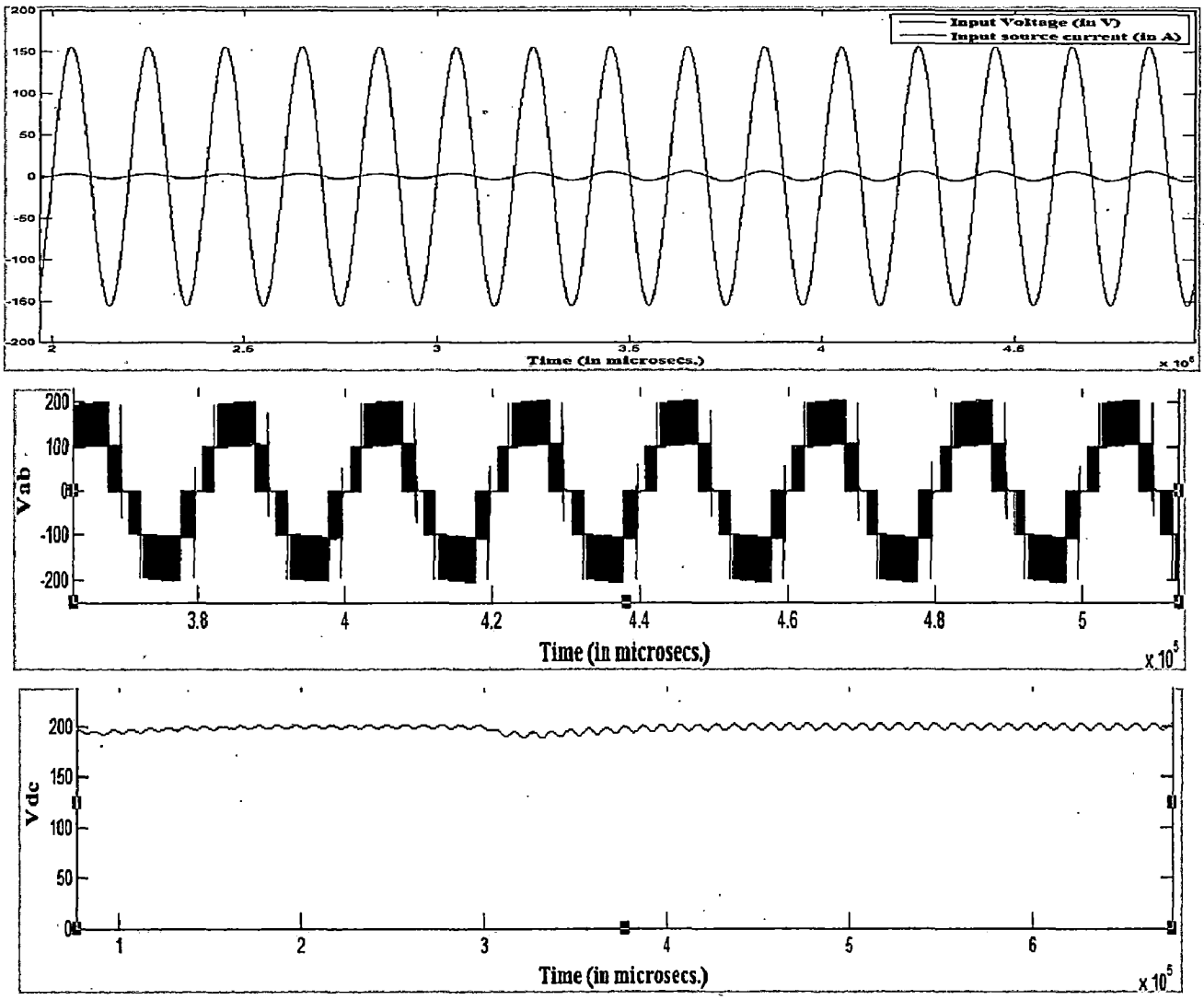
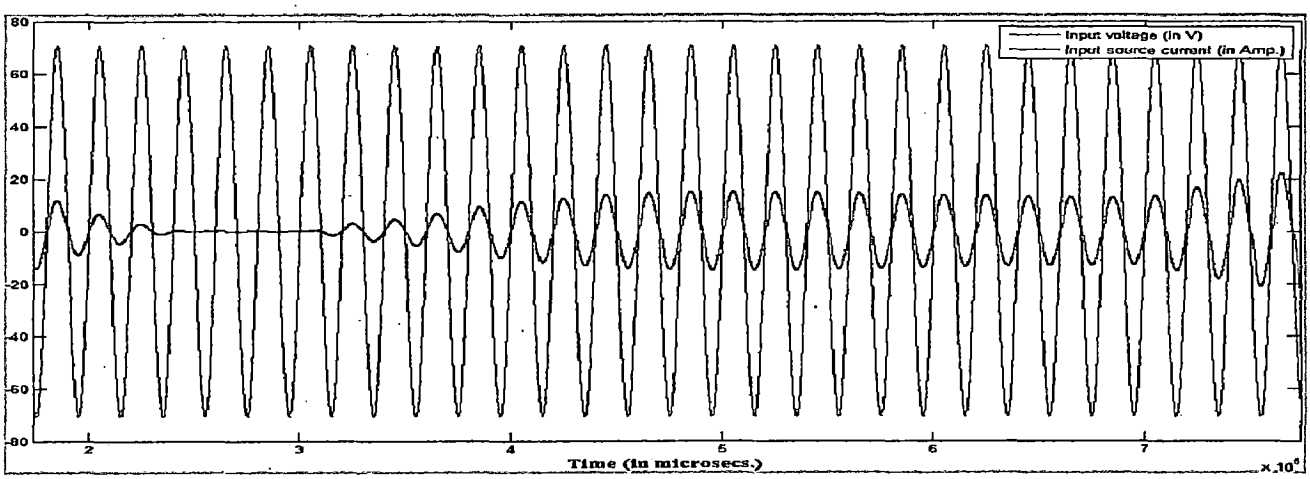


Fig. 2.21 Simulation results with three level for 110V supply.



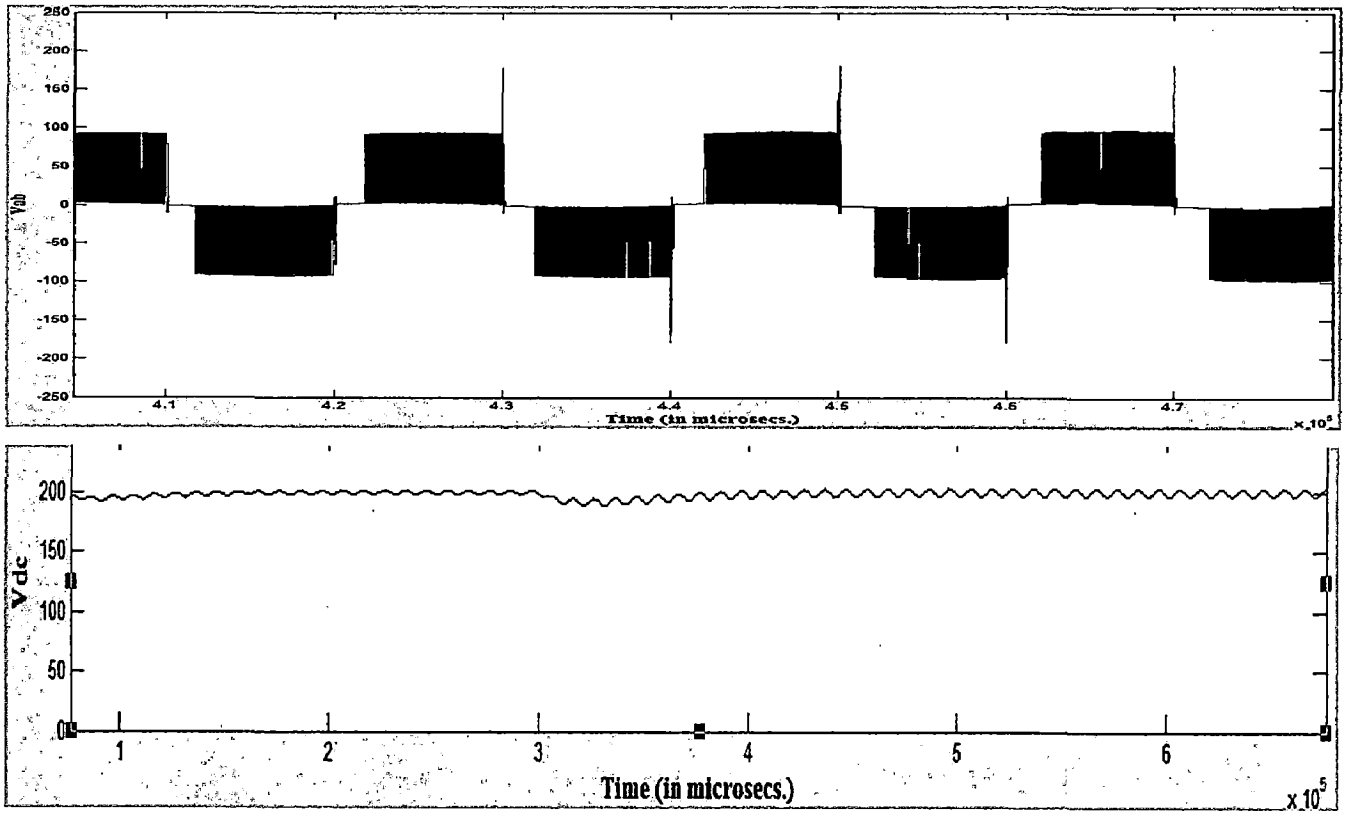


Fig. 2.22 Simulation results with 70V supply.

As we can see that the voltage levels have reduced. We can now see the summary of THDs with both varying loads and input supply in table 2.5.

Input voltage (V)	Load current (A)	THD (%)
110	1	4.92
110	2	4.93
110	4	5.60
70	1	5.71
70	2	6.97
70	4	10.79

Table 2.5 Summary of THDs with varying loads and power supply.

2.6 Topology 4:

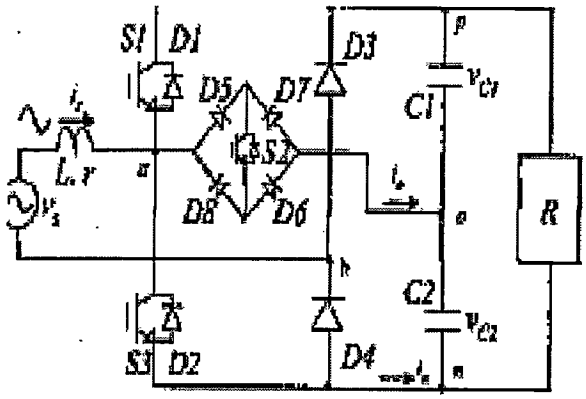


Fig. 2.23 Power circuit of neutral clamped AC/DC converter.

This is the fourth topology shown in figure 2.23 [24] with three switches and a diode bridge clamped in between. This topology can generate two level voltages and three level voltages as well. The simulations results are exactly same as seen for earlier topologies with two level and three level control schemes for following parameters: Input supply = 110V and 50V both, Output DC voltage = 200V and Load R = 1A, 2A and 4A. We can see the summary in table 2.6 and table 2.7 for two level and three level voltages respectively for THDs.

Input Supply (V)	Load current (A)	THD (%)
110	1	5.70
110	2	5.56
110	4	5.77
50	1	2.66
50	2	6.09
50	4	14.27

Table 2.6 Summary of THDs for two level voltages.

Input supply (V)	Load current (A)	THD (%)
110	1	5.40
110	2	5.01

110	4	5.56
50	1	2.45
50	2	5.59
50	4	10.25

Table 2.7 Summary of THDs for three level voltages.

2.7 Topology 5:

Next topology is the full bridge three level rectifier [31]. The power circuit (shown in figure 2.24) comprises a conventional full bridge rectifier in addition to an AC power switch which is built with two unidirectional switches connected in series. This topology also uses the simple PWM control scheme as used in previous topologies. The simulations results for the parameters as given below are shown in figure 2.25. Parameters are: Input mains voltage = 110V, DC output voltage = 200V, Load current = 1A, 2A, 3A and 5A.

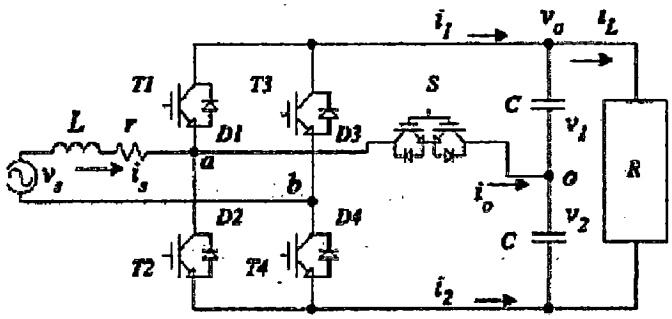
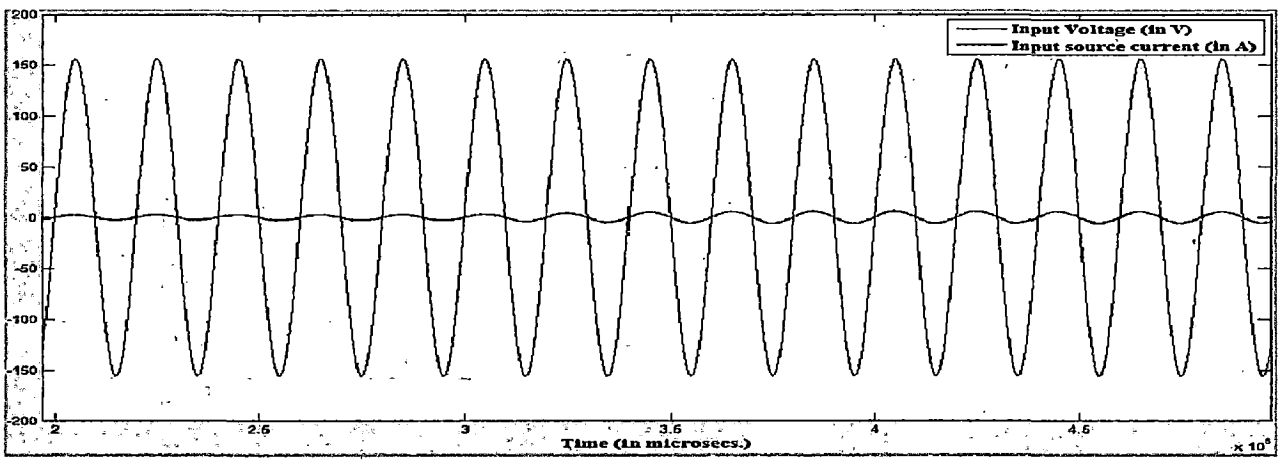


Fig. 2.24 Power circuit of a three level rectifier.



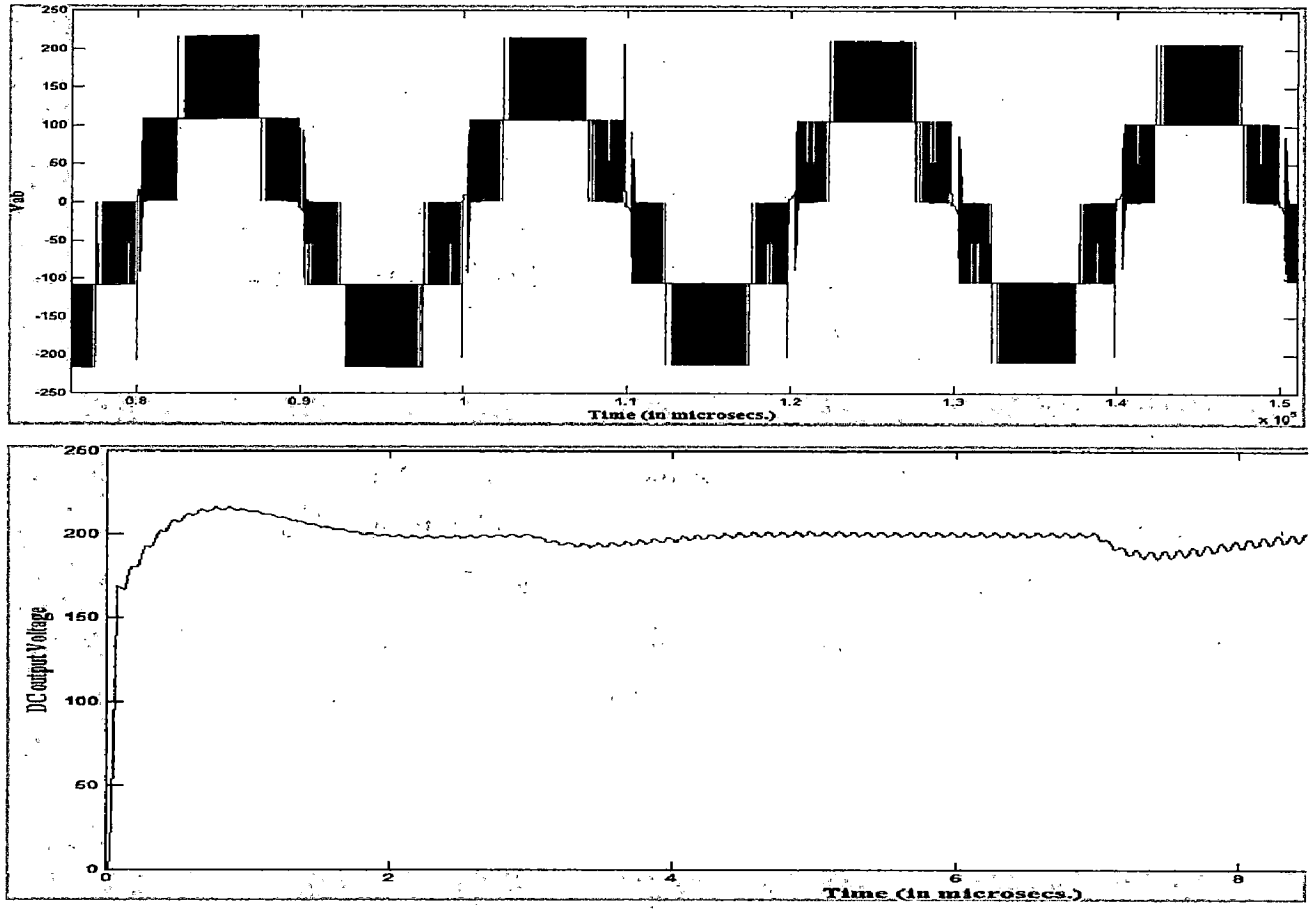


Fig. 2.25 Simulation results showing Input mains voltage, input source current, three level voltages and DC output voltage.

If we decrease the input mains voltage to 50V, the number of level will reduce to two and stiffness of the DC output voltage also decreases significantly as load increases.

Input Voltage (V)	Load current (A)	THD (%)
110	1	4.80
110	2	4.82
110	3	5.11
110	5	5.94
50	1	4.97
50	2	8.64

50	3	12.7
50	5	19.74

Table 2.8 Summary of THDs.

2.8 Topology 6:

Next topology is a single phase bridge rectifier [32] comprising a diode bridge and two power switches. Its power circuit is as shown in figure 2.26. This topology also uses the same control scheme as mentioned earlier. The simulation results for the parameters as used in other topologies are shown in figure 2.27. Then a table of summary is given in table 2.9.

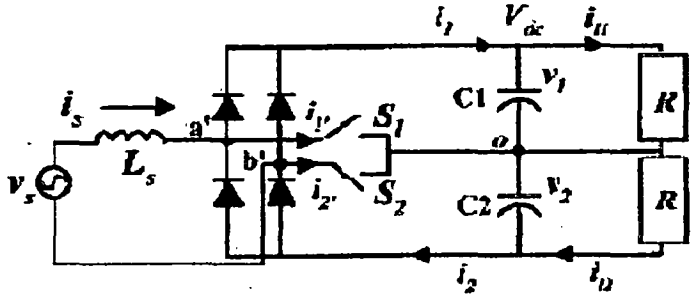
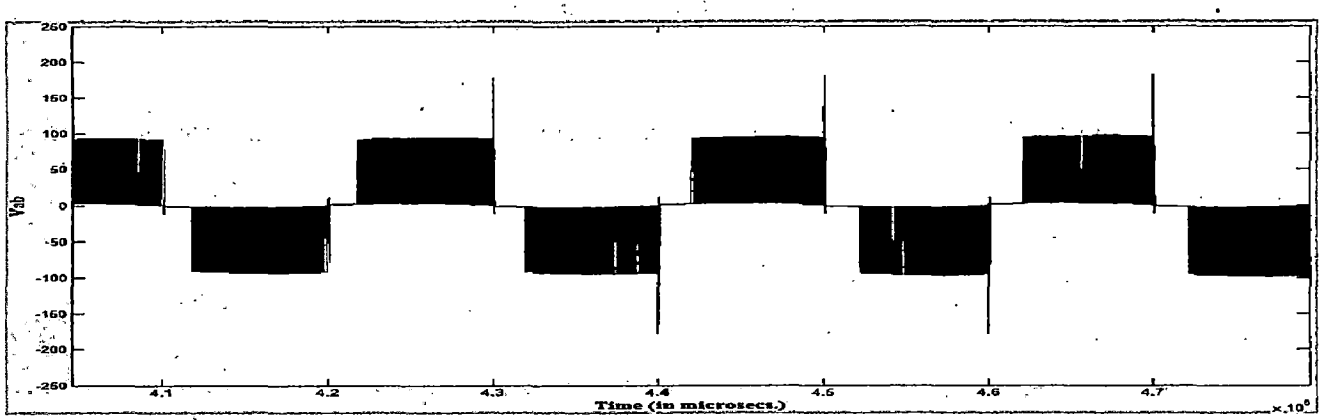


Fig. 2.26 Power circuit.



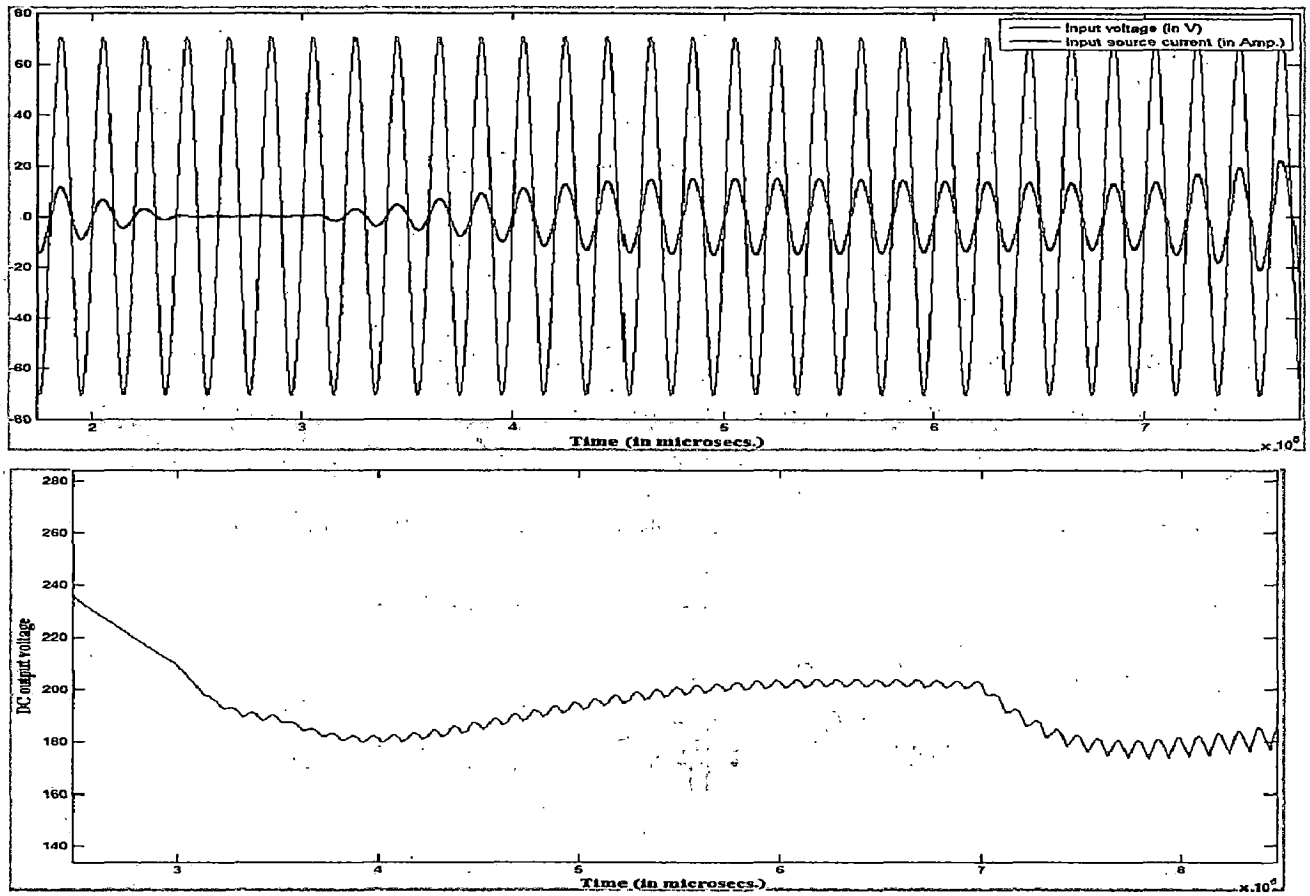


Fig. 2.27 Simulation results showing input voltage, input current, two level voltages and DC output voltage.

Input voltage (V)	Load current(A)	THD in input source current(%)
110	1	2.68
110	2	2.84
110	4	3.33
50	1	2.96
50	2	5.36
50	4	10.98

Table 2.9 Summary of THDs of input source current.

2.9 Topology 7:

Next topology is the bidirectional capacitor clamped converter [25]. This topology is been explained in detail in next chapter. The simulation results for the same parameters as used before are shown in figure 2.28.

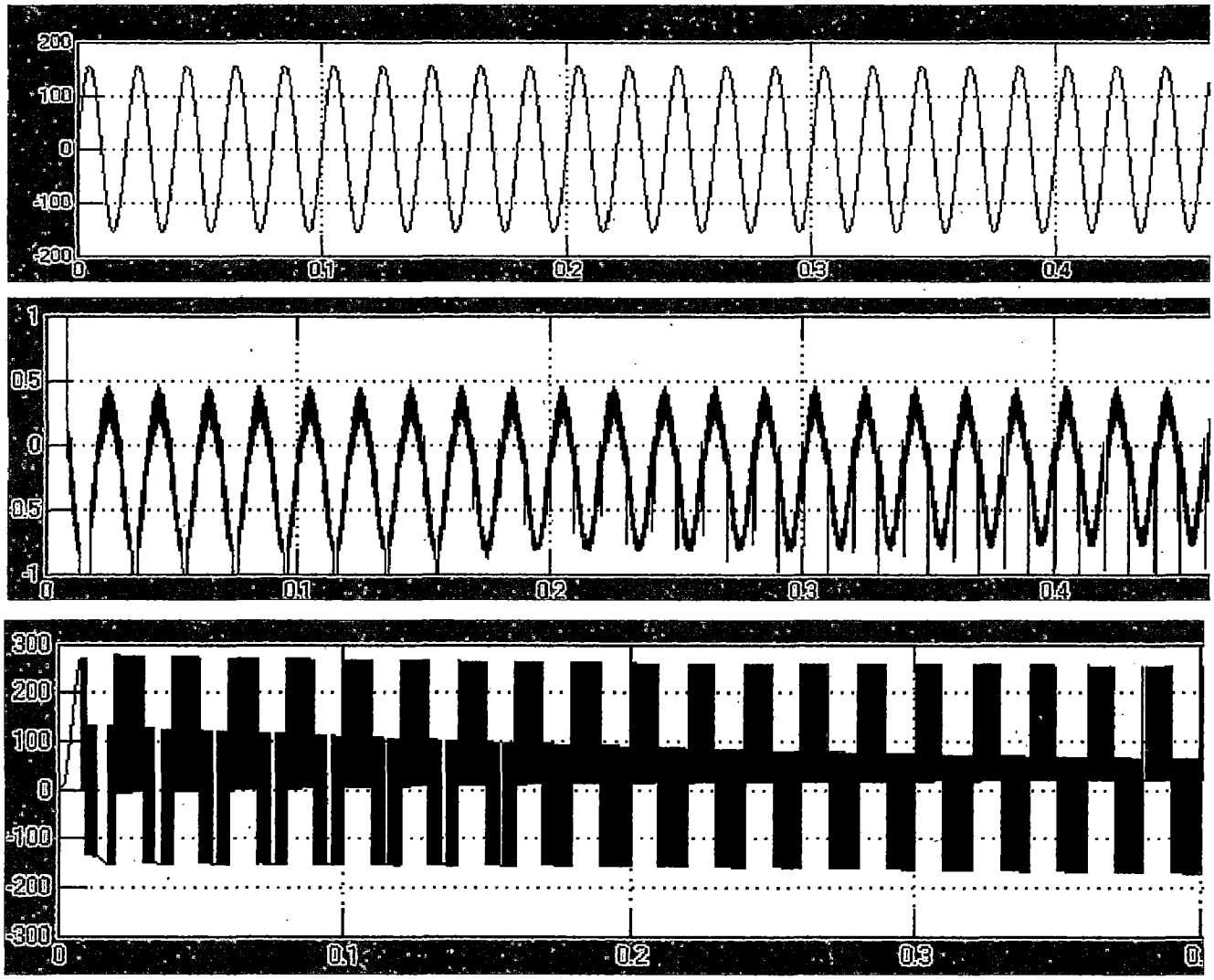


Fig. 2.28 Simulation results showing input voltage, input current and two level voltages.

2.10 Conclusion:

After having a deep analysis of all aforementioned topologies with R load, the study of THDs with varying load and varying input voltage supply, we can conclude the following results with certain justifications.

1. THD increases as the number of levels decrease. The reason being that as voltage levels are synthesized in small steps they get closer to a sinusoidal shape hence reducing THDs. This is what happens when the input voltage reduces decreasing number of levels and hence the THD increases.
2. Secondly, DC output voltage gets more rippled when the load current increases thus showing that the stiffness of the voltage source decreases with increasing load. This is because of the unequal charging and discharging of the DC link capacitors. The ripple voltage increases to around 20 volts at the maximum load current of 5A which is the limit kept here.
3. Thirdly, with increasing load current the THD increases in case of R load. This is due to the voltage unbalance of the capacitors which distorts the current waveform hence increasing the THD.

Chapter 3: FPGA application to Multilevel converters

3.1Background:

The use of any digital controller is the need of hour today because of the complex control strategies employed in the converters to achieve the improved power quality. These control strategies otherwise employ too much complicated hardware circuitry which again increase the bulk and cost of these converters.

The analog PFC approach is very straightforward. However, it has the following limitations:

1. Non-linearity of the multiplier. This could cause distortion when operating in a wide input voltage range.
2. Inflexibility of the circuit. When there is a change in the rectifier, parameters of the PFC control circuit generally need to change. For products in production stage this is extremely inconvenient when new component or sometimes even new layout is required.
3. In a switching environment, an analog circuit with many discrete components may be more susceptible to noise and hence affect proper function of the control circuit.

Thus the need for digital control arose because of following reasons:

1. Adjustment of control parameters. such as gains and bandwidth, is through software, hence more convenient.
2. Various control schemes can be realized through, which in the case of an analog controller might be difficult if not impossible.
3. As for practical implementation. it will reduce the component counts, which will lead to reduced material and assembly cost.
4. Digital processing inside these controllers offer high immunity to circuit noise and hence a more robust and reliable controller can be achieved.

Now the question arises that which controller to go for? Let us first go back to some of the controllers which have been in existence for long.

The idea behind was to construct combinational logic circuits that were programmable. Secondly they have an advantage over microprocessors in terms of programmability at hardware level besides running a program. The first PLDs were called PAL (Programmable array logic) or PLA (Programmable Logic Array) depending on the programming scheme. These chips collectively were known as SPLDs (simple programmable logic devices). Then came complex PLDs (CPLDs). CPLDs are currently very popular due to their high density, high performance, and low cost (CPLDs under a dollar can be found). There are some other controllers present as well such as DSPs (digital signal processing Controller). To implement any design or algorithm for any application employing software control designers need to keep following things in mind as follows:

Firstly, the platform should support multiple inputs of sensors, further multiple interfaces with different protocols of interfaces, which is the basic and key property.

Secondly, the process core on the platform should be flexible and easy enough to implement different algorithms.

Finally, process core should have great computing power and the complex calculation of the tested algorithm can be finished in predictable time, which also mean real-time.

Let us start with DSP controllers which are also very popular in digital control of Power converters. Technology advancements, such as faster processing speed, built-in pulse width modulator (PWM) outputs, and on-chip analog-to-digital (A/D) converters, are extending their applications to real-time power electronics circuits. Compared with traditional analog control methods, digital implementation using a DSP offers many distinctive advantages, such as a standard hardware design, easier implementation of sophisticated control algorithms, and flexibility of modifying designs to meet a particular customer need. However, using DSPs to control power supplies has its own unique challenges. Limited bandwidth and limited sampling frequency, discretizing effects, and processing delays tend to compromise the performance of a real-time control system. Since DSPs just begin to gain some serious considerations in controlling power supplies, many issues pertinent to the design and implementation remain unsolved.

These all core properties are very well met by FPGAs which came into existence in mid 1980s. FPGAs (Field Programmable Gate Arrays) differ from CPLDs in architecture, technology, built-

in features, and cost. They are aimed mainly at the implementation of large size, high-performance circuits.

3.2 FPGA: An overview:

A **field-programmable gate array (FPGA)** is an integrated circuit designed to be configured by the customer or designer after manufacturing, hence "field programmable". It is a scalable chip architecture based on a 2-D array of simple computational cells with individually configuring processing functions. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of a portion of the design and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost) offer advantages for many applications. Figures below show example of FPGAs popular nowadays.

FPGA has flexible I/O configuration which make it feasible for design of multiple sensors' data path. The logic circuits in FPGA are programmable so that the configuration of system can be very flexible. Due to the hardware level parallelism, the computing power of FPGA makes the system meet the demand of real-time in data processing.

With respect to security, FPGAs have both advantages and disadvantages as compared to ASICs or secure microprocessors. FPGAs' flexibility makes modifications during fabrication a lower risk. For many FPGAs, the loaded design is exposed while it is loaded (typically on every power-on).

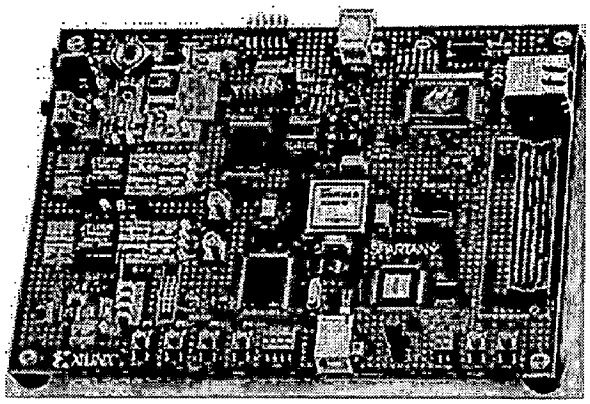


Fig. 3.1 Xilinx Spartan 6 FPGA board.

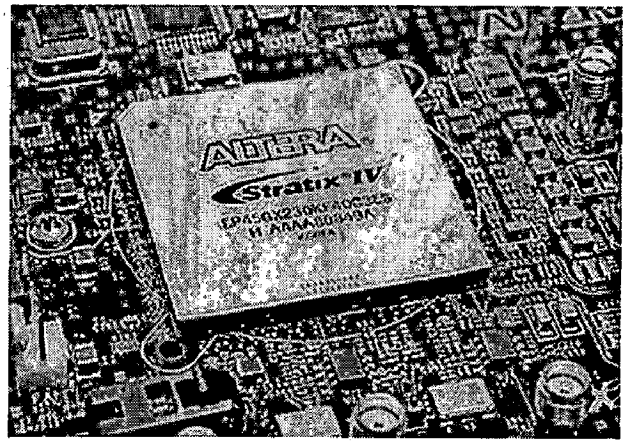


Fig. 3.2 Altera Stratix FPGA.

3.3 Designing with FPGAs:

Sophisticated CAD tools are available to assist with the design of systems using programmable gate arrays. One method of designing a digital system with FPGA uses the following steps.

3.3.1 Entering VHDL code:

Draw a block diagram of digital system, define condition and control signals and construct SM charts or state graphs that describe the required sequence of operations. Write a VHDL description of the system or it can be generated by the system generator of ISE Xilinx software which gets available when configured with MATLAB. Any block diagram in MATLAB SIMULINK file can be converted into VHDL code using system generator. Enter the code into the ISE Xilinx design suite and save it. Programming of FPGA chip can also be done by other hardware description languages as well such as Verilog and SystemC.

3.3.2 Synthesis and implementation:

After the VHDL code is written off, its syntax is first checked and necessary actions would be taken according to the report. When successful report is generated then it is synthesized by the ISE after clicking on the synthesize option. After the synthesis is concluded, view the synthesis report. Also check the RTL diagram. Now the design can be implemented. Double-click on the Implement Design option in the Processes for Source window. After the implementation is concluded, expand the Implement Design option and check the several reports produced, particularly the Pad Report (under the Place & Route directory). Check which pin was assigned to each signal.

3.3.3 Simulation:

Simulating design allows logic errors & design flaws to be resolved early in the process of development. Simulation is the act of verifying HDL or graphical digital designs prior to actual hardware implementation so as to get desired outputs. The circuit's input-signal characteristics are described in HDL that is then applied to design. This lets the coder or code tester observe the outputs' behavior. It may be necessary to modify the source code during simulation to resolve any discrepancies, bugs, or errors. Simulation can be done in ISE Xilinx design suite by creating test benches with certain timing diagrams. Firstly certain end limits are set for the timing diagrams as shown in figure 3.3.

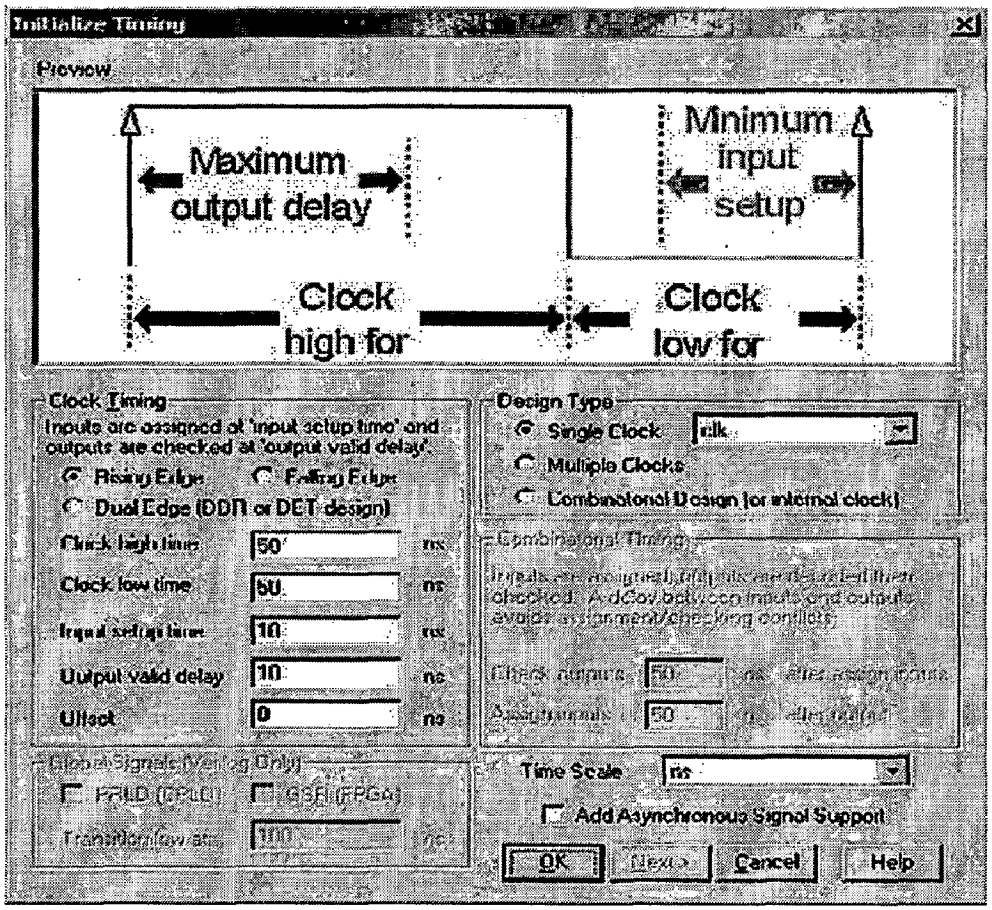


Fig. 3.3 Clock and time settings.

The simulation window appears after changing the setting in the process window to behavioral simulation in which the results can be verified.

3.3.4 Physical realization:

To physically implement the design in a FPGA chip, a development kit is necessary. Inexpensive alternatives are generally available through manufacturer's university programs, which offer design kits at low prices. The development kit must be connected to a PC running ISE in order for the chip to be programmed. A detailed description of how actually the FPGA chip is programmed will be presented in further chapter of this dissertation report.

3.4 Application of FPGAs:

FPGAs originally began as competitors to CPLDs but gained rapid acceptance and growth over the last decade because of their wide applications. Their applications include variety of areas as follows:

- ***Power Electronics***
- ***Image and Signal Processing***
- ***Medical Equipment***
- ***Wired and Wireless Telecommunications***
- ***Robotics***
- ***Automotive***
- ***Space and Aircraft Embedded Control Systems***
- ***Thermal Management and Packaging***
- ***Defense system***
- ***Speech recognition***
- ***Cryptography***
- ***Metal detection***
- ***Radio astronomy***
- ***Bioinformatics***
- ***Computer hardware emulation***

- ***ASIC prototyping***

These days the most important application of FPGA is its usage in distance learning by engineering students [33]. Students can use the software tools to design their circuits and then test them in real hardware implementation by using FPGA chip. In fact, FPGA has the usage in partial e-learning courses in which students can learn at home and create their designs by downloading certain softwares through internet. FPGA remote laboratory has been introduced for hardware courses in area of computer engineering to deliver the full e-learning courses.

3.5 Major Manufacturers:

Xilinx and ***Altera*** are the current FPGA market leaders and long-time industry rivals. Together, they control over 80 percent of the market, with Xilinx alone representing over 50 percent.

Both ***Xilinx*** and ***Altera*** provide free Windows and Linux design software which provides limited set of devices.

Other competitors include ***Lattice Semiconductor*** (SRAM based with integrated configuration Flash, instant-on, low power, live reconfiguration), ***Actel*** (antifuse, flash-based, mixed-signal),***Silicon Blue Technologies*** (extremely low power SRAM-based FPGAs with optional integrated nonvolatile configuration memory), ***Achronix*** (RAM based, 1.5 GHz fabric speed) who will be building their chips on Intels' state-of-the art 22 nm process, and Quick Logic (handheld focused CSSP, no general purpose FPGAs).

In March 2010, ***Tabula*** announced their new FPGA technology that uses time-multiplexed logic and interconnect for greater potential cost savings for high-density applications.

3.6 Limitations associated with FPGA system design:

Wide applications of FPGA in various fields as mentioned earlier and other advances in this technology have fuelled the drive towards Virtual Hardware development. An efficient FPGA based system design methodology is crucial in lessening the effects of the limiting factors and to meet the objectives.

Before discussing the problems we can have a look at the objectives to be attained by a FPGA based system as follows:

- Higher performance to meet the set goals demanded by the user.
- Utilization of area very efficiently to use a smallest FPGA possible to have an edge over the use of multiple processors.
- Short development and turn-around cycle with consistent results.
- Ease of RTL code migration from one FPGA vendor/family to another.

Following are the major limiting factors:

- Excessive delays in routes (up-to 80-90% of clock period) compared to logic delays after Place & Route process (P&R) when the device is densely packed with lots and lots of transistors used for various combinational logic within the cell.

- Limited by Synthesis and Place & Route tools based optimizations. Non optimal utilization of device is caused by the inefficiency in FPGA mapping which is the most important step and difficult as well. Circuits designed to be implemented into FPGA are optimized for either area or time. Thus mapping and routing results vary significantly with different tools and for different optimization procedures.

- Poor correlation between synthesis and P&R timing results causes multiple iterations.

- Variation in timing is caused even when minor RTL changes take place.

- Inconsistent timing results and violating paths even with minor RTL bug fixes or enhancements.

- For densely packed designs which is certain in some of the cases where circuits involve complexity to large scale for many applications, tool based optimizations are no better to yield major benefits.

3.7 Conclusion:

In this chapter, the brief introduction to FPGA is detailed, starting with origin of FPGA describing its history, its evolution and architecture, design process, problems associated with FPGA, market manufacturers of FPGA and applications are also included in this section.

Chapter 4: Implementation of Digital Control for Multilevel Rectifier

In this chapter design procedure of the control scheme developed for multilevel rectifier has been described.

For implementing the control algorithm of the multilevel rectifier SPARTAN 3 FPGA kit is used. In this system generator is used to generate code for the FPGA processor from SIMULINK model. So here it is not required to write the code which is a laborious task at times.

4.1. Software Details:

The softwares used are:

- Xilinx® Integrated Software Environment (ISE™) 10.1 with Xilinx service pack 3.
- MATLAB® Version R2008a.
- Xilinx System Generator for DSP 10.1.
- Xilinx System Generator Board Description Builder.

4.1.1 Xilinx® Integrated Software Environment (ISE™) 10.1 with Xilinx service pack 3

Xilinx® ISE 10.1 is a tool used for synthesis of Xilinx FPGA's. Xilinx ISE 10.1 supports Design Entry, Simulation, Synthesis, Implementation and downloading the configuration onto FPGA device.

Xilinx service pack 3 is an upgradation to Xilinx® ISE 10.1. Synthesis of a design is done in the following steps.

Brief descriptions about individual steps are given as bellow.

- Creating HDL Module

In this step the HDL module is created for the design which we want to configure onto FPGA. This is done using Xilinx ISE editor. The code is generated using system generator which gets available after Xilinx is configured with MATLAB.

- Simulation of Design

This is done to check the functionality of the design which is created so as to get desired outputs in the final stages. This is done either in steps or as a whole. One by one different designs are simulated or test bench can be created for the overall design.

- Setting Design Constraints

Setting constraints is important step in design implementation. In this step, we assign pin numbers of FPGA device for input reception and output display. Timing constraints are also included in this step.

- Synthesis and Design Optimization

The design is translated into gates and then optimized for the target architecture. RTL schematic can be checked for the proper architecture.

- Size and performance Evaluation

After Synthesis of design, we check whether design logic is sufficient for implementation on FPGA device. If design logic exceeds the resources available on FPGA chip, then we cannot implement the design. The design size and performance details are listed in Device Utilization summary of Synthesis report for analysis.

- Place and Route

Once synthesis is completed, the place and route process places the design into a Xilinx device. The steps comprise taking the synthesized net list through translation, mapping and place and route.

- Generate Bit Stream

Programming file is created only after all the requirements are met. It indicates the information needed to program the device. This file is called as bit stream file. The bit stream file is downloaded to the target device.

- Downloading

It is the process by which the bit stream of the design, as generated by Xilinx software, is loaded into the internal configuration memory (SRAM cells) of the FPGA.

- Creating a PROM, ACE or JTAG File

The configuration bit stream file can be saved in PROM, so that configuration details are not erased from chip when Power is turn off.

4.1.2. MATLAB

MATLAB® is a high-performance language for technical computing and a very interactive system whose basic data element is an array that does not require dimensions. In this dissertation MATLAB® Version R2008a is used. MATLAB has various applications such as it is used for mathematical computational tasks and can solve very complicated equations within no time. MATLAB is used to carry out functional Simulation and Synthesis for FPGA device configuration, using Xilinx System Generator Plug-in. MATLAB SIMULINK is a model based design, which provides an interactive graphical environment and a set of block libraries that lets us design, simulate, implement, and test a variety of designs. Xilinx System Generator block set

is added to SIMULINK after configuring it with MATLAB and many other blocks also get available after the configuration.

4.1.3 Xilinx System Generator

Another tool used for synthesis is Xilinx System Generator. It is a block provided by Xilinx in MATLAB SIMULINK. System Generator is a system-level designing tool that helps in creating FPGA hardware design. It broadens SIMULINK in many ways to provide an environment for modeling that is well suited to hardware design. The tool also provides access to underlying FPGA resources through low-level abstractions. It is a tool that makes the compilation of high level abstractions into FPGA chip just a push-of-a-button away. It also allows the construction of highly efficient and most complicated and complex designs very easily.

System Generator allows the construction of hardware designs which are specific to the device and can be created directly in a flexible high-level system modeling environment. In a System Generator design, signals are not just bits. They can be signed and unsigned fixed-point numbers.

System Generator blends the variety of ingredients to construct the hardware designs. Data flow models, traditional hardware design languages (VHDL, Verilog, EDIF and SystemC), and functions derived from the MATLAB programming language, can be used parallely, simulated together, and synthesized into working hardware. System Generator simulation results are bit and cycle-accurate. This means results seen in simulation exactly match the results that are seen in hardware. System Generator simulations are considerably faster than those from traditional HDL simulators, and results are easier to analyze.

4.1.4 Xilinx System Generator Board Description Builder

System Generator supports hardware co-simulation, making it possible to incorporate a design running in an FPGA directly into a SIMULINK simulation. In layman words, we can say that all the inputs and outputs are shown in a box to check for any missed out signal or any correction.

The System Generator Board Description Builder makes it easy to add hardware co-simulation support for any board with a Xilinx FPGA.

4.2 Implementation of the control scheme with SIMULINK and system generator

System Generator provides a model of FPGA circuits with accuracy of bits and automatically generates a VHDL code which can be synthesized including Test bench. This synthesized VHDL design can be used for implementation in the Xilinx's FPGAs platform Design process for computing.

The control scheme used in this dissertation is simple PWM with hysteresis current control. So the complete process from generation of the code to the dumping into FPGA kit is described for this control scheme only. In this dissertation only one specific topology is implemented on hardware so only that control scheme is implemented onto FPGA and talked about in this chapter.

4.3 Simple PWM scheme:

The control scheme is developed in SIMULINK as shown in figure 4.1 below.

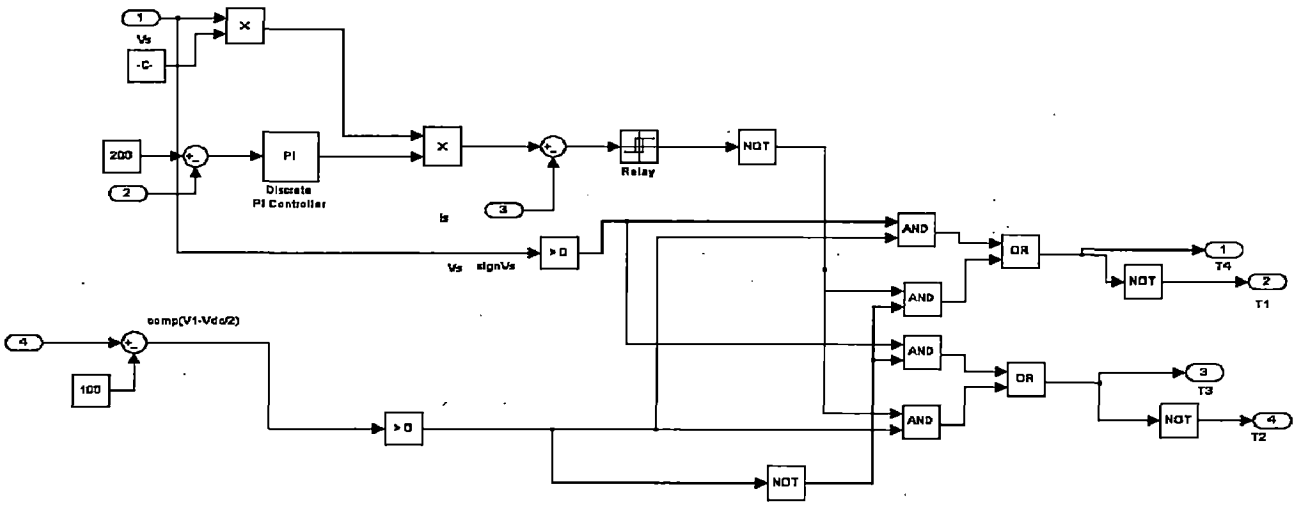


Fig. 4.1 Control scheme using sim power blocks in SIMULINK.

Now the same SIMULINK blocks are replaced by Xilinx system generator blocks, these blocks are appeared when the Xilinx 10.1 software is interfaced with the MATLAB 2008a as shown in Fig 4.2.

The following are the key steps in the design simulation process using MATLAB SIMULINK and System Generator:

- Start the design by implementing the Xilinx blocks in the MATLAB SIMULINK model design.
- Select the Xilinx System Generator block and add it on the top of the design hierarchy.
- "Gateway In" and "Gateway Out" blocks are used to define the inputs and outputs to the Xilinx design. Xilinx gateway blocks automatically converts the double precision floating point numbers from the MATLAB SIMULINK environment into the fixed point numbers for the Xilinx environment.

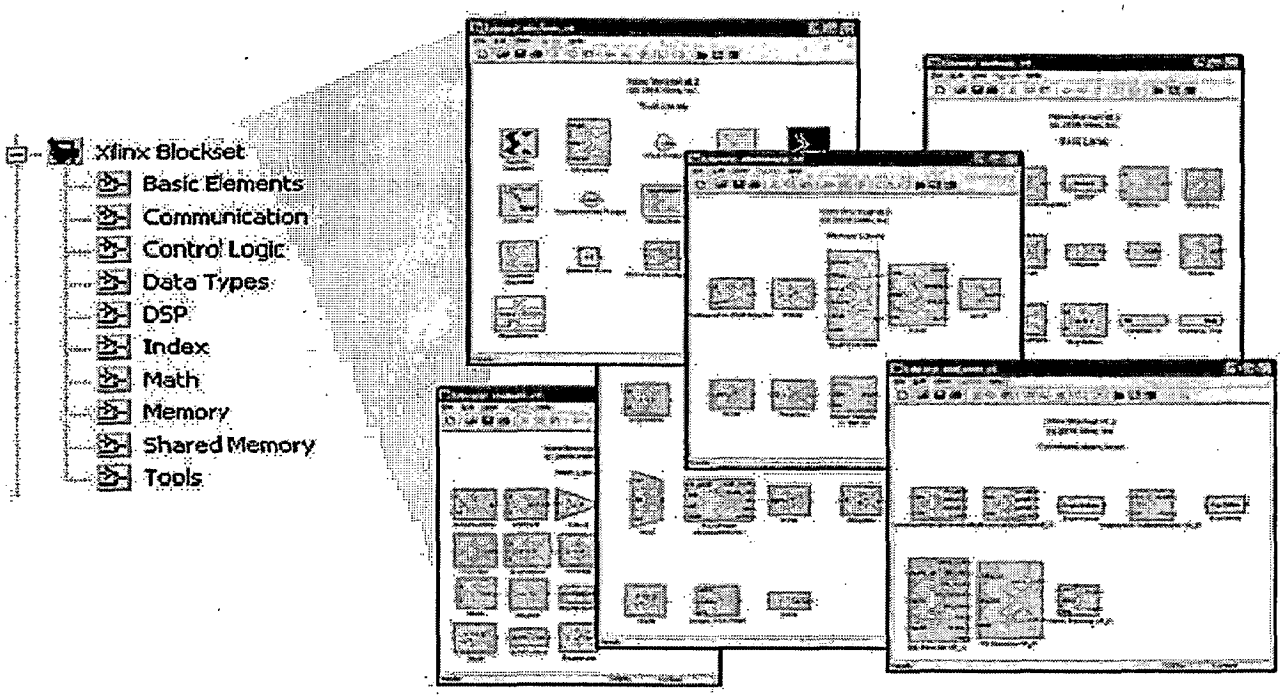


Fig. 4.2 Xilinx block set available in MATLAB SIMULINK.

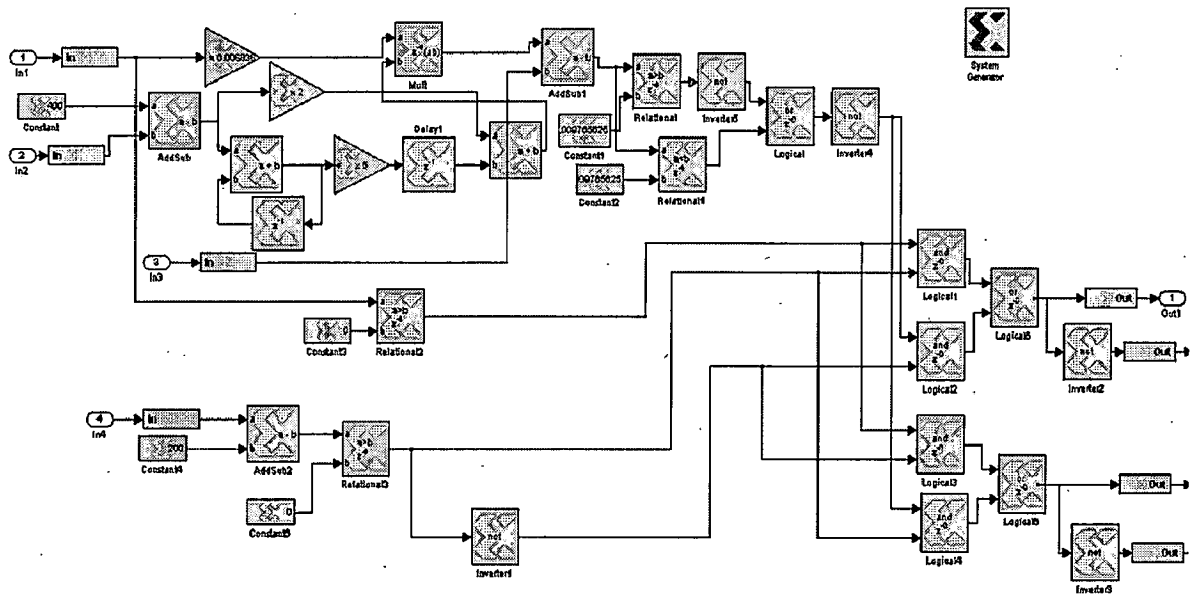


Fig. 4.3 Control scheme using Xilinx blocks in SIMULINK model.

All the system components inside the gateway blocks should be Xilinx blocks only. However, any other MATLAB SIMULINK blocks such as scope can be used to interface with Xilinx design and represented in system level.

The implemented control scheme using system generator blocks is shown in figure 4.3.

Now steps to generate code from the above system generator blocks as follows:

- Double click on system generator token and set compilation mode as shown below

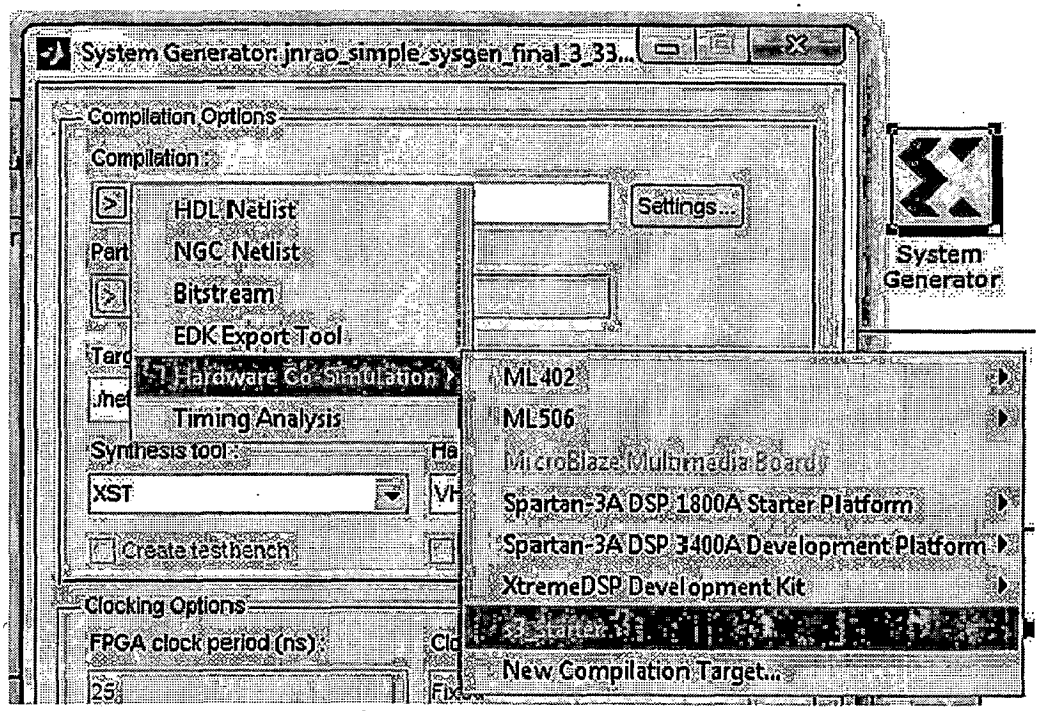


Fig. 4.4 Compilation settings of system generator.

4.4 Hardware Co-Simulation

Hardware Co-Simulation (HWCOSIM) is a great feature in System Generator (SysGen) that allows users to run the full or part of a SysGen design on the FPGA and increases the simulation speed significantly. SysGen already includes HWCOSIM plug-in for commonly used DSP demo boards. The System Generator will automatically synthesize, and place and route the design on the target FPGA platform upon selecting the appropriate options, such as compilation type, target FPGA, synthesis tool, and so on. The key steps in the hardware co-simulation process are summarized as follows:

- The hardware co-simulation platform can be chosen from the System Generator dialog box. When the compilation target is selected, the fields on the System Generator dialog box are automatically configured with settings appropriate for the selected compilation target.

- After initiating the "Generate" button, the code generator is invoked and produces an FPGA configuration bit stream for the design that is suitable for hardware co-simulation. System Generator not only generates the HDL code and net list files for the model during the compilation process, but it also runs the downstream tools necessary to produce an FPGA configuration file.
- After the FPGA configuration bit stream is created, a new hardware co simulation block is created by the System Generator and stored in the MATLAB SIMULINK library. Hardware co-simulation blocks can be used in the design with other MATLAB SIMULINK blocks. When the hardware co-simulation block is simulated, it interacts with the underlying FPGA platform and facilitates the design implementation and verification of the desired FPGA.
- Set target directory and SIMULINK system period and then click on "generate" button to generate code for system generator blocks.
- Process of generating code is as shown in below Fig 4.5.

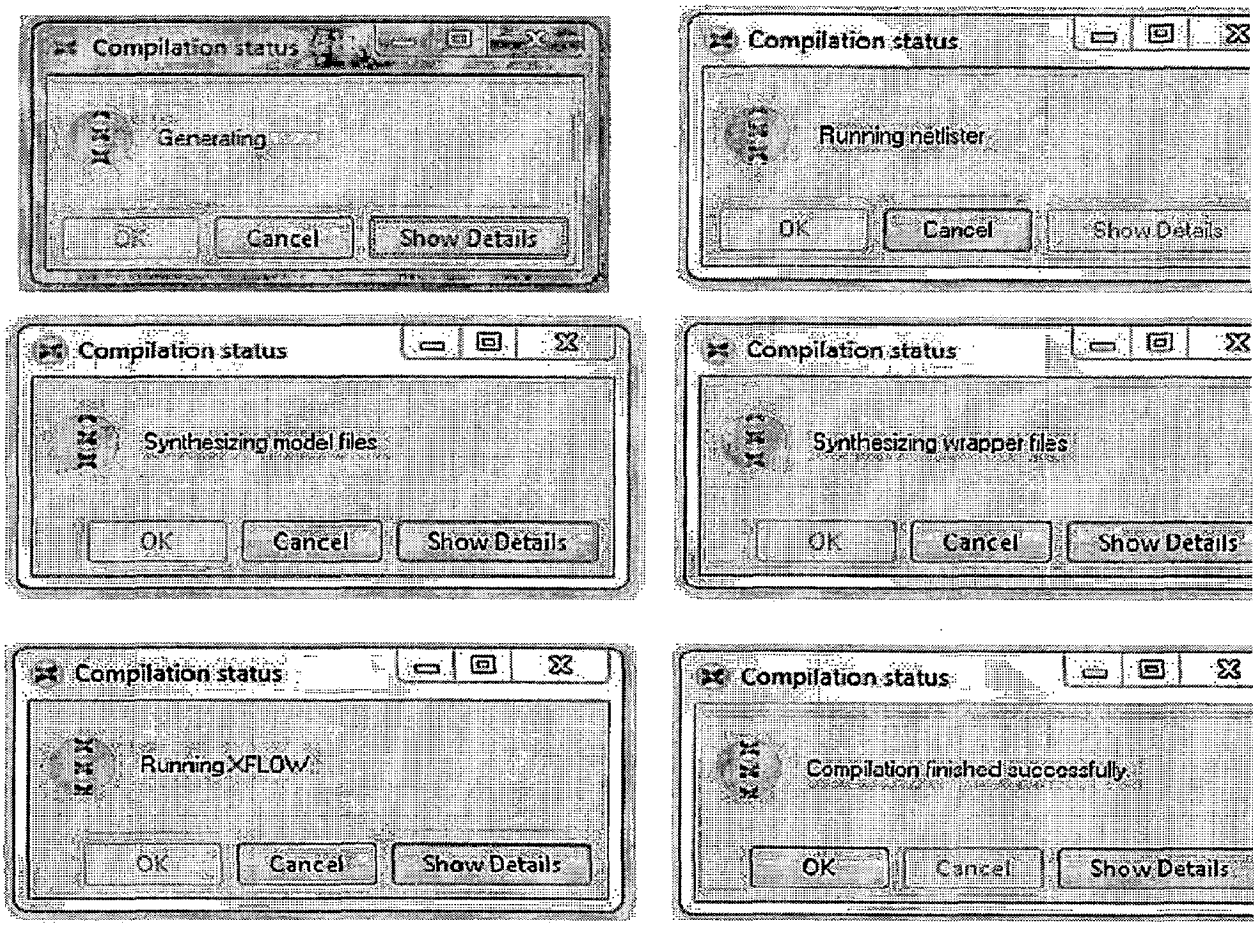


Fig. 4.5 Compilation Process.

Now the process for dumping VHDL code into the FPGA kit is as follows:

Open the folder containing the system generated code and double click on the ISE icon. The process window will appear as shown below in Fig. 4.6.

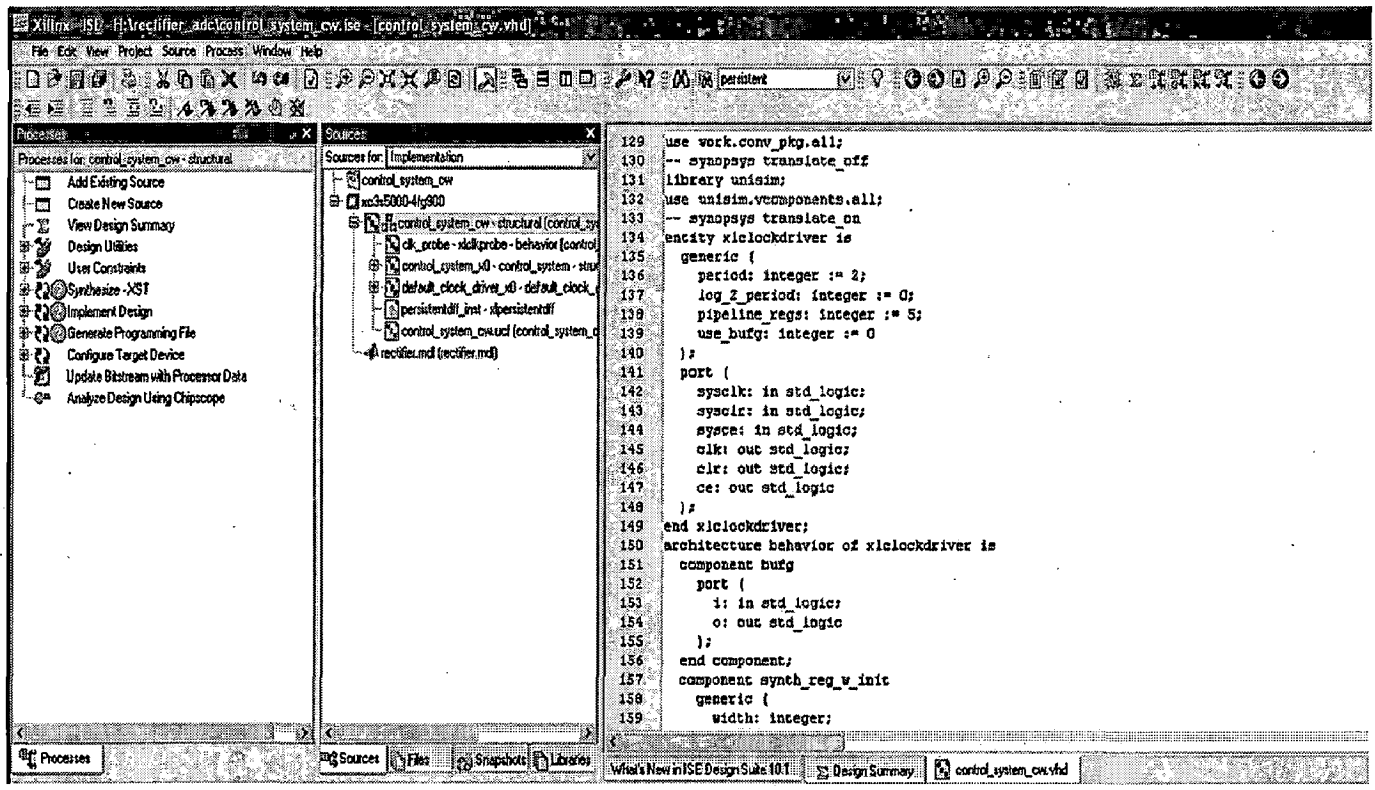
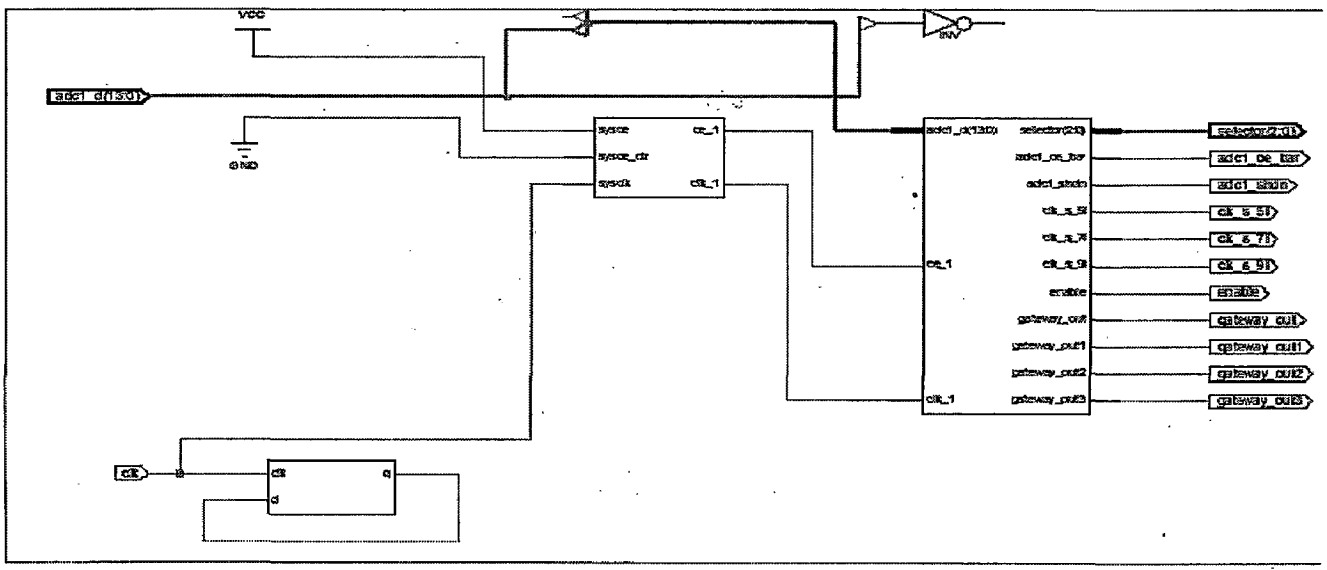


Fig. 4.6 Process Window with Code generated.

Check syntax errors and open RTL schematic diagram which represents the scheme implementation shown in Fig 4.7.



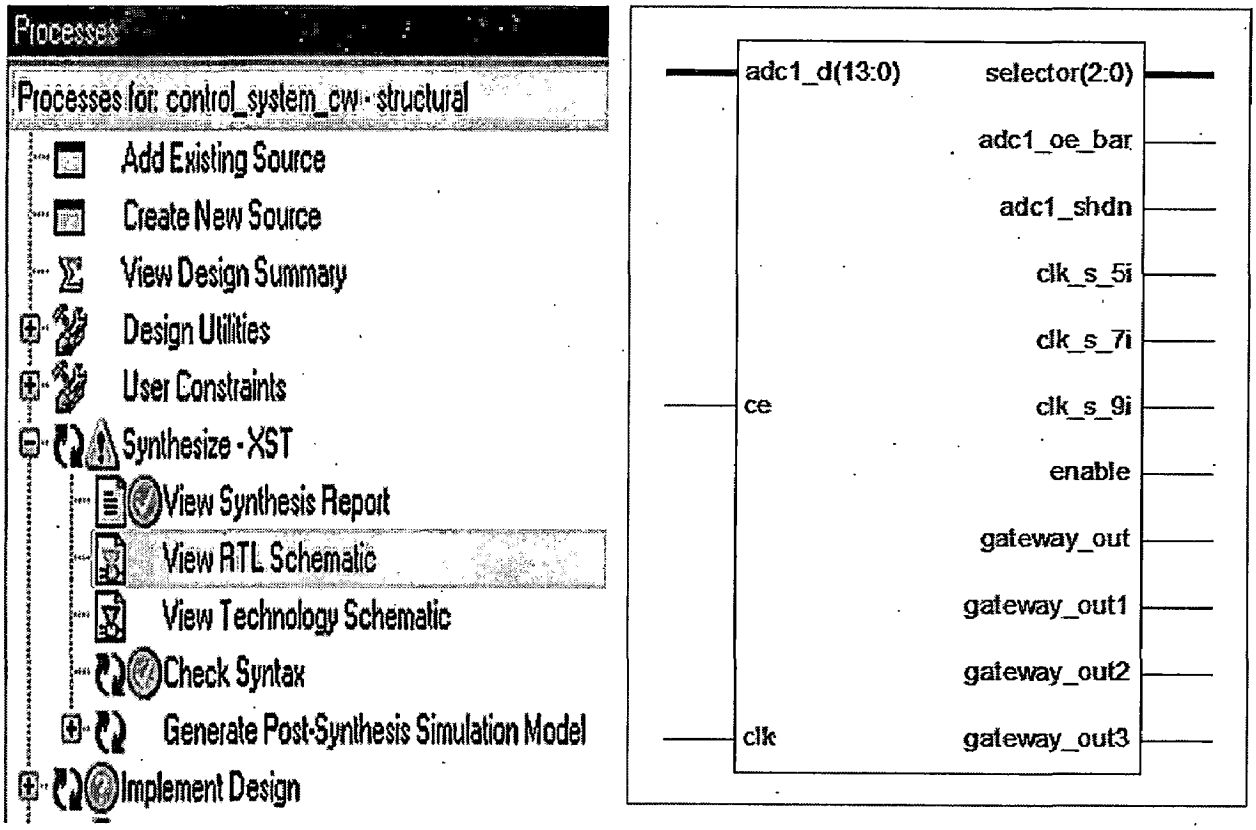


Fig. 4.7 RTL schematic diagram with option in process window.

Now assign the pin locations for clock and I/O pins using Floor plan area (Fig. 3.8) in the process window, it will create an UCF file. The Xilinx PACE, which will open by clicking Floor plan tab in the process window, is a tool where pin locations have to be assigned.

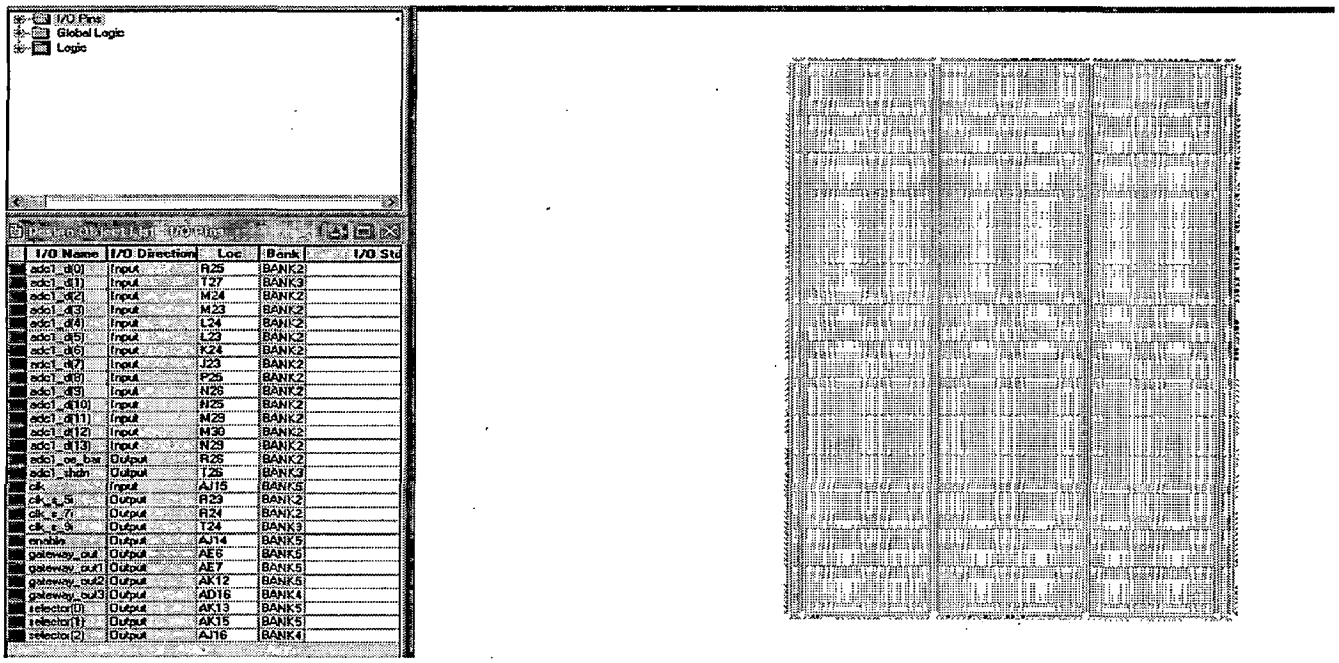


Fig. 4.8 Xilinx Pace window.

The gate pulses are the output which is obtained from the IOCON6 pins as set in the Xilinx PACE. Since the closed loop control is used in this dissertation work, ADC interfacing with the FPGA is done. There is an on-board circuit in the kit which has two single channel ADCs. One of them is interfaced with FPGA chip. Since we have four input signals for the topology implemented through FPGA i.e. input voltage, input source current, capacitor voltage and output DC voltage, we have used a multiplexer to interface with single channel ADC. For the operation of this multiplexer one enable pin and three selector pins are used as output pins on IOCON6 as again shown in figure 4.8. At present clock and ADC are input pins here. The on board ADC has 14 bits. The SIMULINK implementation of control scheme with ADC is as shown in figure 4.9 where there is only one gateway in block. The signals keep coming through it after interval of every 1 microsecond.

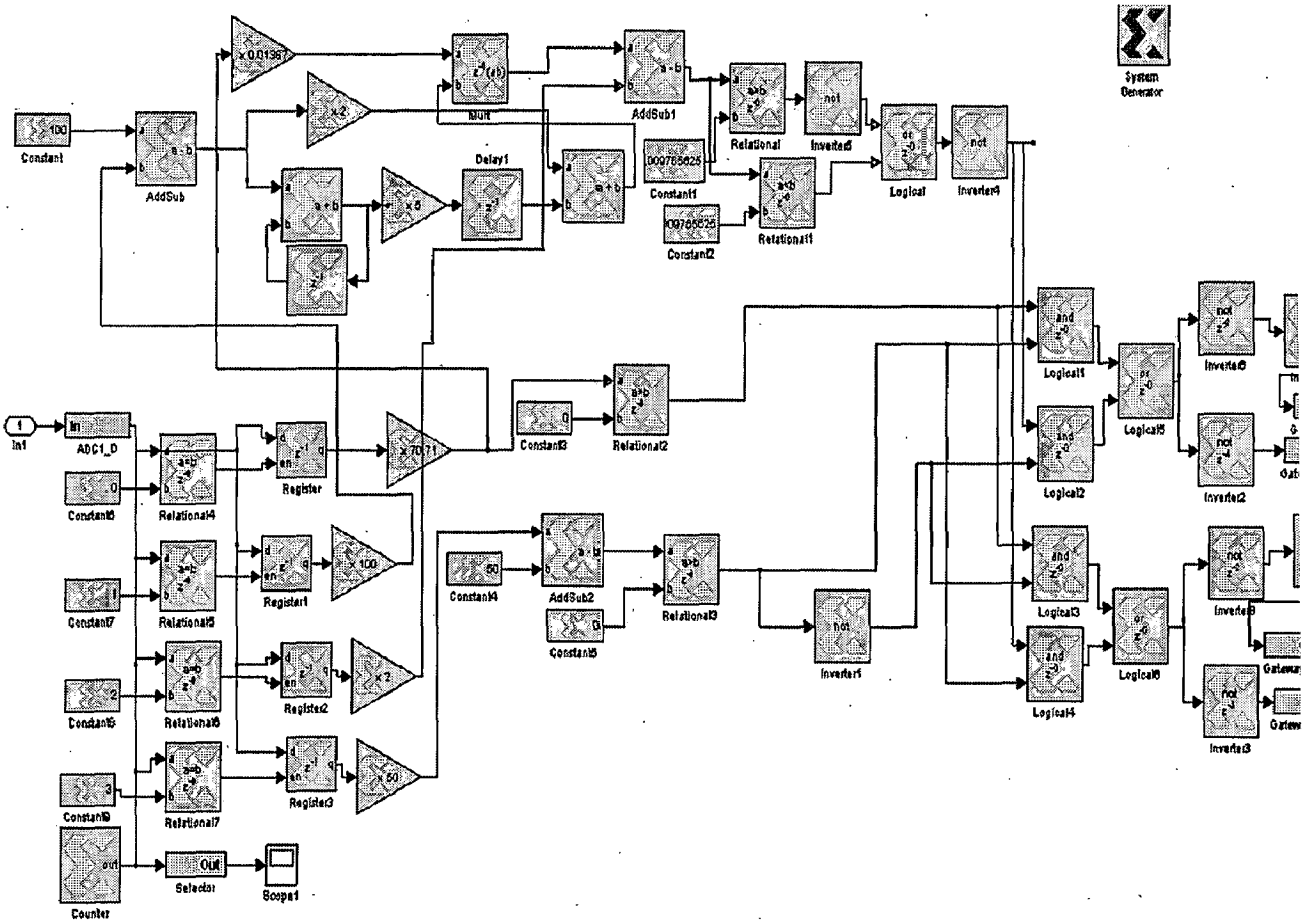


Fig. 4.9 Control model with Xilinx SIMULINK blocks incorporated with ADC.

4.5 Generating BIT STREAM FILE:

The process for generating Bit stream file from VHDL code follows as below.

1. Double click on implement design from process window, inside to this tab there are three steps.

a). Translate b). Mapping c). Place & Route

- Translation and Mapping together will take care of converting Gate level model into device architecture.
- Place & Route will take care of placing the design in device, while optimizing it for speed or area.

2. Double click on Generate Programming File tab, it will generate "Bit Stream file".

4.6 Modes of Downloading Process:

Xilinx provides two tools for downloading purpose.

- iMPACT – is a command line and GUI based tool
- PROM File Formatter

These two tools can be configured by selecting proper jumper settings provided on board.
The modes provided by jumper settings are:

- Boundary Scan Mode
- Master Serial Mode

4.6.1 Boundary Scan Mode:

In boundary scan mode of configuration the Spartan-3 FPGA is directly configured via a JTAG port using the dedicated configuration pins TCK, TMS, TDI and TDO. The jumper setting for selection of boundary scan mode is discussed in Table 4.2 and 4.3.

4.6.2 Master Serial Mode:

In master serial mode the Spartan-3 FPGA is configured through a FLASH PROM. In Master Serial mode, the FPGA automatically loads the configuration bit stream in bit-serial form from configuration flash synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master Serial configuration mode. Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. The jumper setting for selection of Master Serial Mode is discussed in Table 4.2 and 4.3.

4.7 Mode settings:

Mode Selection Jumpers: M0, M1, M2 are the mode selection jumpers used to select the configuration mode either Boundary Scan or Master Serial Mode.

JTAG Chain Selection Jumper: JP2 jumper is used to select the JTAG chain for configuration. When jumper is connected between 2-3, then PROM and FPGA both get added in the JTAG Chain where as connecting jumper between1 and 2 brings only FPGA in Chain.

Configuration Mode	MODE 0	MODE 1	
JTAG	1-2	1-2	Jumper setting 1-2 selects logic 1while 2-3 selects logic 0
MASTER SERIAL	2-3	2-3	

Table 4.1 Mode selection jumper settings.

Configuration Mode	M0	M1	M2
Boundary Scan Mode	1	0	1
Master Serial Mode	0	0	0

Table 4.2 Mode selection table.

4.8 Procedure for downloading using iMPACT:

Double click on 'Configure Device (iMPACT)' from Configure Target Device tab in process window. Then right click in work space and say initialize chain. The device is seen. Then double click on it to assign bitstream file and bypass remaining two blocks and right click over there to program it. While doing this set configuration jumper connections as shown below window and also change jumper JP2 to 1-2. If the device is programmed properly, it says programming succeeded or else programming failed. The DONE LED glows green if programming succeeds. This case is shown in figure 4.10 with program succeeded appearing on the window.

4.9 Procedure for downloading using PROM:

For making the program available even after power is gone select master serial mode by using jumper configuration modes as shown below window and set jumper JP2 to 2-3. In the process window double click on generate target PROM/ACE file (.mcs). Now double click on boundary scan in the sources window and then right click on the first block in the chain then click on program, now the following window showing "program succeeded" will appear as shown in figure 4.11. Now finally click on second block of the chain and then double click on program option in process window, if program is properly dumped into FPGA the window appears as shown in Fig 4.12.

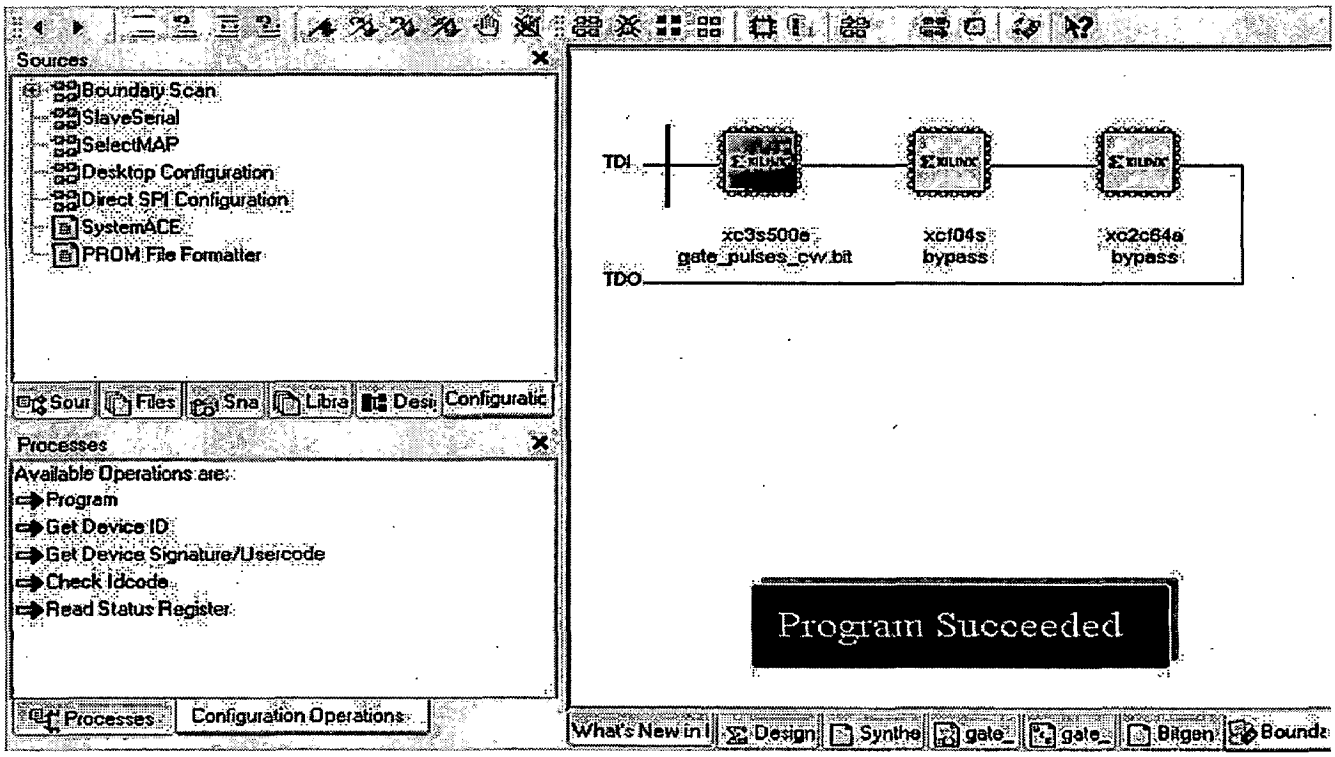


Fig. 4.10 Program succeeded window.

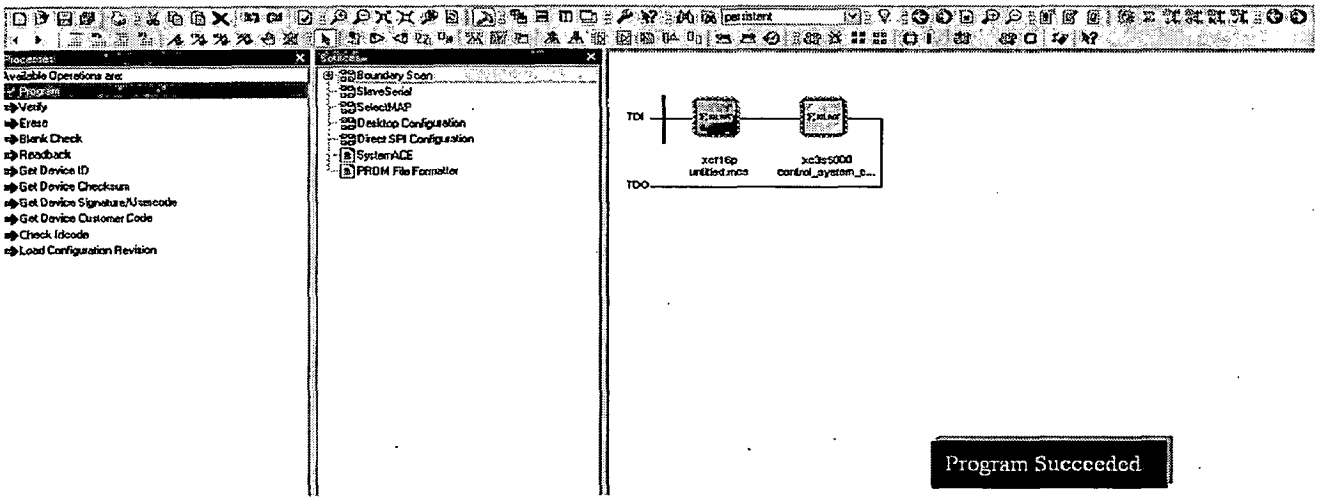


Fig. 4.11 Program succeeded window for .mcs file.

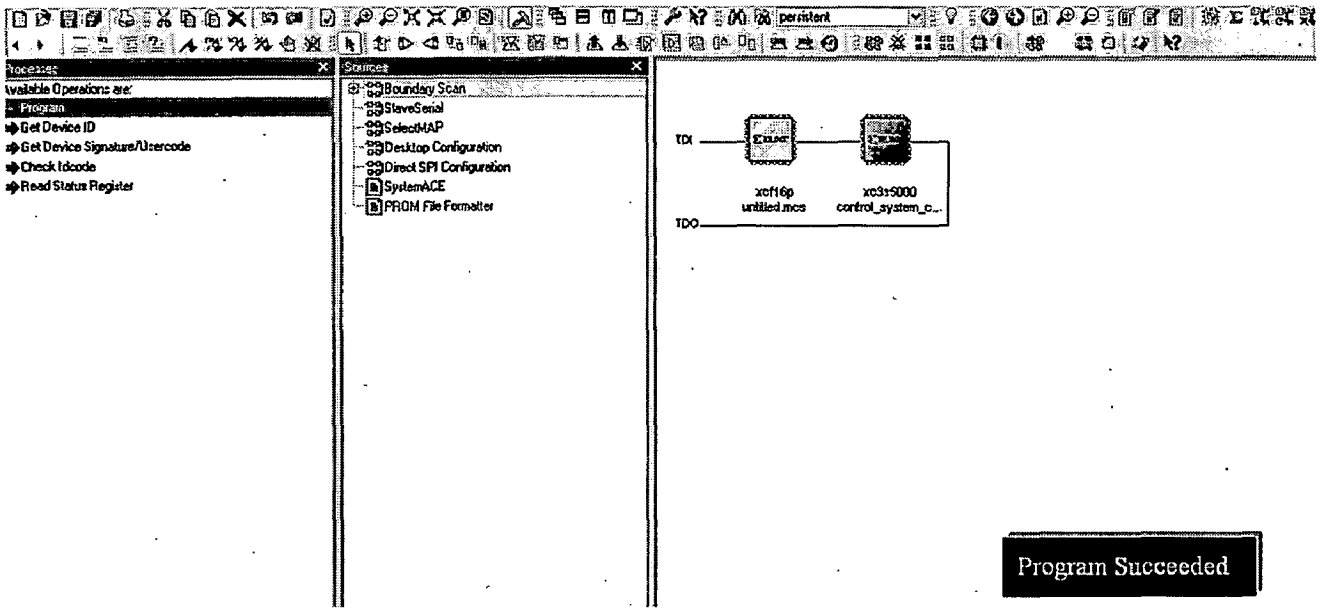


Fig. 4.12 Final step of dumping the code into FPGA kit.

This was the whole process of dumping the VHDL code into the FPGA kit.

4.10 Conclusion:

In this chapter, the detailed description is presented for Xilinx System Generator and procedure in steps is explained starting from MATLAB SIMULINK (.mdl file) to bit stream file generation and downloading process into the FPGA kit.

The SIMULINK model of the simple PWM control scheme is presented along with the system generator based implementation.

Chapter 5: Hardware Implementation and Development of Multilevel Rectifier

In this chapter the design procedure of the hardware developed for the implementation of the multilevel rectifier is described. All the circuits used in the making of hardware prototype has been described.

Before that we have also described about the operation principle of the multilevel rectifier topology which is implemented on hardware. How it gives the level of voltages on AC side due to which input source current drawn is sinusoidal and power factor is improved.

5.1 Power circuit:

Figure 5.1 shows the power circuit of capacitor clamped multilevel rectifier topology. This topology is a single phase half bridge PWM rectifier [].

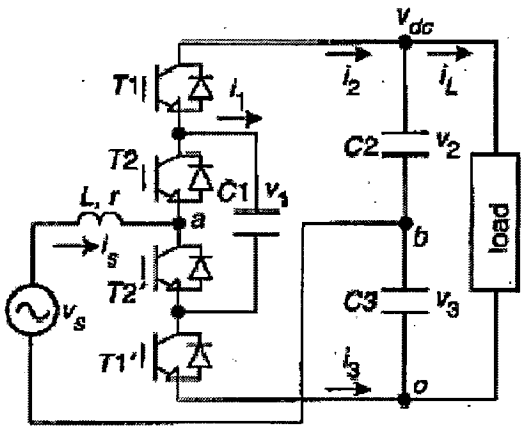


Fig. 5.1 Power circuit of multilevel capacitor clamp rectifier.

This topology consists of four switching devices, one clamped capacitor, one boost inductor and two DC side capacitors across which the load is connected. The voltage stress across each of the switches is $V_{dc}/2$.

5.1.1 Operation Principle:

Firstly, to avoid all the power switches conducting at same time, there is a certain constraint put on these switches which is defined as $T_i + T_{i'} = 1$, i = 1,2 where $T_i = 1$ (or 0) if switch is turned ON (or OFF). According to the switching states of the two independent switches T_1 and T_2 there are four switching states which is summarized in table 5.1. These switching states generate three voltage levels on the AC side. There are three modes of operation for this topology to generate the voltage levels as described below.

Mode 1: In this mode switches T1 and T2 are turned ON to generate the voltage $V_{ab} = V_{dc}/2$ assuming the voltage across each capacitor $V_{dc}/2$. In this the line current decreases because the voltage across the boost inductor is negative.

Mode 2: In this mode there are two operation states, first when switches T1 and T2' are turned ON to generate the voltage level Vab = 0. In this case positive line current charges capacitor C2 and discharges capacitor C1. Second, when switches T1' and T2 are turned ON also to generate the voltage level Vab = 0. In this case positive line current charges capacitor C1 and discharges capacitor C3. In this case the mains current is increasing if mains voltage is positive and mains current is decreasing if mains voltage is negative.

Mode 3: In this mode switches T1' and T2' are turned ON to generate the voltage level Vab = -$V_{dc}/2$. In this case the line current increases because the voltage across the boost inductor is positive.

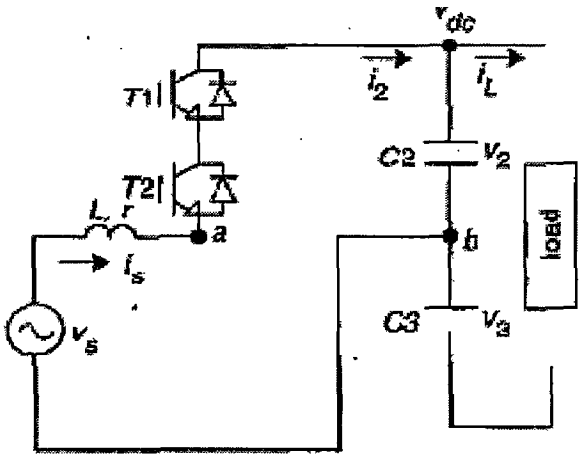
These modes of operation are shown in figure 5.2.

The switching states with proper modes of operation are summarized in table 5.1.

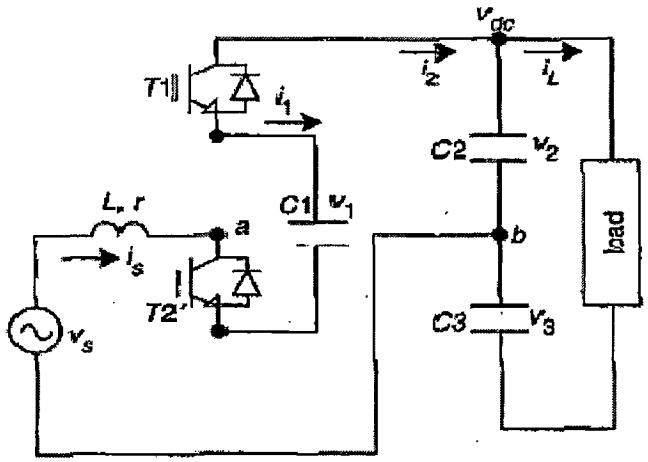
Valid switching state	T1	T2	V_{ab}	$V_{ab}(V_1 = V_2 = V_3 = V_{dc}/2)$	Mode
1	1	1	V_2	$V_{dc}/2$	1
2	1	0	$-V_1+V_2$	0	2

3	0	1	V_1-V_3	0	2
4	0	0	-V_3	-V_{dc}/2	3

Table 5.1 Summary of switching states.



a



b

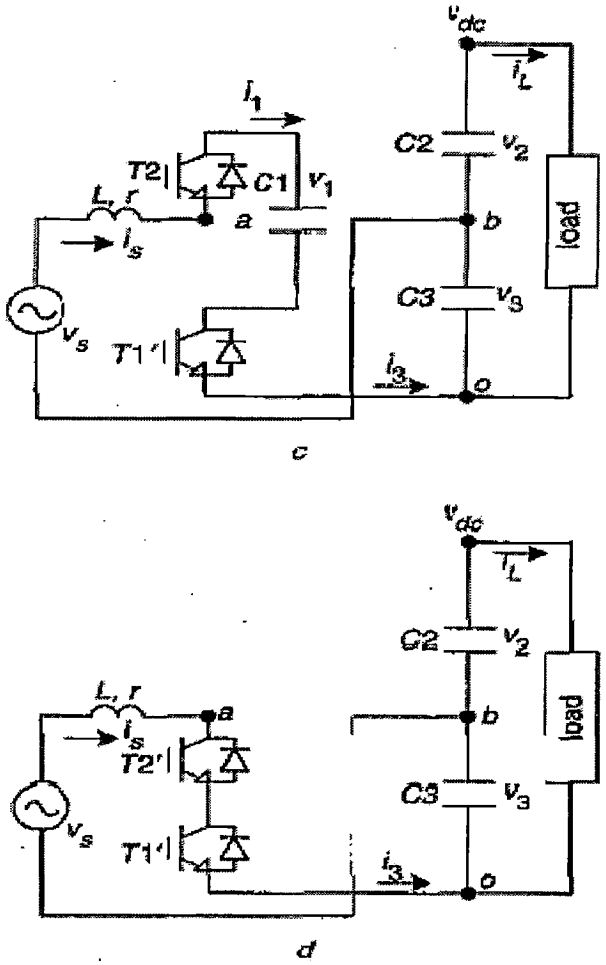


Fig. 5.2 Operation modes of the rectifier (a) Mode1 (b) Mode2 (c)Mode 2(d) Mode 3.

5.1.2 Control Scheme:

This rectifier topology uses unipolar PWM control strategy to improve the input power factor so as to maximize the efficiency at the output receiving end. The aim of this control scheme is also to balance the neutral point and to maintain the output DC voltage. A PI controller is used in the scheme to regulate the DC output voltage. Input mains voltage is given to a phase locked loop (PLL) to generate the unit template and is multiplied with the output of PI controller to give the reference current which is compared with the actual input source current. This error is given to hysteresis current controller to track the input current so that it remains sinusoidal. This scheme also incorporates the balancing of capacitor voltage C1. Based on the modes of operation

described earlier, appropriate switching signals are generated. The figure 5.3 shows the control block diagram.

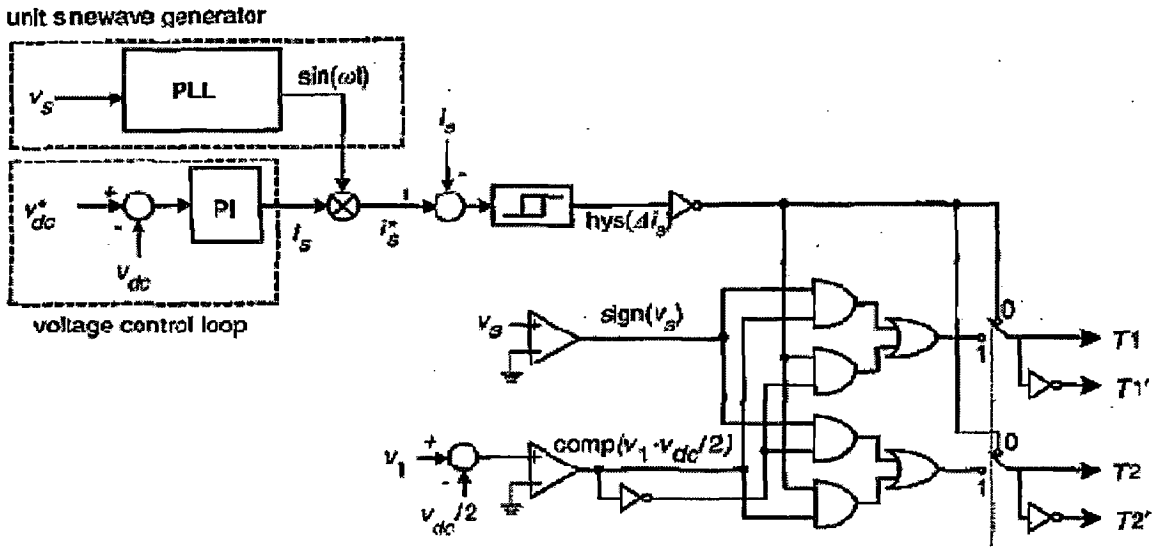


Fig. 5.3 Control block diagram for the rectifier topology.

5.2 Hardware development:

The system has been developed for the closed loop control containing following circuits:

1. Power circuit.
2. Pulse amplification and isolation circuit.
3. Power supplies.
4. Voltage sensing circuits.
5. Current sensing circuit.
6. Multiplexer chip followed by a buffer.

5.2.1 Power circuit:

Switching devices used here are MOSFETS IRPF 460. These MOSFETS have an inbuilt anti-parallel diode. Heat sinks are used for cooling purpose. Electrolytic capacitors are used in the design of capacity 2200μF. The purpose of these capacitors is to absorb the current ripple and to maintain the voltage balance.

5.2.2 Pulse amplification and isolation circuit:

This circuit is basically the driving circuit of MOSFETs. The MOSFET used in this project is IRFP460 which has the maximum threshold V_{gs} voltage of 4V. The circuit used in the hardware is giving the output of 12V which is good enough to drive the MOSFETs. The pulse amplification and the isolation circuit is shown in the figure 5.4. The opto-coupler MCT 2E provides the necessary isolation between low voltage isolation circuit and the high voltage power circuit. The pulse amplification is provided by the output amplifier transistor 2N222. When the input gating is +5 volt level, the transistor saturates, the LED conducts and the light emitted by it falls on the base of the photo-transistor, thus forming its base drive. The output transistor thus receives no base drive and remains in cut-off state and a +12 volt pulse (amplified) appears at its collector terminal. When the input gating pulse reaches ground level, the input switching transistor goes to cut-off state and LED remains off, thus emitting no light and therefore the phototransistor remains off. The output transistor receives base drive and saturates, hence the output falls to zero. Therefore, the circuit provides the proper amplification and isolation. Further, since the slightest spike above 20V can damage the MOSFET, a 12V zener diode is connected across the output isolation circuit. This clamps the triggering voltage to 12V. Switching high current in short time gives rise to voltage transients that could exceed the rating of the MOSFET. Snubbers are therefore needed to protect the switch from transients. Snubber circuit for MOSFET is shown in figure 5.5. The diode prevents the discharging of the capacitor via the switching device, which could damage the device due to large discharging current. An additional protective metal oxide varistor (MOV) is used across the devices. Such four individual circuits are used for each of the four switches. The hardware circuit is shown in figure 5.6.

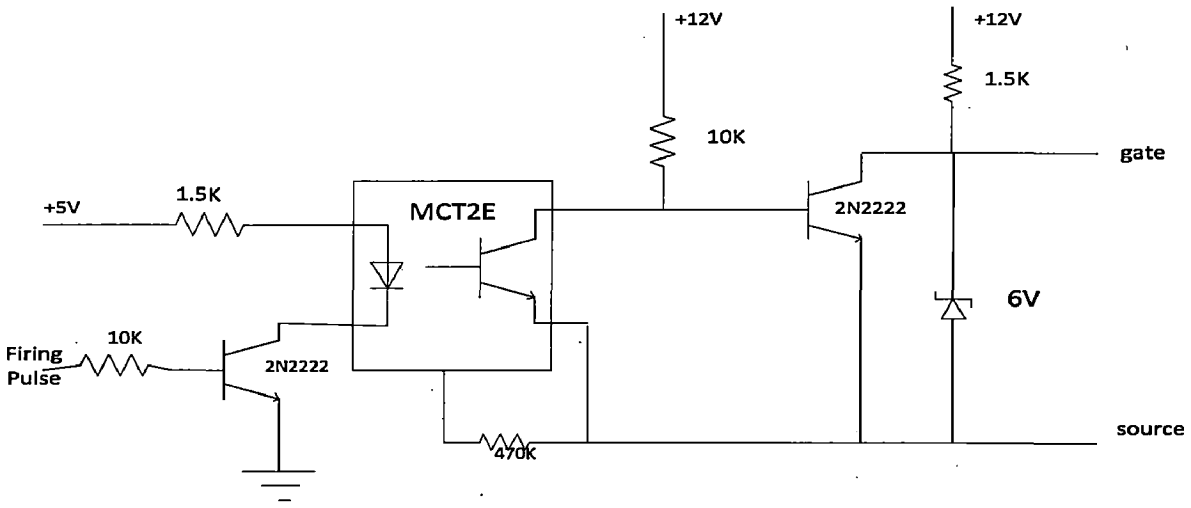


Fig. 5.4 Pulse amplification and isolation circuit.

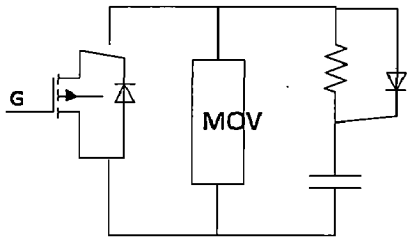


Fig. 5.5 Snubber circuit.

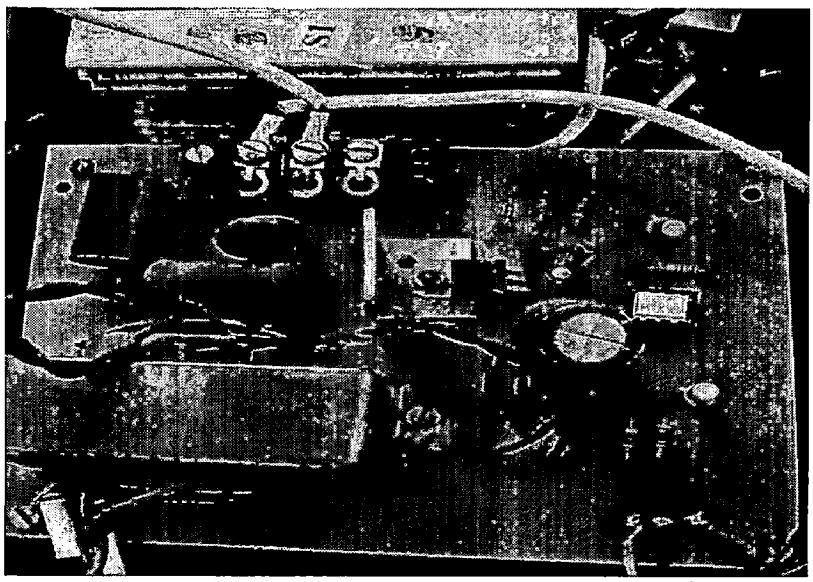


Fig. 5.6 Hardware circuit for driving MOSFETs.

5.2.3 Power Supplies:

DC regulated supplies of +12,-12 and +5 volts are required to provide the biasing to various ICs, hall effect current sensor and various other circuits used in the hardware like driving circuit of MOSFETs. For this purpose the ICs 7812, 7912, 7805 are used for generating regulated supply of +12, -12, +5 volts respectively. The circuit diagram of the power supplies is as shown in figure 5.7(a)&(b). The equivalent hardware prototype is shown in figure 5.8.

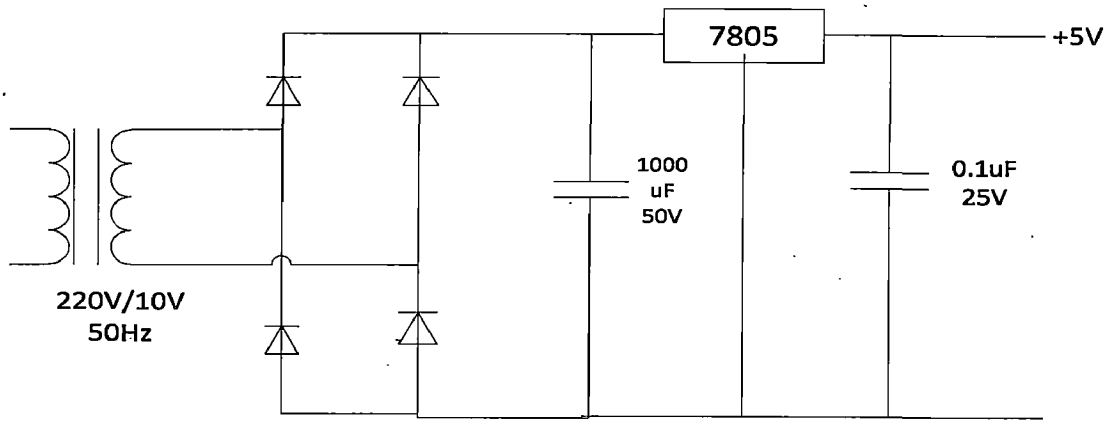


Fig. 5.7(a) Power supply circuit for +5 volts.

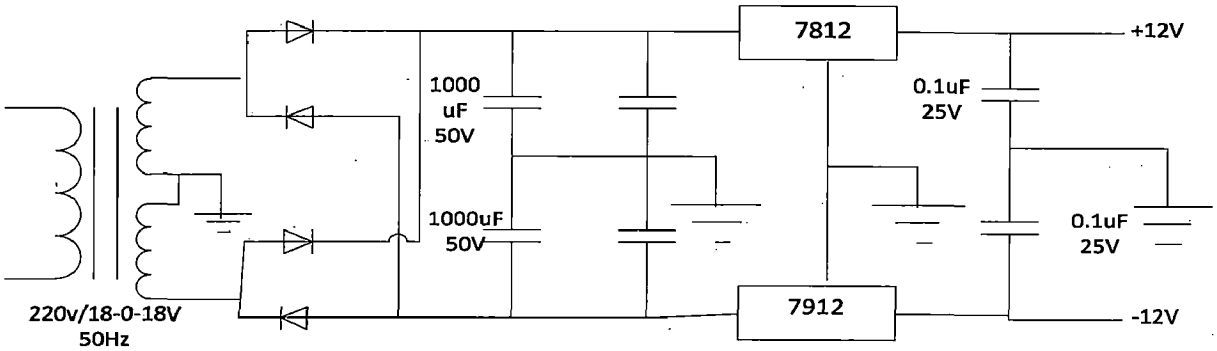


Fig. 5.7(b) Power supply circuit for +12 and -12 volts.

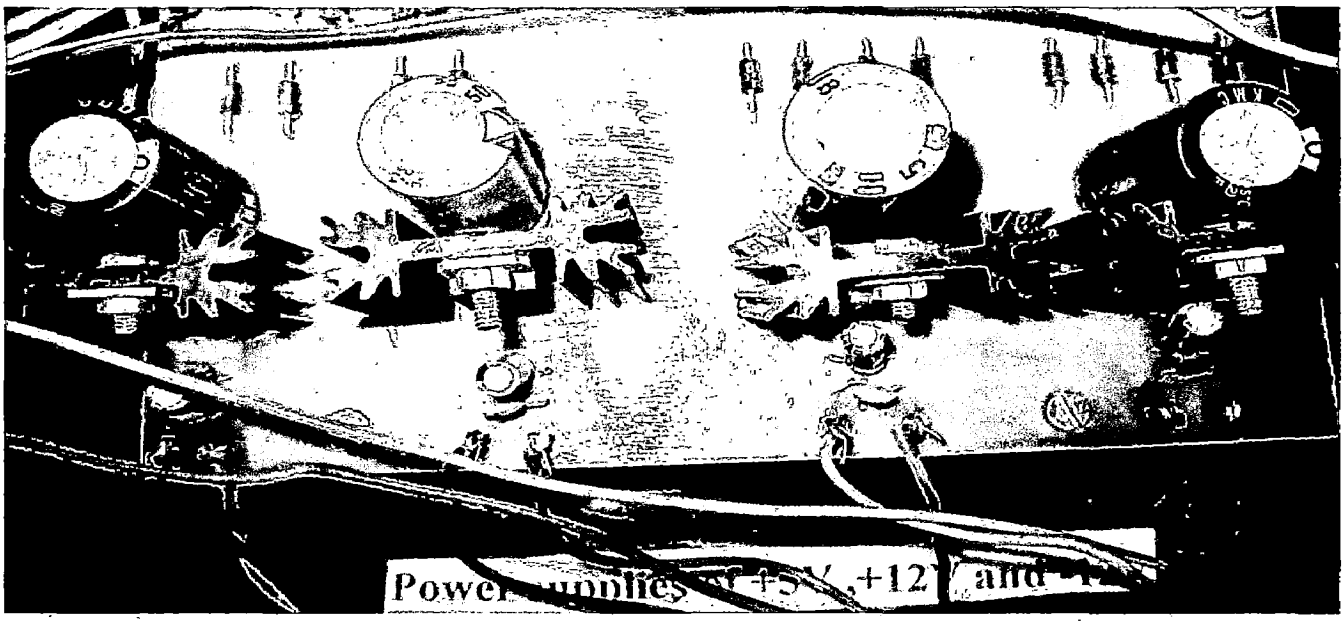


Fig. 5.8 Power supplies on hardware.

5.2.4 AC and DC voltage sensing circuit:

The closed loop control scheme involves the sensing of three voltages: AC supply mains, voltage across the flying capacitor and DC output voltage. Out of these voltages two are DC and one is AC. The sensing circuit PCB is designed in such a way so as to sense both AC and DC voltages. The sensing circuit diagram is shown in figure 5.9. Resistors are used to scale down the voltage within the range of AD202 which is an isolation amplifier. Op-amp circuits are used at the output of AD202 for scaling. The scaling using the variable resistor is done in such a way that the output is within the range of +1V and -1V. This range is for the ADC which is attached on-board of FPGA tool kit. This ADC takes the voltage sensed by circuits as inputs. Since this ADC is a single channel ADC, a multiplexer circuit is also used for four inputs which is explained further. The hardware prototype is shown in figure 5.10.

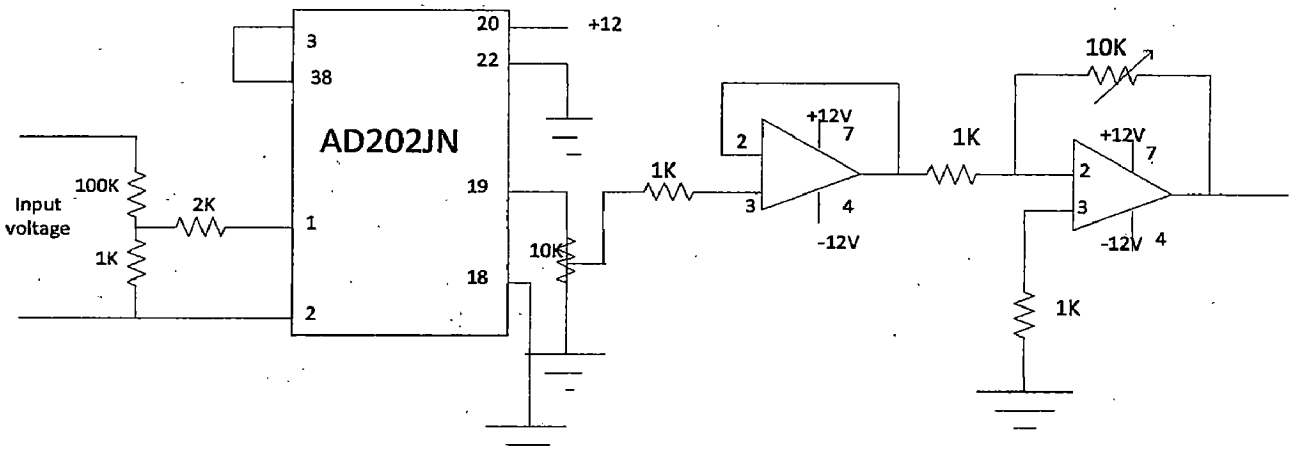


Fig. 5.9 Voltage sensing circuit.

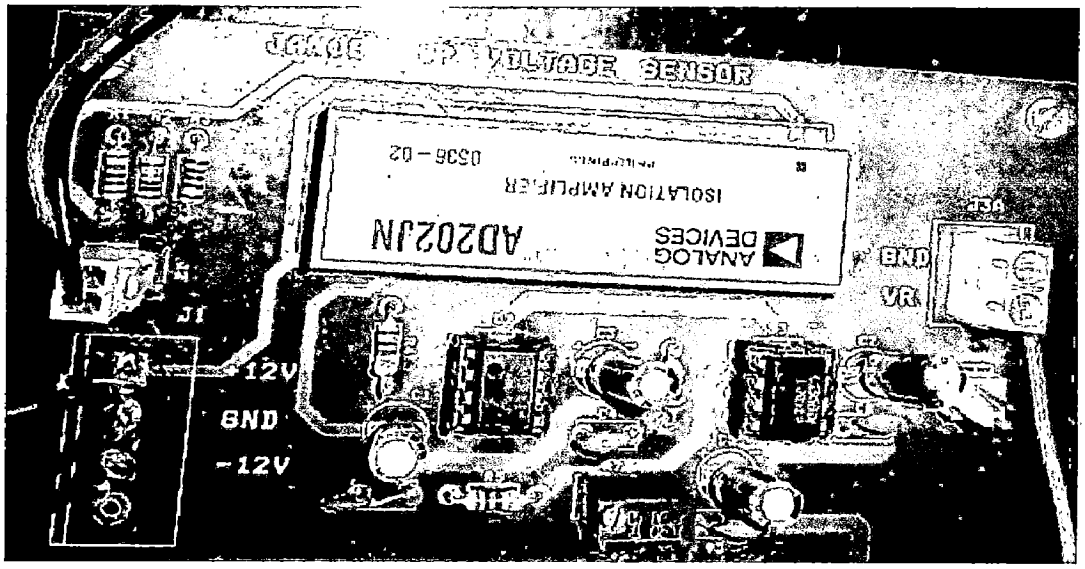


Fig. 5.10 Hardware prototype of voltage sensing circuit.

5.2.5 AC current sensing circuit:

AC source current is sensed using PCB mounted Hall Effect current sensors (HTP 25). Thi current sensor provide galvanic isolation between high voltage power circuit and the low voltag control circuit and require a nominal supply of +-12V. It has the transformation ratio of 1000:1 Here also the scaling is done keeping in mind the input range of ADC of FPGA tool kit a

mentioned previously. The sensor circuit diagram is shown in figure 5.11. The hardware prototype of this circuit is shown in figure 5.12.

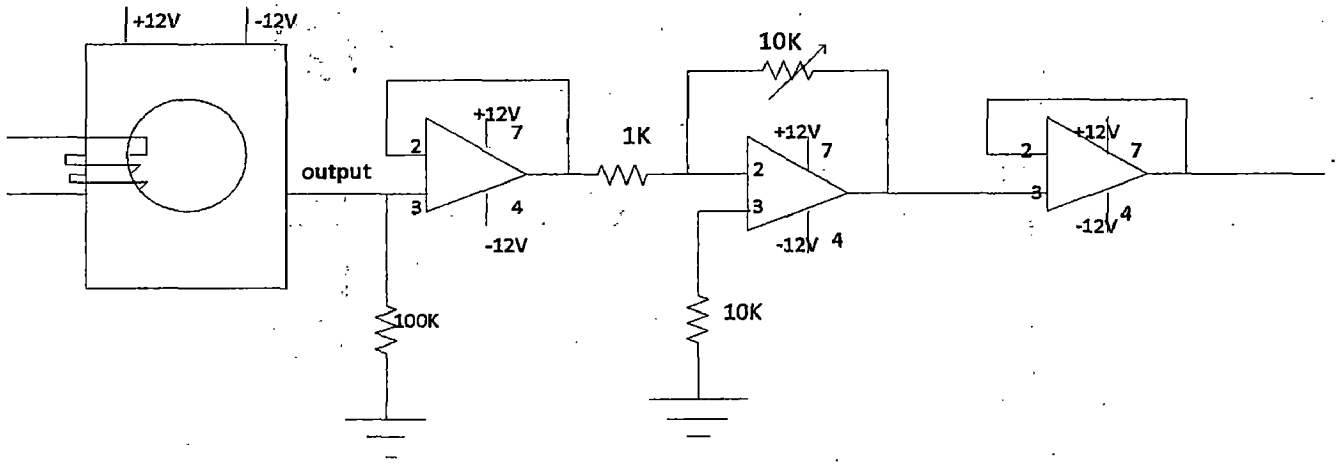


Fig. 5.11 AC current sensing circuit.

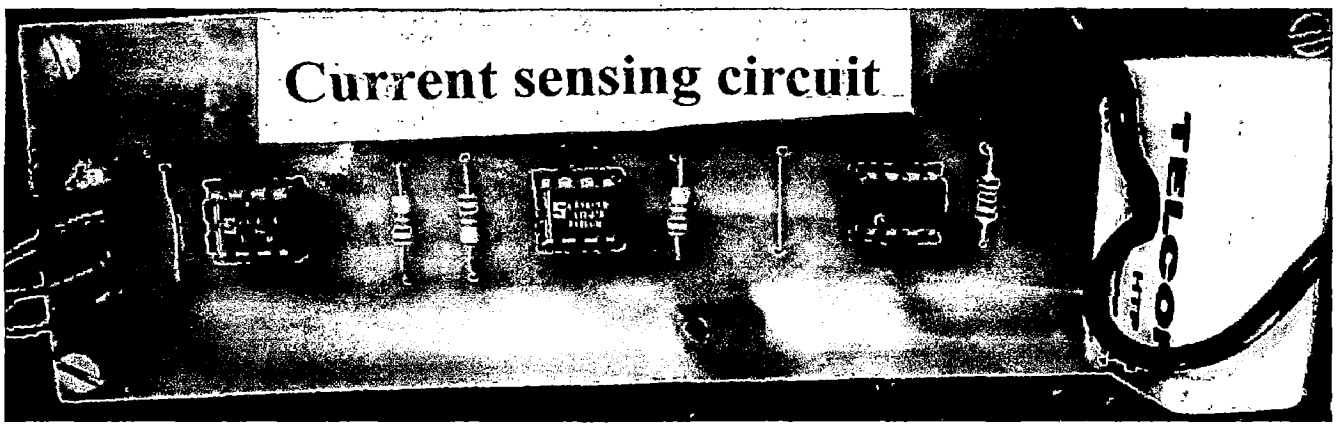


Fig. 5.12 Hardware prototype of current sensing circuit.

5.2.6 Multiplexer circuit:

This circuit is used for four input signals of closed loop control scheme. Since the ADC of FPGA kit is single channel this multiplexer chip is used followed by a buffer chip. The biasing supplies used in its operation are +12 and -12 volts. Four bits are used to select the channels. An enable is also connected to high i.e. it is kept as 1 digitally. Buffer is used to amplify the signals. Hardware prototype is also shown in figure 5.13.

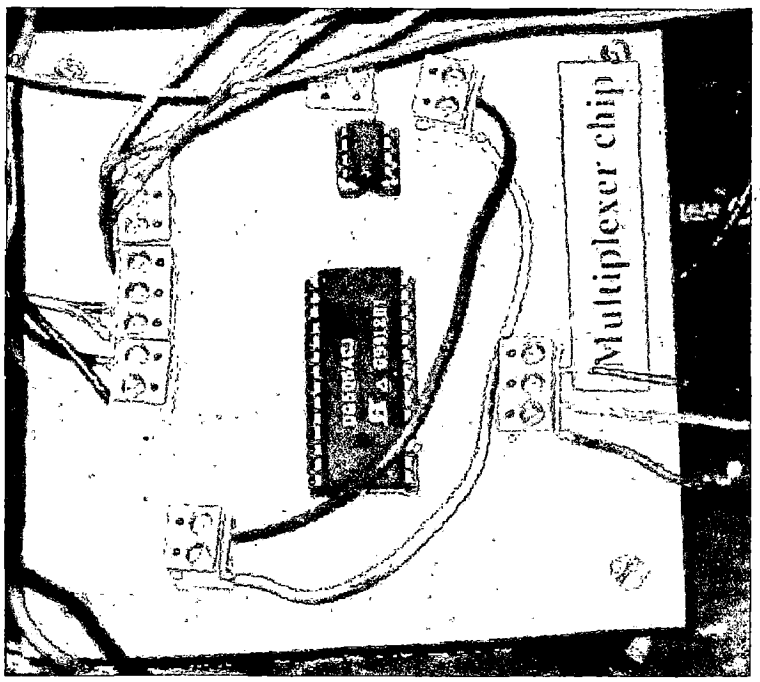


Fig. 5.13 Hardware prototype of multiplexer circuit.

The complete hardware prototype of the multilevel rectifier is shown in figure 5.14.

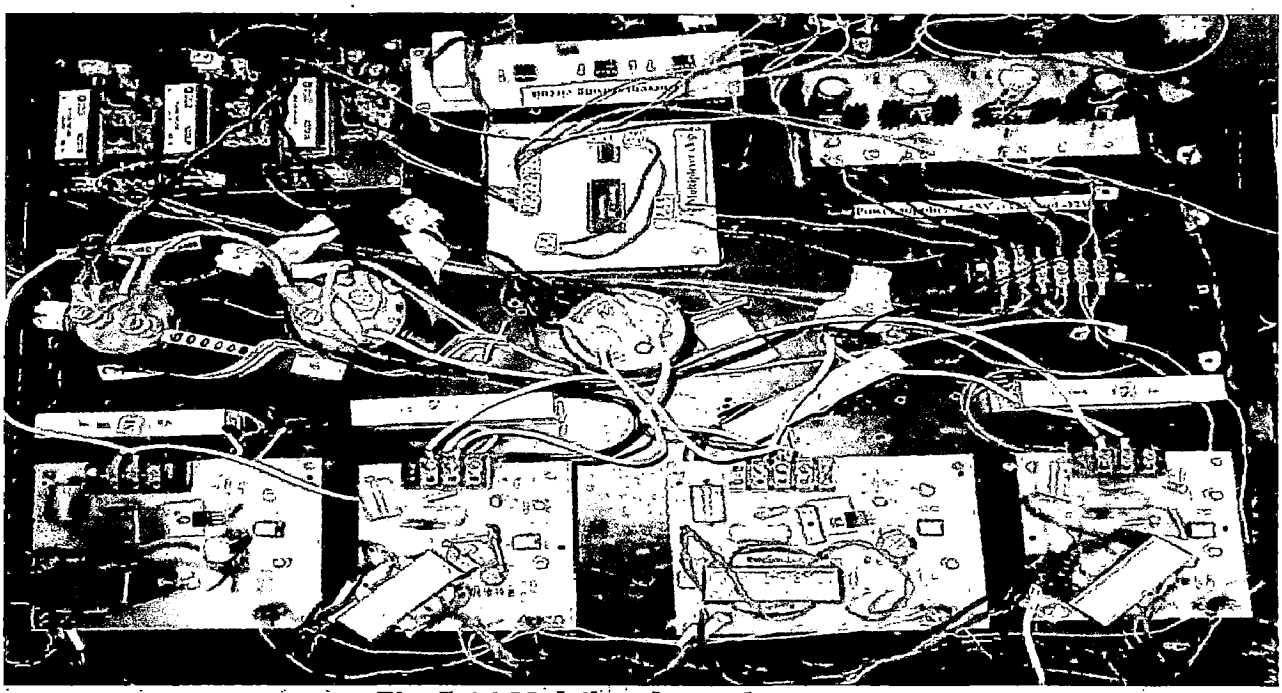


Fig. 5.14 Multilevel rectifier set up.

The hardware set up with FPGA kit as digital control is shown in figure 5.15.

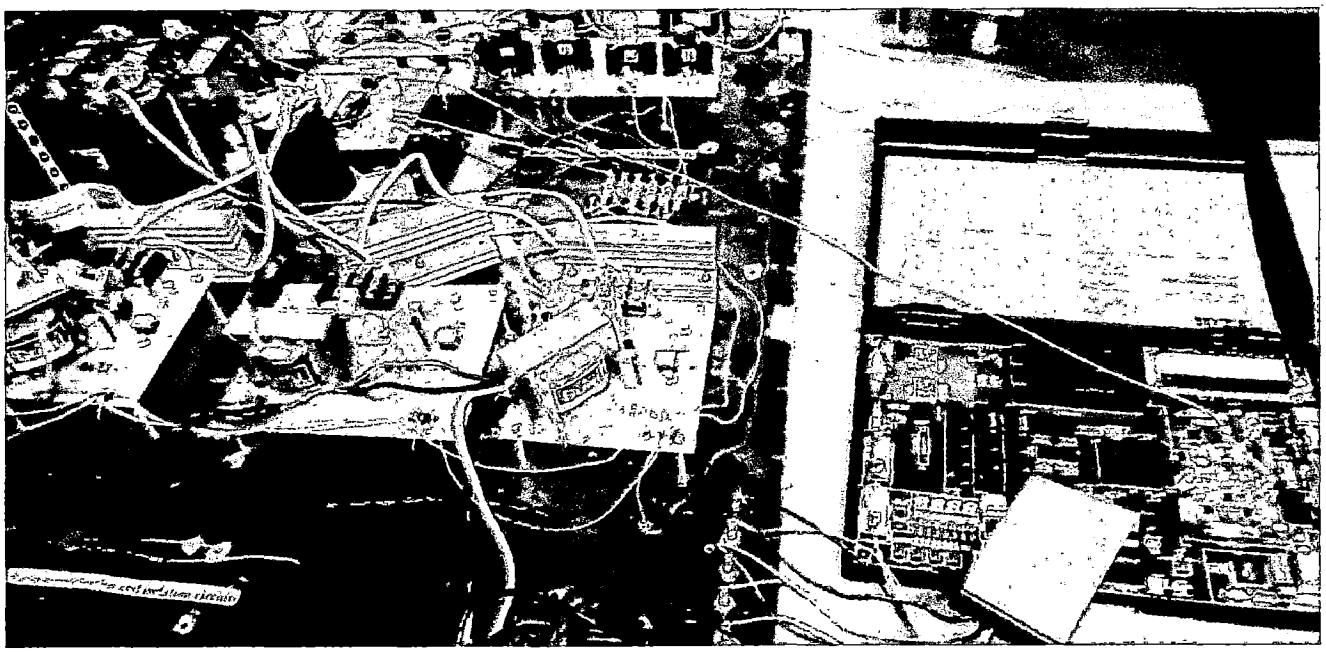


Fig. 5.15 FPGA control to feed the firing pulses.

5.3 Conclusion:

In this chapter the hardware development is presented with all the circuits made in laboratory.

Chapter 6: Conclusions and Future Scope

6.1 Conclusions:

This work has the following contributions:

- Importance of multilevel rectifiers over conventional and traditional rectifiers.
- Comparison of multilevel rectifiers with other conventional converters.
- Explanation of control strategies available for these rectifiers.
- Simulations of different topologies of multilevel rectifiers in MATLAB employing simple PWM scheme.
- Analysis of THDs in input source current and their comparisons with varying load current and input power supply.
- Hardware is developed in laboratory for a particular multilevel rectifier topology.
- Control scheme is implemented through FPGA Spartan 3 kit.

6.2 Future Scope in this work:

- Future work has to extend to getting experimental results.
- Other control schemes are to be implemented on FPGA besides simple PWM which has been implemented in this work.
- In the closed loop, PI controller parameters are decided by hit and trial method but it should be calculated by modeling the system.

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